TECHNICAL DATA SHEET

6 Lake Street, Lawrence, MA 01841
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NPN SILICON TRANSISTOR

Qualified per MIL-PRF-19500/317

DEVICES

2N2369A **2N2369AUB** **2N4449**
2N2369AU **2N2369AUBC ***
2N2369AUA

LEVELS

JAN
JANTX
JANTXV
JANS

*** Available to JANS quality level only.**

ABSOLUTE MAXIMUM RATINGS ***(T_C = +25°C unless otherwise noted)***

Parameters / Test Conditions	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Emitter-Base Voltage	V_{EBO}	4.5	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Collector-Emitter Voltage	I_{CES}	40	Vdc
Total Power Dissipation @ T_A = +25°C: 2N2369A; 2N4449	P_T	0.36 (1)	W
UA, UB, UBC		0.36 (1, 3)	
U		0.50 (2)	
Operating & Storage Junction Temperature Range	T_{op}, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

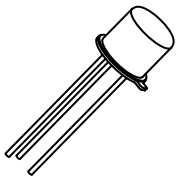
Parameters / Test Conditions	Symbol	Value	Unit
Thermal Resistance, Ambient-to-Case: 2N2369A; 2N4449	$R_{\theta JA}$	400	°C/W
UA, UB, UBC		486 (3)	
U		350	

Note:

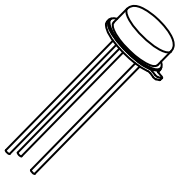
1. Derate linearly 2.06 mW°/C above T_A = +25°C.
2. Derate linearly 3.44 mW°/C above T_A = +54.5°C.
3. Mounted on FR-4 PCB (1Oz. Cu) with contacts 20 mils larger than package pads.

ELECTRICAL CHARACTERISTICS ***(T_A = +25°C, unless otherwise noted)***

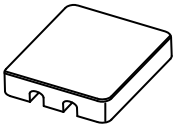
Parameters / Test Conditions	Symbol	Min.	Max.	Unit
OFF CHARACTERTICS				
Collector-Emitter Breakdown Voltage I_C = 10mAdc	$V_{(BR)CEO}$	15		Vdc
Collector-Base Cutoff Current V_{CE} = 20Vdc	I_{CES}		0.4	µAdc



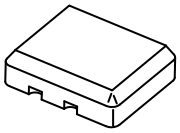
TO-18 (TO-206AA)
2N2369A



TO-46 (TO-206AB)
2N4449



SURFACE MOUNT
UA



SURFACE MOUNT
UB & UBC
(UBC = Ceramic Lid Version)



SURFACE MOUNT
U (Dual Transistor)

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ELECTRICAL CHARACTERISTICS ***(T_A = +25°C, unless otherwise noted)***

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Emitter-Base Cutoff Current V_{EB} = 4.5Vdc V_{EB} = 4.0Vdc	I_{EBO}		10 0.25	µAdc
Collector- Base Cutoff Current V_{CB} = 40Vdc V_{CB} = 32Vdc	I_{CBO}		10 0.2	µAdc
ON CHARACTERISTICS (1)				
Forward-Current Transfer Ratio I_C = 10mAdc, V_{CE} = 0.35Vdc I_C = 30mAdc, V_{CE} = 0.4Vdc I_C = 10mAdc, V_{CE} = 1.0Vdc I_C = 100mAdc, V_{CE} = 1.0Vdc	h_{FE}	 40 30 40 20	 120 120 120 120	
Collector-Emitter Saturation Voltage I_C = 10mAdc, I_B = 1.0mAdc I_C = 30mAdc, I_B = 3.0mAdc I_C = 100mAdc, I_B = 10mAdc	$V_{CE(sat)}$		 0.20 0.25 0.45	Vdc
Base-Emitter Saturation Voltage I_C = 10mAdc, I_B = 1.0mAdc I_C = 30mAdc, I_B = 3.0mAdc I_C = 100mAdc, I_B = 10mAdc	$V_{BE(sat)}$	 0.70 0.80	 0.85 0.90 1.20	Vdc

DYNAMIC CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Forward Current Transfer Ratio I_C = 10mAdc, V_{CE} = 10Vdc, f = 100MHz	$\|h_{fe}\|$	5.0	10	
Output Capacitance V_{CB} = 5.0Vdc, I_E = 0, 100kHz ≤ f ≤ 1.0MHz	C_{obo}		4.0	pF
Input Capacitance V_{EB} = 0.5Vdc, I_C = 0, 100kHz ≤ f ≤ 1.0MHz	C_{ibo}		5.0	pF

SWITCHING CHARACTERISTICS

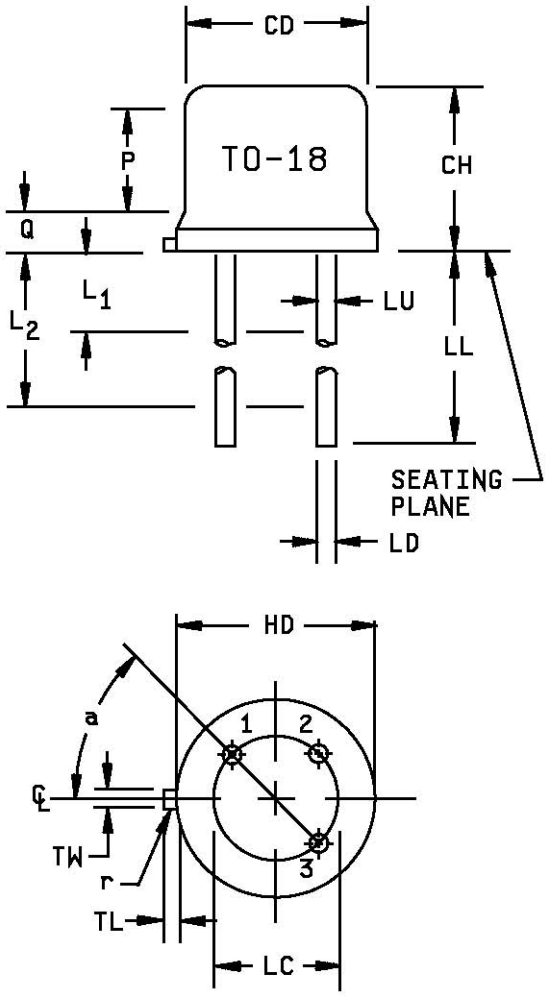
Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Turn-On Time I_C = 10mAdc; I_{B1} = 3.0mAdc, I_{B2} = -1.5mAdc	t_{on}		12	ηs
Turn-Off Time I_C = 10mAdc; I_{B1} = 3.0mAdc, I_{B2} = -1.5mAdc	t_{off}		18	ηs
Charge Storage Time I_C = 10mAdc; I_{B1} = 10mAdc, I_{B2} = 10mAdc	t_S		13	ηs

(1) Pulse Test: Pulse Width = 300µs, Duty Cycle ≤ 2.0%.

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PACKAGE DIMENSIONS



Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8,13
LU	.016	.019	0.41	0.48	7,8
L_1		.050		1.27	7,8
L_2	.250		6.35		7,8
P	.100		2.54		5
Q		.030		0.76	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	3
r		.010		0.25	10
α	45° TP		45° TP		6

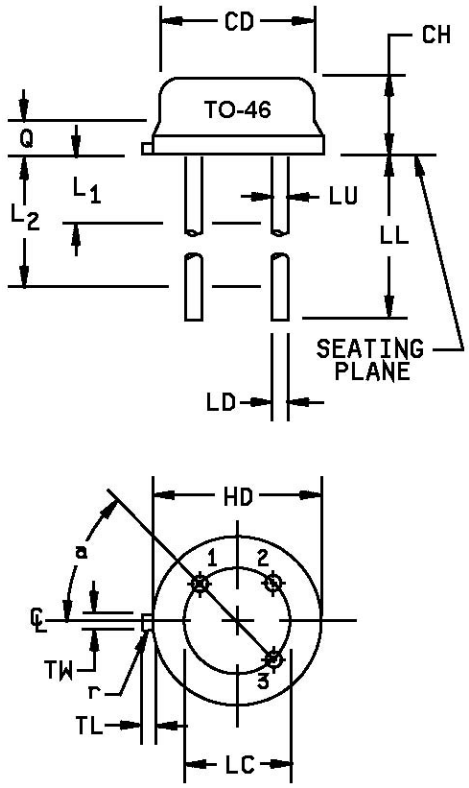
NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TH shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L1 and L2. Dimension LD applies between L2 and LL minimum. Diameter is uncontrolled in L1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.

FIGURE 1. Physical dimensions TO-18 (2N2369A).

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Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.065	.085	1.65	2.16	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		5
LD	.016	.021	0.41	0.53	
LL	.500	1.750	12.70	44.45	6
LU	.016	.019	0.41	0.48	6
L_1		.050		1.27	6
L_2	.250		6.35		6
Q		.040		1.02	3
TL	.028	.048	0.71	1.22	8
TW	.036	.046	0.91	1.17	4
r		.010		0.25	9
α	45° TP		45° TP		

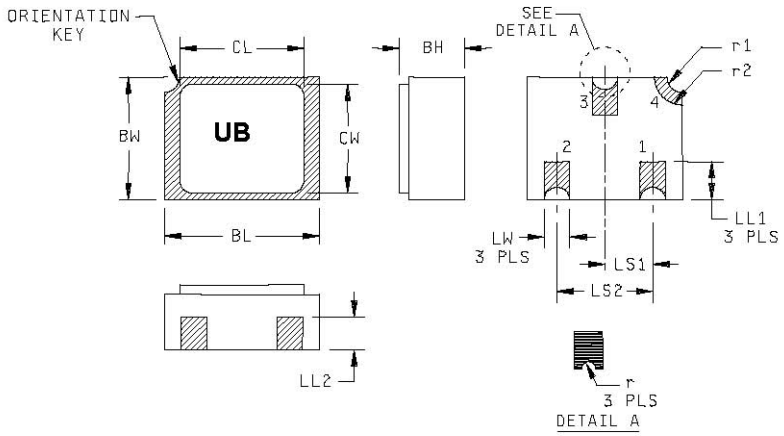
NOTES:

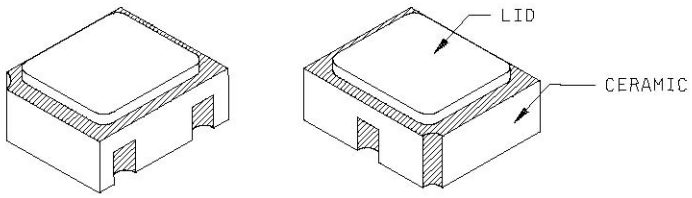
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of TP relative to tab. Device may be measured by direct methods or by gauge.
6. Symbol LU applies between L1 and L2. Dimension LD applies between L2 and LL minimum.
7. Lead number three is electrically connected to case.
8. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
9. Symbol r applied to both inside corners of tab.
10. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.
11. Lead 1 is emitter, lead 2 is base, and lead 3 is collector.

FIGURE 2. Physical dimensions - TO-46 (2N4449).

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NOTES:

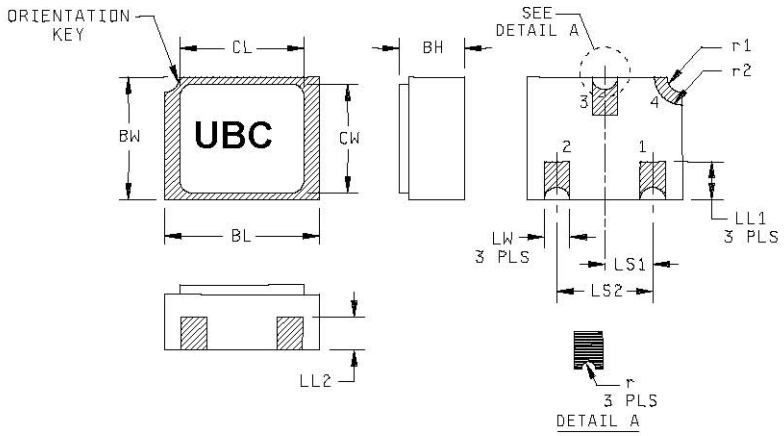
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas.
4. Lid material: Kovar.
5. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
6. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

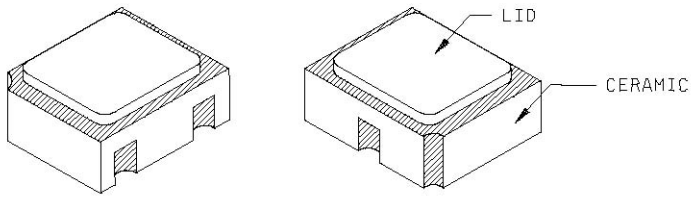
Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.056	1.17	1.42	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.96	
LL2	.017	.035	0.43	0.89	
LS1	.036	.040	0.91	1.02	
LS2	.071	.079	1.81	2.01	
LW	.016	.024	0.41	0.61	
r		.008		.203	
r1		.012		.305	
r2		.022		.559	

FIGURE 3. Physical dimensions - surface mount (UB version, 2N2369AUB).

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Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.071	1.17	1.80	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.96	
LL2	.017	.035	0.43	0.89	

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
LS1	.036	.040	0.91	1.02	
LS2	.071	.079	1.81	2.01	
LW	.016	.024	0.41	0.61	
r		.008		.203	
r1		.012		.305	
r2		.022		.559	

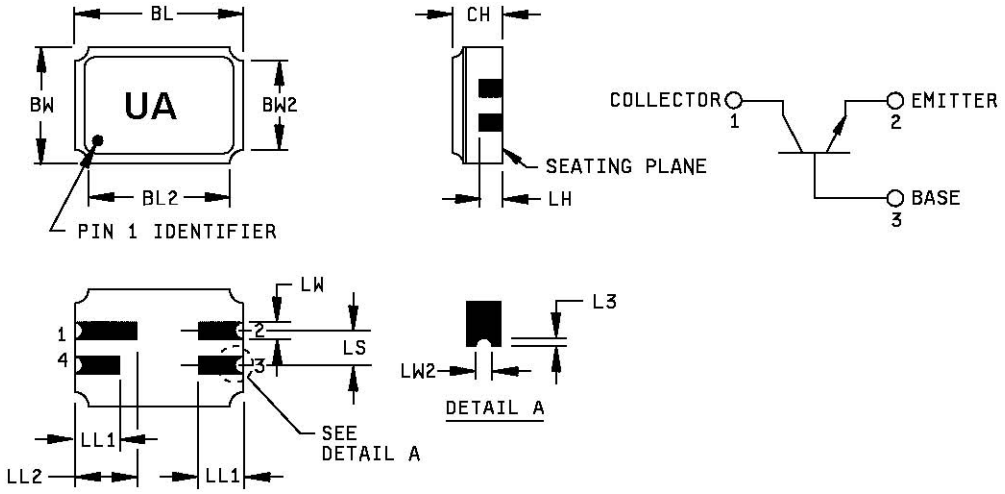
NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = connected to the lid braze ring.
5. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.

FIGURE 4. Physical dimensions, surface mount (UBC version, ceramic lid).

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Ltr.	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.215	.225	5.46	5.71
BL2		.225		5.71
BW	.145	.155	3.68	3.93
BW2		.155		3.93
CH	.061	.075	1.55	1.90
L3	.003	.007	0.08	0.18
LH	.029	.042	0.74	1.07
LL1	.032	.048	0.81	1.22
LL2	.072	.088	1.83	2.23
LS	.045	.055	1.14	1.39
LW	.022	.028	0.56	0.71
LW2	.006	.022	0.15	0.56

Pin number.	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

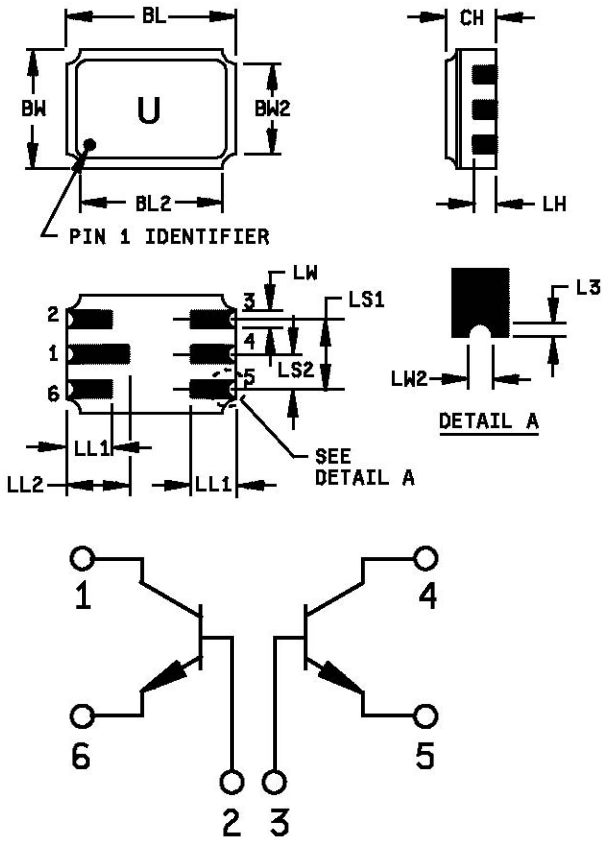
NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension CH controls the overall package thickness. When a window lid is used, dimension CH must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions LW2 minimum and L3 minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on the bottom two layers, optional on the top ceramic layer.) Dimension LW2 maximum and L3 maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.

FIGURE 5. Physical dimensions - surface mount (UA version).

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Ltr.	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.240	.250	6.10	6.35
BL2		.250		6.35
BW	.165	.175	4.19	4.44
BW2		.175		4.44
CH	.066	.080	1.68	2.03
L3	.003	.007	0.08	0.18
LH	.026	.039	0.66	0.99
LL1	.060	.070	1.52	1.78
LL2	.082	.098	2.08	2.49
LS1	.095	.105	2.41	2.67
LS2	.045	.055	1.14	1.39
LW	.022	.028	0.56	0.71
LW2	.006	.022	0.15	0.56

Pin number	1	2	3	4	5	6
Transistor	Collector no. 1	Base no. 1	Base no. 2	Collector no. 2	Emitter no. 2	Emitter no. 1

NOTES:

1. 1.Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension CH controls the overall package thickness. When a window lid is used, dimension CH must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions LW2 minimum and L3 minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on the bottom two layers, optional on the top ceramic layer.) Dimension LW2 maximum and L3 maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.

FIGURE 6. Physical dimensions - surface mount (dual transistors, U version only, 2N2369AU).