# 150V Low $I_Q$, Synchronous Step-Down DC/DC Controller

## FEATURES

- **Wide $V_{IN}$ Range: 4V to 140V (150V Abs Max)**
- **Wide Output Voltage Range: 0.8V to 60V**
- **Adjustable Gate Drive Level: 5V to 10V (OPTI-DRIVE)**
- **Low Operating $I_Q$: 40µA (Shutdown = 10µA)**
- **100% Duty Cycle Operation**
- **Integrated Bootstrap Diode**
- Selectable Gate Drive UVLO Thresholds
- Onboard LDO or External NMOS LDO for $DRV_{CC}$
- $EXTV_{CC}$ LDO Powers Drivers from $V_{OUT}$
- Phase-Lockable Frequency (75kHz to 850kHz)
- Programmable Fixed Frequency (50kHz to 900kHz)
- Selectable Continuous, Pulse-Skipping or Low Ripple Burst Mode® Operation at Light Loads
- Adjustable Burst Clamp
- Power Good Output Voltage Monitor
- Programmable Input Overvoltage Lockout
- Small 24-Lead 4mm × 5mm QFN or TSSOP Packages

## APPLICATIONS

- Automotive and Industrial Power Systems
- High Voltage Battery Operated Systems
- Telecommunications Power Systems

## DESCRIPTION

The LTC®7801 is a high performance step-down switching regulator DC/DC controller that drives an all N-channel synchronous power MOSFET stage that can operate from input voltages up to 140V. A constant frequency current mode architecture allows a phase-lockable frequency of up to 850kHz.

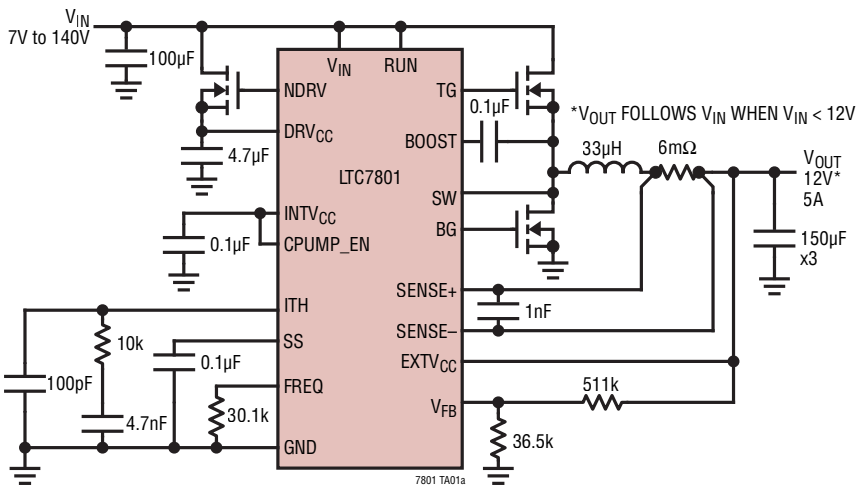
The gate drive voltage can be programmed from 5V to 10V to allow the use of logic or standard-level FETs to maximize efficiency. An integrated switch in the top gate driver eliminates the need for an external bootstrap diode. An internal charge pump allows for 100% duty cycle operation.

The low 40µA no-load quiescent current extends operating run time in battery-powered systems. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The LTC7801 features a precision 0.8V reference and power good output indicator. The output voltage can be programmed between 0.8V to 60V using external resistors.

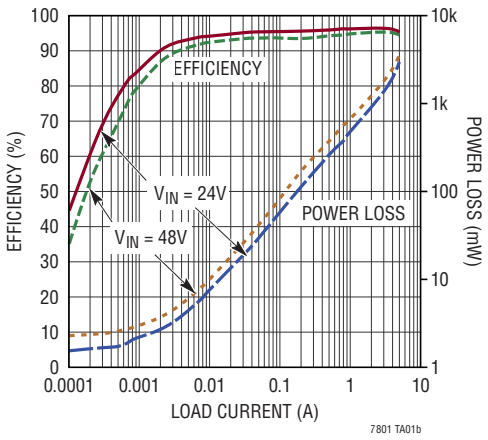
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## TYPICAL APPLICATION

**High Efficiency High Voltage 12V Output Step-Down Regulator**




**Efficiency and Power Loss vs Load Current**



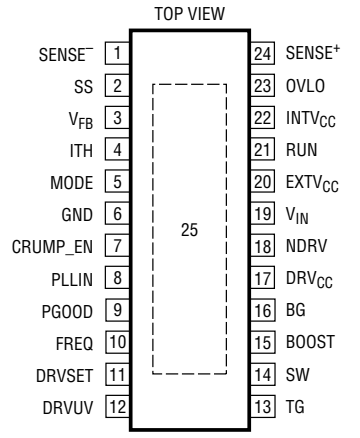

Rev. A

## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

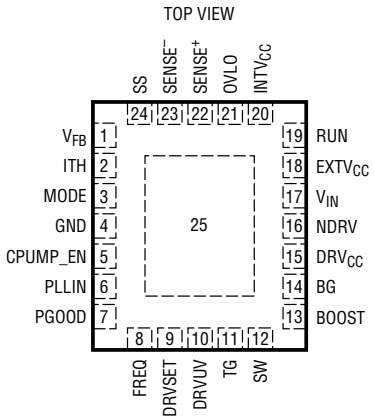
Input Supply Voltage ($V_{IN}$) ..... –0.3V to 150V
Top Side Driver Voltage BOOST ..... –0.3V to 150V
Switch Voltage (SW) ..... –5V to 150V
$DRV_{CC}$, (BOOST-SW) Voltages ..... –0.3V to 11V
BG, TG ..... (Note 8)
RUN Voltage ..... –0.3V to 150V
$SENSE^+$, $SENSE^-$ Voltages ..... –0.3V to 65V
PLLIN, PGOOD Voltages ..... –0.3V to 6V
MODE, DRVUV Voltages ..... –0.3V to 6V
FREQ Voltage ..... –0.3V to 6V
DRVSET, CPUMP_EN Voltages ..... –0.3V to 6V
NDRV ..... (Note 9)
$EXTV_{CC}$ Voltage ..... –0.3V to 14V
ITH, $V_{FB}$ Voltages ..... –0.3V to 6V
SS, OVLO Voltages ..... –0.3V to 6V
Operating Junction Temperature Range (Notes 2, 3)
LTC7801E, LTC7801I ..... –40°C to 125°C
LTC7801H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

## PIN CONFIGURATION




FE PACKAGE
24-LEAD PLASTIC TSSOP

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 33°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB FOR RATED ELECTRICAL AND THERMAL CHARACTERISTICS




UFD PACKAGE
24-LEAD (4mm × 5mm) PLASTIC QFN

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 43°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB FOR RATED ELECTRICAL AND THERMAL CHARACTERISTICS

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC7801EFE#PBF | LTC7801EFE#TRPBF | LTC7801FE | 24-Lead Plastic TSSOP | –40°C to 125°C |
| LTC7801IFE#PBF | LTC7801IFE#TRPBF | LTC7801FE | 24-Lead Plastic TSSOP | –40°C to 125°C |
| LTC7801HFE#PBF | LTC7801HFE#TRPBF | LTC7801FE | 24-Lead Plastic TSSOP | –40°C to 150°C |
| LTC7801EUFD#PBF | LTC7801EUFD#TRPBF | 7801 | 24-Lead (4mm × 5mm) Plastic QFN | –40°C to 125°C |
| LTC7801IUFD#PBF | LTC7801IUFD#TRPBF | 7801 | 24-Lead (4mm × 5mm) Plastic QFN | –40°C to 125°C |
| LTC7801HUFD#PBF | LTC7801HUFD#TRPBF | 7801 | 24-Lead (4mm × 5mm) Plastic QFN | –40°C to 150°C |

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Note 2), $V_{IN}$ = 12V, $V_{RUN}$ = 5V, $V_{EXTVCC}$ = 0V, $V_{DRVSET}$ = 0V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Supply Operating Voltage Range | (Note 10) DRVUV = 0V | ● | 4 | | 140 | V |
| $V_{OUT}$ | Regulated Output Voltage Set Point | | | 0.8 | | 60 | V |
| $V_{FB}$ | Regulated Feedback Voltage | (Note 4); ITH Voltage = 1.2V<br>0°C to 85°C | <br>● | <br>0.792<br>0.788 | <br>0.800<br>0.800 | <br>0.808<br>0.812 | <br>V<br>V |
| $I_{FB}$ | Feedback Current | (Note 4) | | | –0.006 | ±0.050 | µA |
| | Reference Voltage Line Regulation | (Note 4) $V_{IN}$ = 4.5V to 150V | | | 0.002 | 0.02 | %/V |
| | Output Voltage Load Regulation | (Note 4) Measured in Servo Loop,<br>ΔITH Voltage = 1.2V to 0.7V | ● | | 0.01 | 0.1 | % |
| | | (Note 4) Measured in Servo Loop,<br>ΔITH Voltage = 1.2V to 1.6V | ● | | –0.01 | –0.1 | % |
| $g_m$ | Transconductance Amplifier gm | (Note 4) ITH = 1.2V, Sink/Source 5µA | | | 2 | | mmho |
| $I_Q$ | Input DC Supply Current | (Note 5) $V_{DRVSET}$ = 0V | | | | | |
| | Pulse Skip or Forced Continuous Mode | $V_{FB}$ = 0.83V (No Load) | | | 2.5 | | mA |
| | Sleep Mode | $V_{FB}$ = 0.83V (No Load) | | | 40 | 55 | µA |
| | Shutdown | RUN = 0V | | | 10 | 20 | µA |
| UVLO | Undervoltage Lockout | $DRV_{CC}$ Ramping Up<br>DRVUV = 0V<br>DRVUV = $INTV_{CC}$, DRVSET = $INTV_{CC}$ | <br>●<br>● | <br><br> | <br>4.0<br>7.5 | <br>4.2<br>7.8 | <br>V<br>V |
| | | $DRV_{CC}$ Ramping Down<br>DRVUV = 0V<br>DRVUV = $INTV_{CC}$, DRVSET = $INTV_{CC}$ | <br>●<br>● | <br>3.6<br>6.4 | <br>3.8<br>6.7 | <br>4.0<br>7.0 | <br>V<br>V |
| $V_{RUN}$ ON | RUN Pin ON Threshold | $V_{RUN}$ Rising | ● | 1.1 | 1.2 | 1.3 | V |
| $V_{RUN}$ Hyst | RUN Pin Hysteresis | | | | 80 | | mV |
| OVLO | Overvoltage Lockout Threshold | $V_{OVLO}$ Rising | ● | 1.1 | 1.2 | 1.3 | V |
| OVLO Hyst | OVLO Hysteresis | | | | 100 | | mV |
| | OVLO Delay | | | | 1 | | µs |
| | Feedback Overvoltage Protection | Measured at $V_{FB}$, Relative to Regulated $V_{FB}$ | | 7 | 10 | 13 | % |
| $I_{SENSE+}$ | $SENSE^+$ Pin Current | | | | | ±1 | µA |
| $I_{SENSE–}$ | $SENSE^–$ Pin Current | $SENSE^–$ < $V_{INTVCC}$ – 0.5V<br>$SENSE^–$ > $V_{INTVCC}$ + 0.5V | | | <br>850 | ±1 | µA<br>µA |
| | Maximum Duty Factor | In Dropout<br>CPUMP_EN = 0V, FREQ = 0V<br>CPUMP_EN = $INTV_{CC}$ | | <br>98<br>100 | <br>99<br> | <br><br> | <br>% |
| $I_{SS}$ | Soft-Start Charge Current | $V_{SS}$ = 0V | | 8 | 10 | 12 | µA |
| $V_{SENSE(MAX)}$ | Maximum Current Sense Threshold | $V_{FB}$ = 0.7V, $V_{SENSE–}$ = 3.3V | ● | 66 | 75 | 84 | mV |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Note 2), $V_{IN}$ = 12V, $V_{RUN}$ = 5V, $V_{EXTVCC}$ = 0V, $V_{DRVSET}$ = 0V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Gate Driver** | | | | | | | |
| | TG Pull-up On-Resistance<br>TG Pull-down On-Resistance | $V_{DRVSET}$ = $INTV_{CC}$ | | | 2.2<br>1.0 | | Ω<br>Ω |
| | BG Pull-up On-Resistance<br>BG Pull-down On-Resistance | $V_{DRVSET}$ = $INTV_{CC}$ | | | 2.0<br>1.0 | | Ω<br>Ω |
| | BOOST to $DRV_{CC}$ Switch On-Resistance | $V_{SW}$ = 0V, $V_{DRVSET}$ = $INTV_{CC}$ | | | 11 | | Ω |
| | TG Transition Time:<br>Rise Time<br>Fall Time | (Note 6) $V_{DRVSET}$ = $INTV_{CC}$<br>$C_{LOAD}$ = 3300pF<br>$C_{LOAD}$ = 3300pF | | | <br>25<br>15 | | <br>ns<br>ns |
| | BG Transition Time:<br>Rise Time<br>Fall Time | (Note 6) $V_{DRVSET}$ = $INTV_{CC}$<br>$C_{LOAD}$ = 3300pF<br>$C_{LOAD}$ = 3300pF | | | <br>25<br>15 | | <br>ns<br>ns |
| | Top Gate Off to Bottom Gate On Delay<br>Synchronous Switch-On Delay Time | $C_{LOAD}$ = 3300pF each driver, $V_{DRVSET}$ = $INTV_{CC}$ | | | <br>55 | | <br>ns |
| | Bottom Gate Off to Top Gate On Delay<br>Top Switch-On Delay Time | $C_{LOAD}$ = 3300pF each driver, $V_{DRVSET}$ = $INTV_{CC}$ | | | <br>50 | | <br>ns |
| $t_{ON(MIN)}$ | TG Minimum On-Time | (Note 7) $V_{DRVSET}$ = $INTV_{CC}$ | | | 80 | | ns |
| **Charge Pump for High Side Driver Supply** | | | | | | | |
| $I_{CPUMP}$ | Charge Pump Output Current | $V_{BOOST}$ =16V, $V_{SW}$ = 12V, $V_{FREQ}$ = 0V<br>$V_{BOOST}$ =19V, $V_{SW}$ = 12V, $V_{FREQ}$ = 0V | | | 65<br>55 | | µA<br>µA |
| **$DRV_{CC}$ LDO Regulator** | | | | | | | |
| | $DRV_{CC}$ Voltage from NDRV LDO Regulator | NDRV Driving External NFET, $V_{EXTVCC}$ = 0V<br>7V < $V_{IN}$ < 150V, DRVSET = 0V<br>11V < $V_{IN}$ < 150V, DRVSET = $INTV_{CC}$ | | <br>5.8<br>9.6 | <br>6.0<br>10.0 | <br>6.2<br>10.4 | <br>V<br>V |
| | $DRV_{CC}$ Load Regulation from NDRV LDO Regulator | NDRV Driving External NFET<br>$I_{CC}$ = 0mA to 50mA, $V_{EXTVCC}$ = 0V | | | <br>0 | <br>1.0 | <br>% |
| | $DRV_{CC}$ Voltage from Internal $V_{IN}$ LDO | NDRV = $DRV_{CC}$, $V_{EXTVCC}$ = 0V<br>7V < $V_{IN}$ < 150V, DRVSET = 0V<br>11V < $V_{IN}$ < 150V, DRVSET = $INTV_{CC}$ | | <br>5.6<br>9.5 | <br>5.85<br>9.85 | <br>6.1<br>10.3 | <br>V<br>V |
| | $DRV_{CC}$ Load Regulation from $V_{IN}$ LDO | $I_{CC}$ = 0mA to 50mA, $V_{EXTVCC}$ = 0V<br>DRVSET = 0V<br>DRVSET = $INTV_{CC}$ | | | <br>1.4<br>0.9 | <br>2.5<br>2.0 | <br>%<br>% |
| | $DRV_{CC}$ Voltage from Internal $EXTV_{CC}$ LDO | 7V < $V_{EXTVCC}$ < 13V, DRVSET = 0V<br>11V < $V_{EXTVCC}$ < 13V, DRVSET = $INTV_{CC}$ | | 5.8<br>9.6 | 6.0<br>10.0 | 6.2<br>10.4 | V<br>V |
| | $DRV_{CC}$ Load Regulation from Internal $EXTV_{CC}$ LDO | $I_{CC}$ = 0mA to 50mA<br>DRVSET = 0V, $V_{EXTVCC}$ = 8.5V<br>DRVSET = $INTV_{CC}$, $V_{EXTVCC}$ = 13V | | | <br>0.7<br>0.5 | <br>2.0<br>2.0 | <br>%<br>% |
| | $EXTV_{CC}$ LDO Switchover Voltage | $EXTV_{CC}$ Ramping Positive<br>DRVUV = 0V<br>DRVUV = $INTV_{CC}$, DRVSET = $INTV_{CC}$ | | <br>4.5<br>7.4 | <br>4.7<br>7.7 | <br>4.9<br>8.0 | <br>V<br>V |
| | $EXTV_{CC}$ Hysteresis | | | | 250 | | mV |
| | Programmable $DRV_{CC}$ | $R_{DRVSET}$ = 50k<br>NDRV Driving External NFET, $V_{EXTVCC}$ = 0V | | | <br>5.0 | | <br>V |
| | Programmable $DRV_{CC}$ | $R_{DRVSET}$ = 70k<br>NDRV Driving External NFET, $V_{EXTVCC}$ = 0V | | 6.4 | 7.0 | 7.6 | V |
| | Programmable $DRV_{CC}$ | $R_{DRVSET}$ = 90k<br>NDRV Driving External NFET, $V_{EXTVCC}$ = 0V | | | 9.0 | | V |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Note 2), $V_{IN}$ = 12V, $V_{RUN}$ = 5V, $V_{EXTVCC}$ = 0V, $V_{DRVSET}$ = 0V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **$INTV_{CC}$ LDO Regulator** | | | | | | | |
| $V_{INTVCC}$ | $INTV_{CC}$ Voltage | $I_{CC}$ = 0mA to 2mA | | 4.7 | 5.0 | 5.2 | V |
| **Oscillator and Phase-Locked Loop** | | | | | | | |
| | Programmable Frequency | $R_{FREQ}$ = 25k, PLLIN = DC Voltage | | | 105 | | kHz |
| | Programmable Frequency | $R_{FREQ}$ = 65k, PLLIN = DC Voltage | | 375 | 440 | 505 | kHz |
| | Programmable Frequency | $R_{FREQ}$ =105k, PLLIN = DC Voltage | | | 835 | | kHz |
| | Low Fixed Frequency | $V_{FREQ}$ = 0V, PLLIN = DC Voltage | | 320 | 350 | 380 | kHz |
| | High Fixed Frequency | $V_{FREQ}$ = $INTV_{CC}$, PLLIN = DC Voltage | | 485 | 535 | 585 | kHz |
| $f_{SYNC}$ | Synchronizable Frequency | PLLIN = External Clock | ● | 75 | | 850 | kHz |
| | PLLIN Input High Level<br>PLLIN Input Low Level | PLLIN = External Clock<br>PLLIN = External Clock | ●<br>● | 2.8 | | <br>0.5 | V<br>V |
| **PGOOD Output** | | | | | | | |
| $V_{PGL}$ | PGOOD Voltage Low | $I_{PGOOD}$ = 2mA | | | 0.02 | 0.04 | V |
| $I_{PGOOD}$ | PGOOD Leakage Current | $V_{PGOOD}$ = 3.3V | | | | 10 | µA |
| | PGOOD Trip Level | $V_{FB}$ with Respect to Set Regulated Voltage<br>$V_{FB}$ Ramping Negative<br>Hysteresis | | <br>–13 | <br>–10<br>2.5 | <br>–7 | <br>%<br>% |
| | | $V_{FB}$ with Respect to Set Regulated Voltage<br>$V_{FB}$ Ramping Positive<br>Hysteresis | | <br>7 | <br>10<br>2.5 | <br>13 | <br>%<br>% |
| | Delay for Reporting a Fault | | | | 40 | | µs |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Ratings for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC7801 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7801E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7801I is guaranteed over the –40°C to 125°C operating junction temperature range and the LTC7801H is guaranteed over the –40°C to 150°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. High temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125ºC. The junction temperature ($T_J$, in °C) is calculated from the ambient temperature ($T_A$, in °C) and power dissipation ($P_D$, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where $\theta_{JA}$ = 33°C/W for the TSSOP package and $\theta_{JA}$ = 43°C/W for the QFN package.

**Note 3:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

**Note 4:** The LTC7801 is tested in a feedback loop that servos $V_{ITH}$ to a specified voltage and measures the resultant $V_{FB}$. The specification at 85°C is not tested in production and is assured by design, characterization and correlation to production testing at other temperatures (125°C for the LTC7801E and LTC7801I, 150°C for the LTC7801H). For the LTC7801I and LTC7801H, the specification at 0°C is not tested in production and is assured by design, characterization and correlation to production testing at –40°C.

**Note 5:** Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications Information section.

**Note 6:** Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

**Note 7:** The minimum on-time condition is specified for an inductor peak-to-peak ripple current >40% of $I_{MAX}$ (See Minimum On-Time Considerations in the Applications Information section).

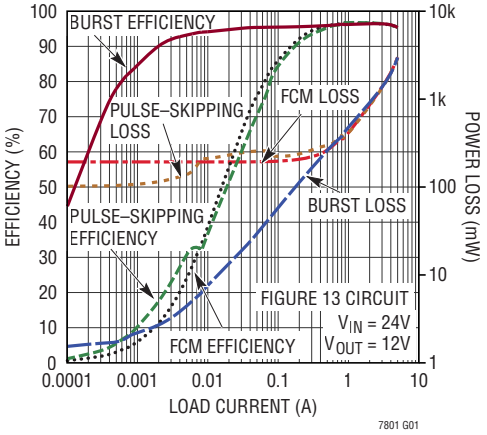
**Note 8:** Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

**Note 9:** Do not apply a voltage or current source to the NDRV pin, other than tying NDRV to $DRV_{CC}$ when not used. If used it must be connected to capacitive loads only (see $DRV_{CC}$ Regulators in the Applications Information section), otherwise permanent damage may occur.

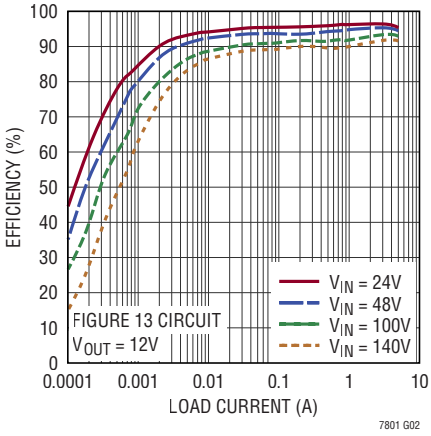
**Note 10:** The minimum input supply operating range is dependent on the $DRV_{CC}$ UVLO thresholds as determined by the DRVUV pin setting.

# TYPICAL PERFORMANCE CHARACTERISTICS

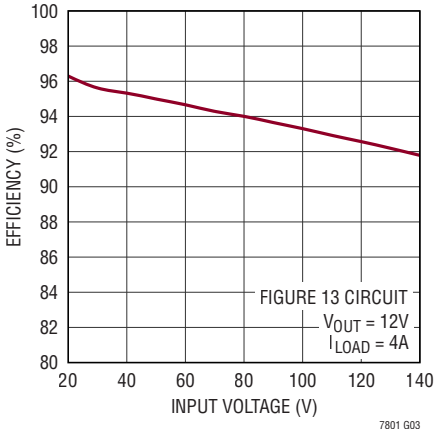
### Efficiency and Power Loss vs Load Current



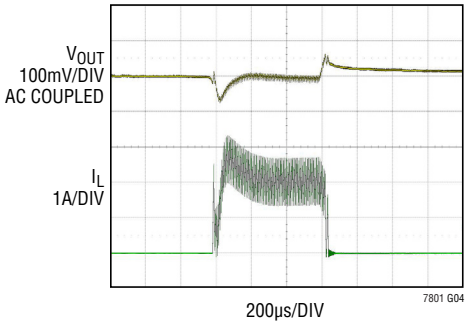

### Efficiency vs Load Current




### Efficiency vs Input Voltage

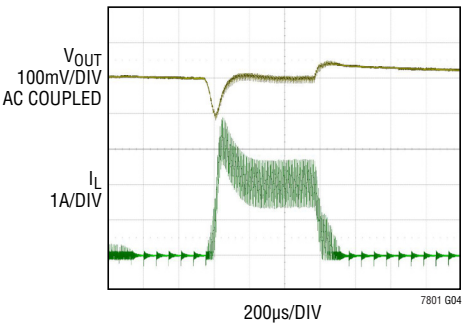



### Load Step Burst Mode Operation



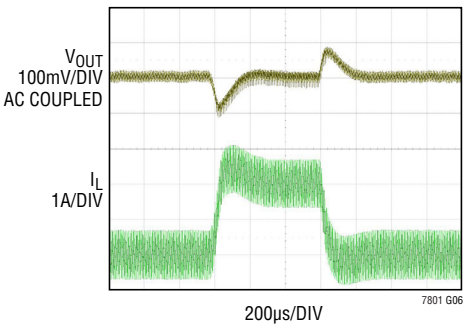

VIN = 24V
FIGURE 13 CIRCUIT

### Load Step Pulse-Skipping Mode



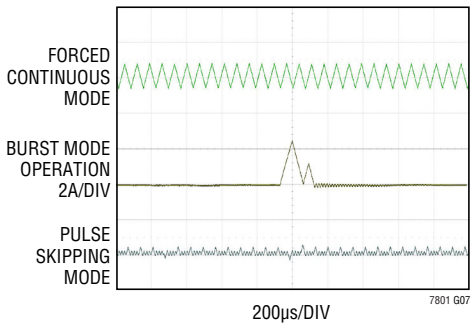

VIN = 24V
FIGURE 13 CIRCUIT

### Load Step Forced Continuous Mode



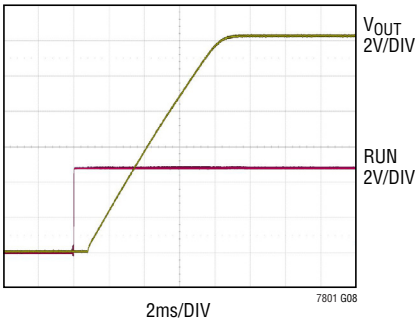

VIN = 24V
FIGURE 13 CIRCUIT

### Inductor Current at Light Load



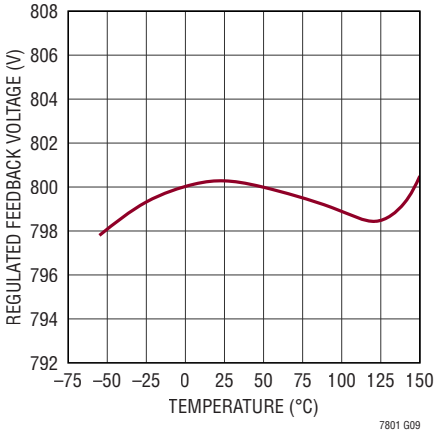

VIN = 24V
FIGURE 13 CIRCUIT

### Soft Start-Up



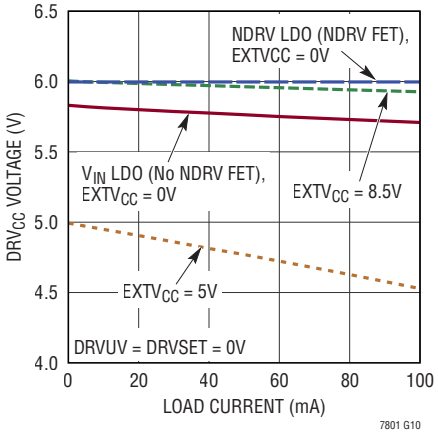

VIN = 24V
FIGURE 13 CIRCUIT

### Regulated Feedback Voltage vs Temperature

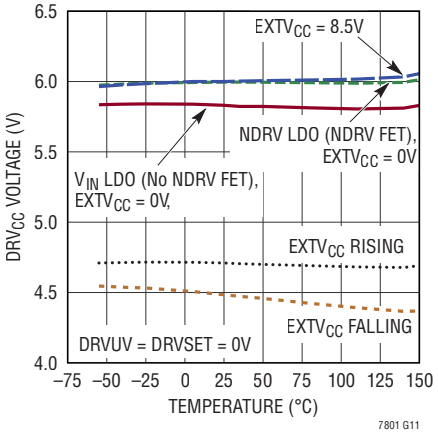


# TYPICAL PERFORMANCE CHARACTERISTICS

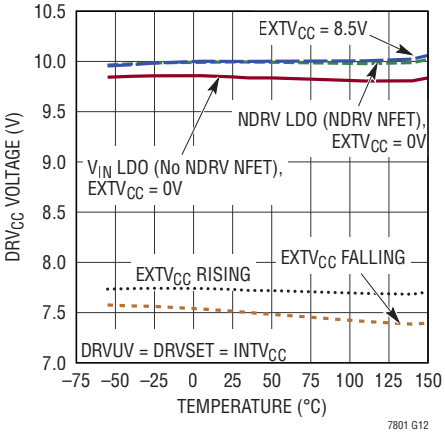
### $DRV_{CC}$ and $EXTV_{CC}$ vs Load Current



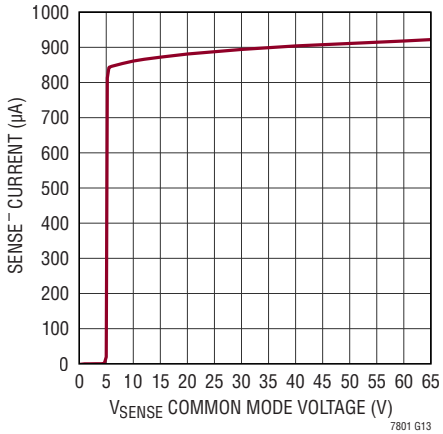

### $EXTV_{CC}$ Switchover and $DRV_{CC}$ Voltages vs Temperature



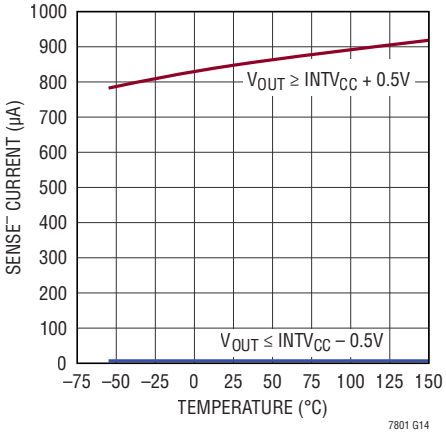

### $EXTV_{CC}$ Switchover and $DRV_{CC}$ Voltages vs Temperature



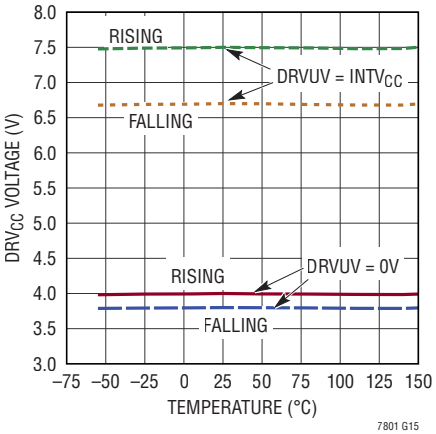

### $SENSE^-$ Pin Input Current vs $V_{SENSE}$ Voltage



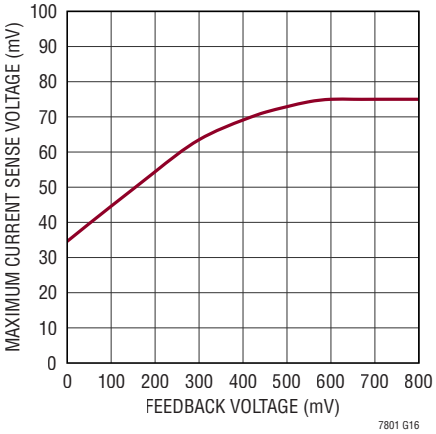

### $SENSE^-$ Pin Input Bias Current vs Temperature



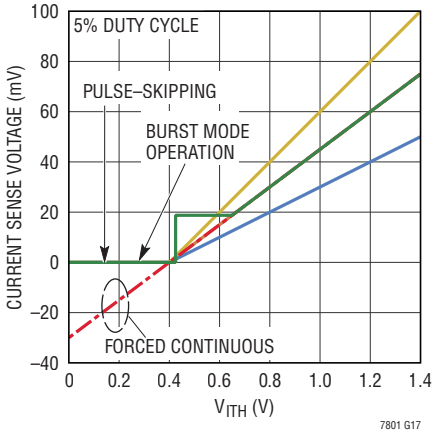

### Undervoltage Lockout Threshold vs Temperature



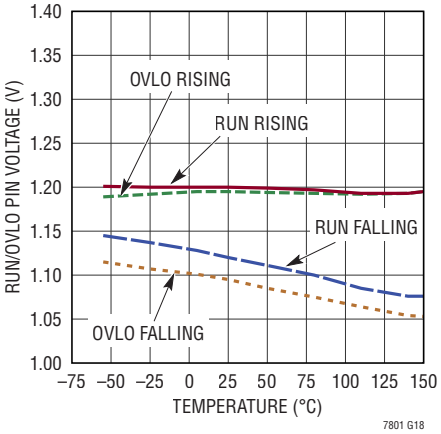

### Foldback Current Limit




### Maximum Current Sense Threshold vs ITH Voltage

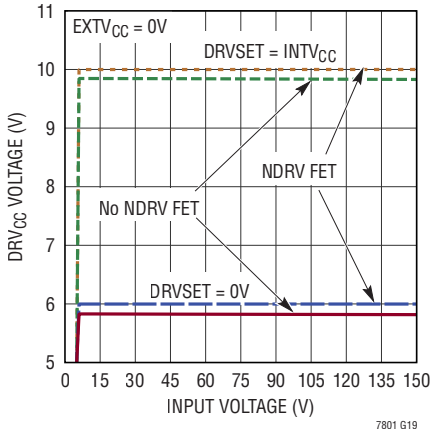



### RUN/OVLO Threshold vs Temperature

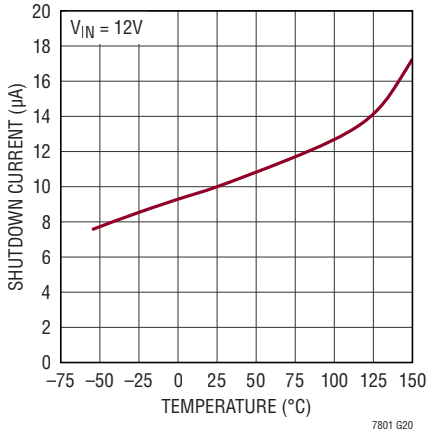


# TYPICAL PERFORMANCE CHARACTERISTICS

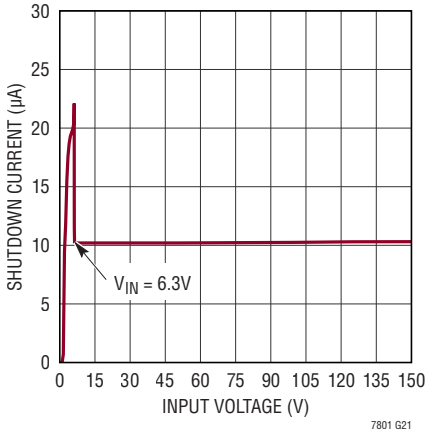
### $DRV_{CC}$ Line Regulation



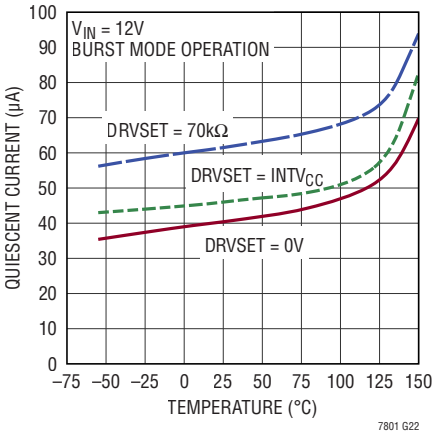

### Shutdown Current vs Temperature



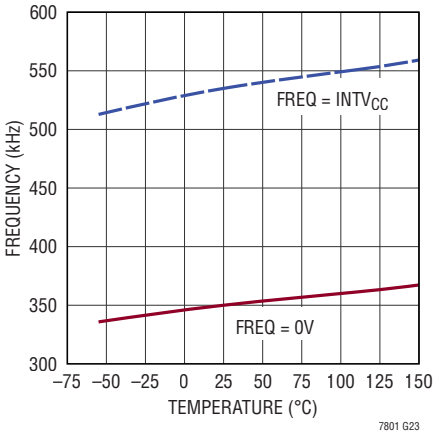

### Shutdown Current vs Input Voltage



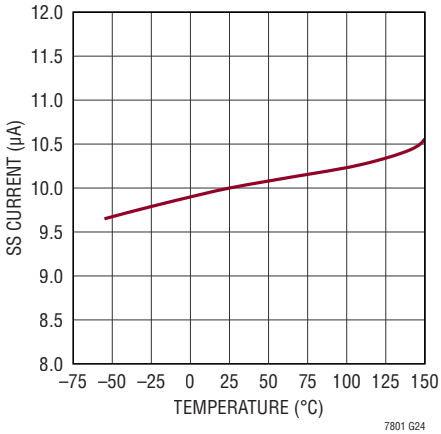

### Quiescent Current vs Temperature



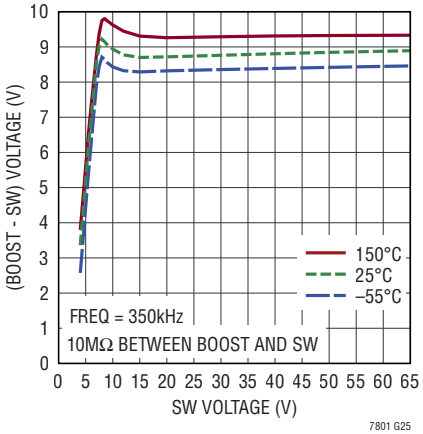

### Oscillator Frequency vs Temperature



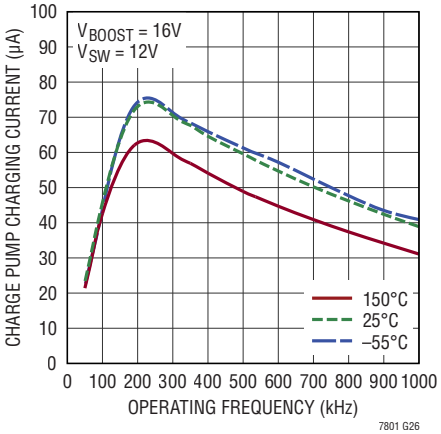

### SS Pull-Up Current vs Temperature



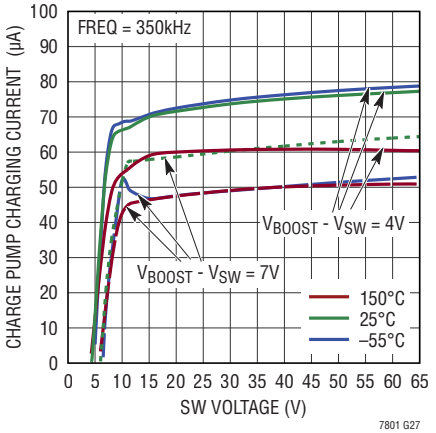

### Boost Charge Pump Voltage vs SW Voltage




### BOOST Charge Pump Charging Current vs Frequency




### BOOST Charge Pump Charging Current vs SW Voltage



## PIN FUNCTIONS (QFN/TSSOP)

**$V_{FB}$ (Pin 1/Pin 3):** Feedback Input. This pin receives the remotely sensed feedback voltage from an external resistor divider across the output.

**ITH (Pin 2/Pin 4):** Error Amplifier Output and Switching Regulator Compensation Point. The current comparator trip point increases with this control voltage.

**MODE (Pin 3/Pin 5):** Mode Select and Burst Clamp Adjust Input. This input determines how the LTC7801 operates at light loads. Pulling this pin to ground selects Burst Mode operation with the burst clamp level defaulting to 25% of $V_{SENSE(MAX)}$. Tying this pin to a voltage between 0.5V and 1.0V selects Burst Mode operation and adjusts the burst clamp between 10% and 60%. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to a voltage greater than 1.4V and less than $INTV_{CC}$ – 1.3V selects pulse-skipping operation.

**GND (Pin 4, Exposed Pin 25/Pin 6, Exposed Pad Pin 25):** Ground. All GND pins must be tied together for operation. The exposed pad must be soldered to PCB ground for rated electrical and thermal performance.

**CPUMP_EN (Pin 5/Pin 7):** Charge Pump Enable Pin for the Top Gate Driver Boost Supply. Tying this pin to $INTV_{CC}$ enables the boost supply charge pump and allows for 100% duty cycle operation in dropout. Tying this pin to GND disables the charge pump and enables boost refresh, allowing for 99% duty cycle operation in dropout. Do not float this pin.

**PLLIN (Pin 6/ Pin 8):** External Synchronization Input to Phase Detector. When an external clock is applied to this pin, the phase-locked loop will force the rising TG signal to be synchronized with the rising edge of the external clock. If the MODE pin is set to Forced Continuous Mode or Burst Mode operation, then the regulator operates in Forced Continuous Mode when synchronized. If the MODE pin is set to pulse-skipping mode, then the regulator operates in pulse-skipping mode when synchronized.

**PGOOD (Pin 7/Pin 9):** Open-Drain Logic Output. PGOOD is pulled to ground when the voltage on the $V_{FB}$ pin is not within ±10% of its set point.

**FREQ (Pin 8/Pin 10):** Frequency Control Pin for the Internal VCO. Connecting the pin to GND forces the VCO to a fixed low frequency of 350kHz. Connecting the pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 535kHz. Other frequencies between 50kHz and 900kHz can be programmed by using a resistor between FREQ and GND. An internal 20µA pull-up current develops the voltage to be used by the VCO to control the frequency.

**DRVSET (Pin 9/Pin 11):** $DRV_{CC}$ Regulation Program Pin. This pin sets the regulated output voltage of the $DRV_{CC}$ linear regulator. Tying this pin to GND sets $DRV_{CC}$ to 6.0V. Tying this pin to $INTV_{CC}$ sets $DRV_{CC}$ to 10V. Other voltages between 5V and 10V can be programmed by placing a resistor (50k to 100k) between the DRVSET pin and GND. An internal 20µA pull-up current develops the voltage to be used as the reference to the $DRV_{CC}$ LDO. See PC Board Layout Checklist in the Applications Information section for additional considerations when using higher DRVSET settings.

**DRVUV (Pin 10/Pin 12):** $DRV_{CC}$ UVLO Program Pin. This pin determines the higher or lower $DRV_{CC}$ UVLO and $EXTV_{CC}$ switchover thresholds, as listed on the Electrical Characteristics table. Connecting DRVUV to GND chooses the lower thresholds whereas tying DRVUV to $INTV_{CC}$ chooses the higher thresholds. Do not float this pin.

**TG (Pin 11/Pin 13):** High Current Gate Drives for Top N-Channel MOSFET. This is the output of floating high side driver with a voltage swing equal to $DRV_{CC}$ superimposed on the switch node voltage SW.

**SW (Pin 12/Pin 14):** Switch Node Connection to Inductor.

**BOOST (Pin 13/Pin 15):** Bootstrapped Supply to the Topside Floating Driver. A capacitor is connected between the BOOST and SW pins. Voltage swing at the BOOST pin is from approximately $DRV_{CC}$ to ($V_{IN}$ + $DRV_{CC}$).

**BG (Pin 14/Pin 16):** High Current Gate Drive for Bottom (Synchronous) N-Channel MOSFET. Voltage swing at this pin is from ground to $DRV_{CC}$.

## PIN FUNCTIONS (QFN/TSSOP)

**$DRV_{CC}$ (Pin 15/Pin 17):** Output of the Internal or External Low Dropout Regulators. The gate drivers are powered from this voltage source. The $DRV_{CC}$ voltage is set by the DRVSET pin. Must be decoupled to ground with a minimum of 4.7µF ceramic or other low ESR capacitor, as close as possible to the IC. Do not use the $DRV_{CC}$ pin for any other purpose.

**NDRV (Pin 16/Pin 18):** Drive Output for External Pass Device of the NDRV LDO Linear Regulator for $DRV_{CC}$. Connect this pin to the gate of an external NMOS pass device. An internal charge pump allows NDRV to regulate above $V_{IN}$ for low dropout performance. To disable this external NDRV LDO, tie NDRV to $DRV_{CC}$.

**$V_{IN}$ (Pin 17/Pin 19):** Main Supply Pin. A bypass capacitor should be tied between this pin and the GND pins.

**$EXTV_{CC}$ (Pin 18/Pin 20):** External Power Input to an Internal LDO linear regulator Connected to $DRV_{CC}$. This LDO supplies $DRV_{CC}$ power from $EXTV_{CC}$, bypassing the internal LDO powered from $V_{IN}$ or the external NDRV LDO whenever $EXTV_{CC}$ is higher than its switchover threshold (4.7V or 7.7V depending on the DRVUV pin). See $DRV_{CC}$ Regulators in the Applications Information section. Do not exceed 14V on this pin. Do not connect $EXTV_{CC}$ to a voltage greater than $V_{IN}$. If not used, connect to GND and place a 330k or smaller resistor between $INTV_{CC}$ and SS.

**RUN (Pin 19/Pin 21):** Run Control Input. Forcing this pin below 1.12V shuts down the controller. Forcing this pin below 0.7V shuts down the entire LTC7801, reducing quiescent current to approximately 10µA. This pin can be tied to $V_{IN}$ for always-on operation. Do not float this pin.

**$INTV_{CC}$ (Pin 20/Pin 22):** Output of the Internal 5V Low Dropout Regulator. Many of the low voltage analog and digital circuits are powered from this voltage source. A low ESR 0.1µF ceramic bypass capacitor should be connected between $INTV_{CC}$ and GND, as close as possible to the LTC7801.

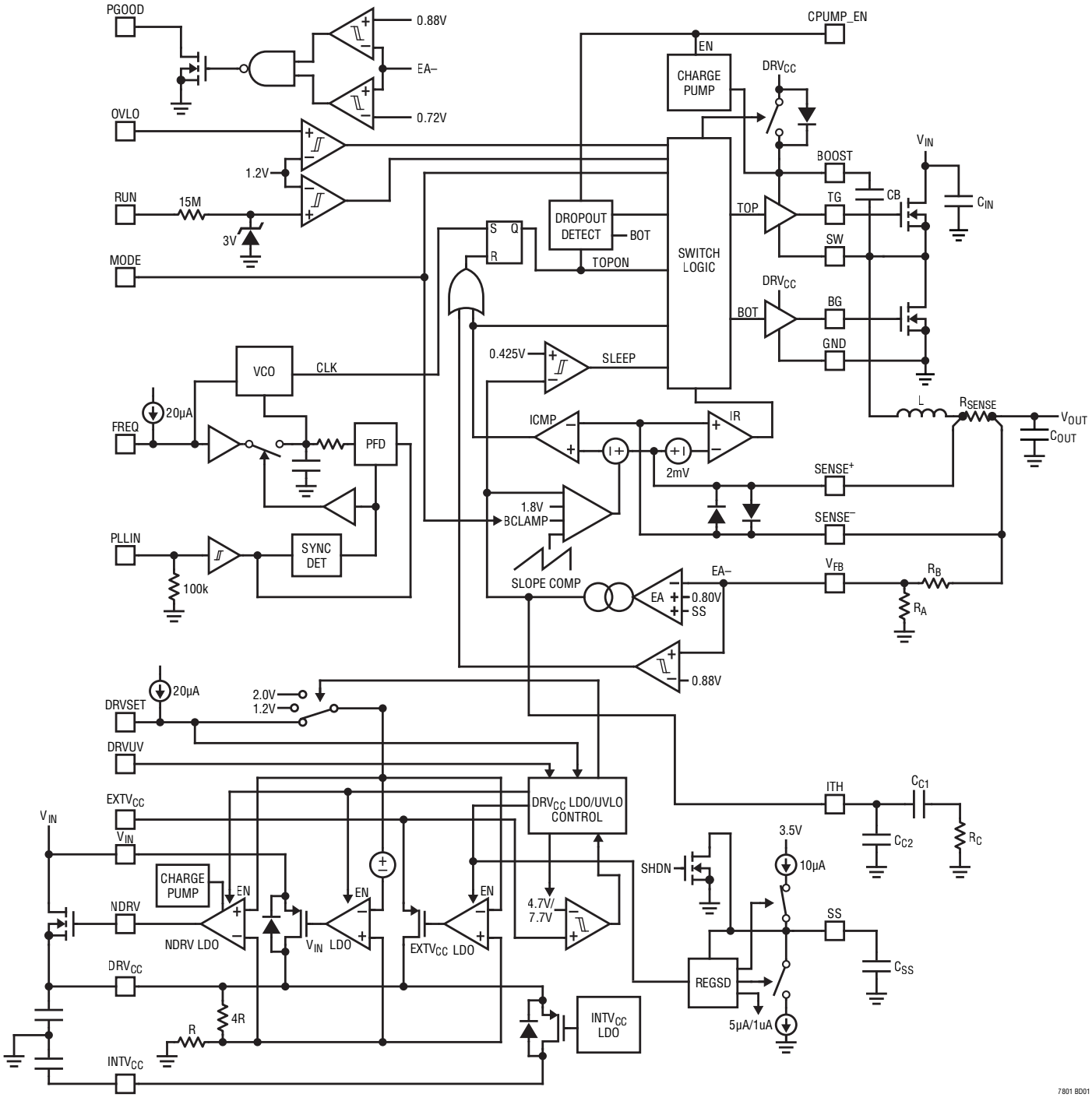
**OVLO (Pin 21/Pin 23):** Overvoltage Lockout Input. A voltage on this pin above 1.2V disables switching of the controller. The $DRV_{CC}$ and $INTV_{CC}$ supplies maintain regulation during an OVLO event. Exceeding the OVLO threshold triggers a soft-start reset. If the OVLO function is not used, connect this pin to GND.

**$SENSE^+$ (Pin 22/Pin 24):** The (+) Input to the Differential Current Comparator. The ITH pin voltage and controlled offsets between the $SENSE^-$ and $SENSE^+$ pins in conjunction with $R_{SENSE}$ set the current trip threshold.

**$SENSE^-$ (Pin 23/Pin 1):** The (–) Input to the Differential Current Comparator. When $SENSE^-$ is greater than $INTV_{CC}$, the $SENSE^-$ pin supplies power to the current comparator.

**SS (Pin 24/Pin 2):** Soft-Start Input. The LTC7801 regulates the $V_{FB}$ voltage to the smaller of 0.8V or the voltage on the SS pin. An internal 10µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to final regulated output voltage. The SS pin is also used for the Regulator Shutdown (REGSD) feature. A 5µA/1µA pull-down current can be connected on SS depending on the state of the $EXTV_{CC}$ LDO and the voltage on SS. See Regulator Shutdown in the Operation section for more information. To defeat the REGSD feature, place a 330k or smaller resistor between $INTV_{CC}$ and SS. See Soft-Start Pin in the Applications Information section for more information on defeating REGSD.

# FUNCTIONAL DIAGRAM



## OPERATION

### Main Control Loop

The LTC7801 uses a constant frequency, current mode step-down architecture. During normal operation, the external top MOSFET is turned on when the clock sets the $R_S$ latch, and is turned off when the main current comparator, ICMP, resets the $R_S$ latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier compares the output voltage feedback signal at the $V_{FB}$ pin (which is generated with an external resistor divider connected across the output voltage, $V_{OUT}$, to ground) to the internal 0.800V reference voltage. When the load current increases, it causes a slight decrease in $V_{FB}$ relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current.

After the top MOSFET is turned off each cycle, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current comparator IR, or the beginning of the next clock cycle.

### $DRV_{CC}/EXTV_{CC}/INTV_{CC}$ Power

Power for the top and bottom MOSFET drivers is derived from the $DRV_{CC}$ pin. The $DRV_{CC}$ supply voltage can be programmed from 5V to 10V by setting the DRVSET pin. Two separate LDOs (low dropout linear regulators) can provide power from $V_{IN}$ to $DRV_{CC}$. The internal $V_{IN}$ LDO uses an internal P-channel pass device between the $V_{IN}$ and $DRV_{CC}$ pins. To prevent high on-chip power dissipation in high input voltage applications, the LTC7801 also includes an NDRV LDO that utilizes the NDRV pin to supply power to $DRV_{CC}$ by driving the gate of an external N-channel MOSFET acting as a linear regulator with its source connected to $DRV_{CC}$ and drain connected to $V_{IN}$. The NDRV LDO includes an internal charge pump that allows NDRV to be driven above $V_{IN}$ for low dropout performance.

When the $EXTV_{CC}$ pin is tied to a voltage below its switchover voltage (4.7V or 7.7V depending on the DRVUV pin), the $V_{IN}$ and NDRV LDOs are enabled and one of them supplies power from $V_{IN}$ to $DRV_{CC}$. The $V_{IN}$ LDO has a slightly lower regulation point than the NDRV LDO. If the NDRV LDO is being used with an external N-channel MOSFET, the gate of the MOSFET tied to the NDRV pin is driven such that $DRV_{CC}$ regulates above the $V_{IN}$ LDO regulation point, causing all $DRV_{CC}$ current to flow through the external N-channel MOSFET, bypassing the internal $V_{IN}$ LDO pass device. If the NDRV LDO is not being used, all $DRV_{CC}$ current flows through the internal P-channel pass device between the $V_{IN}$ and $DRV_{CC}$ pins.

If $EXTV_{CC}$ is taken above its switchover voltage, the $V_{IN}$ and NDRV LDOs are turned off and an $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies power from $EXTV_{CC}$ to $DRV_{CC}$. Using the $EXTV_{CC}$ pin allows the $DRV_{CC}$ power to be derived from a high efficiency external source such as the LTC7801 switching regulator output.

The $INTV_{CC}$ supply powers most of the other internal circuits in the LTC7801. The $INTV_{CC}$ LDO regulates to a fixed value of 5V and its power is derived from the $DRV_{CC}$ supply.

### Top MOSFET Driver and Charge Pump (CPUMP_EN Pin)

The top MOSFET driver is biased from the floating bootstrap capacitor, $C_B$, which normally recharges during each cycle through an internal switch whenever SW goes low.

If the input voltage decreases to a voltage close to its output, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The LTC7801 includes an internal charge pump that allows the top MOSFET to be turned on continuously at 100% duty cycle. This charge pump delivers current to $C_B$ and is enabled when the CPUMP_EN pin is tied to $INTV_{CC}$. Tying CPUMP_EN to GND disables the charge pump and causes the dropout detector to force the top MOSFET off for about one twelfth of the clock period every tenth cycle to allow $C_B$ to recharge, resulting in an effective 99% max duty cycle.

### Shutdown and Start-Up (RUN, SS Pins)

The LTC7801 can be shut down using the RUN pin. Connecting the RUN pin below 1.12V shuts down the main control loop. Connecting the RUN pin below 0.7V disables the controller and most internal circuits, including the $DRV_{CC}$ and $INTV_{CC}$ LDOs. In this state, the LTC7801 draws only 10µA of quiescent current.

## OPERATION

The RUN pin has no internal pull-up current, so the pin must be externally pulled up or driven directly by logic. The RUN pin can tolerate up to 150V (absolute maximum), so it can be conveniently tied to $V_{IN}$ in always-on applications where the controller is enabled continuously and never shut down.

The start-up of the controller's output voltage $V_{OUT}$ is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 0.8V internal reference, the LTC7801 regulates the $V_{FB}$ voltage to the SS pin voltage instead of the 0.8V reference. This allows the SS pin to be used to program a soft-start by connecting an external capacitor from the SS pin to GND. An internal 10µA pull-up current charges this capacitor creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 0.8V (and beyond), the output voltage $V_{OUT}$ rises smoothly from zero to its final value.

### Light Load Current Operation (Burst Mode Operation, Pulse-Skipping or Forced Continuous Mode) (MODE Pin)

The LTC7801 can be enabled to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode, or forced continuous conduction mode at light load currents. To select Burst Mode operation, tie the MODE pin to GND or a voltage between 0.5V and 1.0V. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to a DC voltage greater than 1.4V and less than $INTV_{CC}$ – 1.3V. This can be done with a simple resistor divider off $INTV_{CC}$, with both resistors being 100k.

When the controller is enabled for Burst Mode operation, the minimum peak current in the inductor (burst clamp) is adjustable and can be programmed by the voltage on the MODE pin. Tying the MODE pin to GND sets the default burst clamp to approximately 25% of the maximum sense voltage even when the voltage on the ITH pin indicates a lower value. A voltage between 0.5V and 1.0V on the MODE pin programs the burst clamp linearly between 10% and 60% of the maximum sense voltage.

In Burst Mode operation, if the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off. The ITH pin is then disconnected from the output of the EA and parked at 0.450V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC7801 draws to only 40µA. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (IR) turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates discontinuously.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current.

When the MODE pin is connected for pulse-skipping mode, the LTC7801 operates in PWM pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator, ICMP, may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation,

## OPERATION

exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation. At high output voltages, the efficiency in pulse-skipping mode is comparable to force continuous mode.

If the PLLIN pin is clocked by an external clock source to use the phase-locked loop, see Frequency Selection and Phase-Locked Loop (FREQ and PLLIN Pins) section, then the LTC7801 operates in forced continuous operation when the MODE pin is set to forced continuous or Burst Mode operation. The controller operates in pulse-skipping mode when clocked by an external clock source with the MODE pin set to pulse-skipping mode.

### Frequency Selection and Phase-Locked Loop (FREQ and PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC7801 can be selected using the FREQ pin.

If the PLLIN pin is not being driven by an external clock source, the FREQ pin can be tied to GND, tied to $INTV_{CC}$ or programmed through an external resistor. Tying FREQ to GND selects 350kHz while tying FREQ to $INTV_{CC}$ selects 535kHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 50kHz and 900kHz, as shown in Figure 12.

A phase-locked loop (PLL) is available on the LTC7801 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN pin. The LTC7801's phase detector adjusts the voltage (through an internal lowpass filter) of the VCO input to align the turn-on of the external top MOSFET to the rising edge of the synchronizing signal.

The VCO input voltage is prebiased to the operating frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the rising edge of TG. The ability to prebias the loop filter allows the PLL to lock-in rapidly without deviating far from the desired frequency.

The typical capture range of the LTC7801's phase-locked loop is from approximately 55kHz to 1MHz, with a guarantee to be between 75kHz and 850kHz. In other words, the LTC7801's PLL is guaranteed to lock to an external clock source whose frequency is between 75kHz and 850kHz. It is recommended that the external clock source swing from ground (0V) to at least 2.8V.

### Input Supply Overvoltage Lockout (OVLO Pin)

The LTC7801 implements a protection feature that inhibits switching when the input voltage rises above a programmable operating range. By using a resistor divider from the input supply to ground, the OVLO pin serves as a precise input supply voltage monitor. Switching is disabled when the OVLO pin rises above 1.2V, which can be configured to limit switching to a specific range of input supply voltage.

When switching is disabled, the LTC7801 can safely sustain input voltages up to the absolute maximum rating of 150V. Input supply overvoltage events trigger a soft-start reset, which results in a graceful recovery from an input supply transient.

### Output Overvoltage Protection

An overvoltage comparator guards against transient overshoots as well as other more serious conditions that may overvoltage the output. When the $V_{FB}$ pin rises by more than 10% above its regulation point of 0.800V, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

# OPERATION

### Power Good Pin

The PGOOD pin is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the $V_{FB}$ pin voltage is not within ±10% of the 0.8V reference voltage. The PGOOD pin is also pulled low when the RUN pin is low (shut down). When the $V_{FB}$ pin voltage is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source no greater than 6V.

### Foldback Current

When the output voltage falls to less than 70% of its nominal level, foldback current limiting is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft-start interval (as long as the $V_{FB}$ voltage is keeping up with the SS voltage). Foldback current limiting is intended to limit power dissipation during overcurrent and short-circuit fault conditions. Note that the LTC7801 continuously monitors the inductor current and prevents current runaway under all conditions.

### Regulator Shutdown (REGSD)

High input voltage applications typically require using the $EXTV_{CC}$ LDO to keep power dissipation low. Fault conditions where the $EXTV_{CC}$ LDO becomes disabled ($EXTV_{CC}$ below the switchover threshold) for an extended period of time could result in overheating of the IC (or overheating the external N-channel MOSFET if the NDRV LDO is used). In the cases where $EXTV_{CC}$ is tied to the regulator output, this event could happen during overload conditions such as an output short to ground. The LTC7801 includes a regulator shutdown (REGSD) feature that shuts down the regulator to substantially reduce power dissipation and the risk of overheating during such events.

The REGSD circuit monitors the $EXTV_{CC}$ LDO and the SS pin to determine when to shut down the regulator. Refer to the timing diagram in Figure 1. Whenever SS is above 2.2V *and* the $EXTV_{CC}$ LDO is not switched over (the $EXTV_{CC}$ pin is below the switchover threshold), the internal 10µA pull-up current on SS turns off and a 5µA pull-down current turns on, discharging SS. Once SS discharges to 2.0V *and* the $EXTV_{CC}$ pin remains below the $EXTV_{CC}$ switchover threshold, the pull-down current reduces to 1µA and the regulator shuts down, eliminating all $DRV_{CC}$ switching current. Switching stays off until the SS pin discharges to approximately 200mV, at which point the 10µA pull-up current turns back on and the regulator re-enables switching. If the short-circuit persists, the regulator cycles on and off at a low duty cycle interval of about 12%.

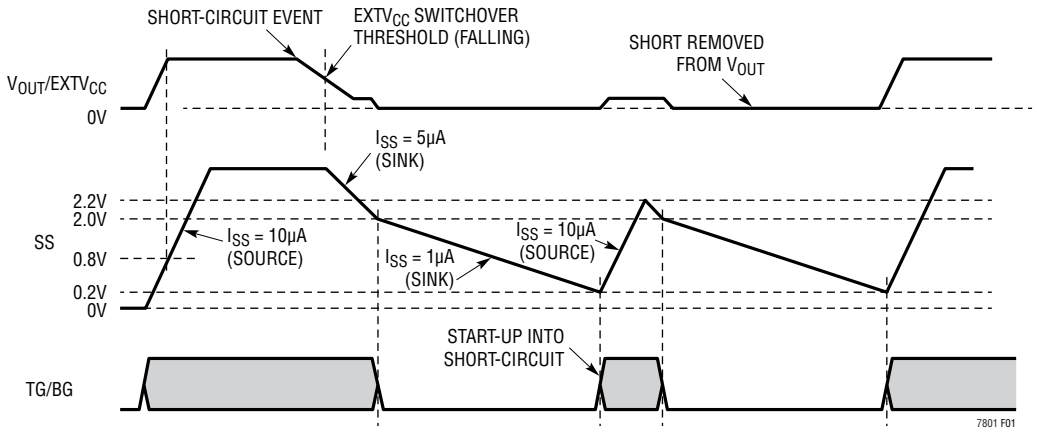



**Figure 1. Regulator Shutdown Operation**

## APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC7801 application circuit. LTC7801 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of $R_{SENSE}$ (if $R_{SENSE}$ is used) and inductor value. Next, the power MOSFETs are selected. Finally, input and output capacitors are selected.

### SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are the inputs to the current comparator. The common mode voltage range on these pins is 0V to 65V (absolute maximum), enabling the LTC7801 to regulate output voltages up to a nominal set point of 60V (allowing margin for tolerances and transients). The SENSE+ pin is high impedance over the full common mode range, drawing at most ±1µA. This high impedance allows the current comparators to be used in inductor DCR sensing. The impedance of the SENSE– pin changes depending on the common mode voltage. When SENSE– is less than $INTV_{CC}$ – 0.5V, a small current of less than 1µA flows out of the pin. When SENSE– is above $INTV_{CC}$ + 0.5V, a higher current (≈850µA) flows into the pin. Between $INTV_{CC}$ – 0.5V and $INTV_{CC}$ + 0.5V, the current transitions from the smaller current to the higher current.

Filter components mutual to the sense lines should be placed close to the LTC7801, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 2). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 3b), resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

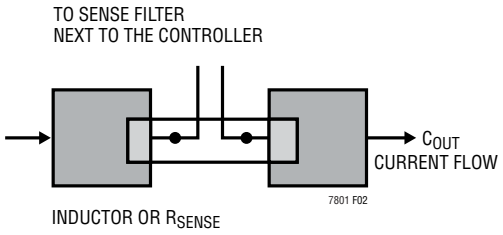



**Figure 2. Sense Lines Placement with Inductor or Sense Resistor**

### Low Value Resistor Current Sensing

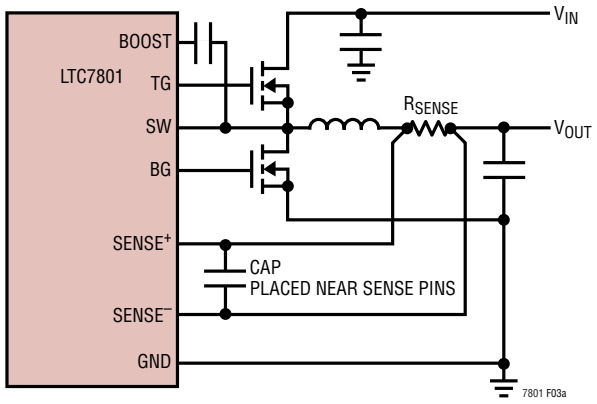
A typical sensing circuit using a discrete resistor is shown in Figure 3a. $R_{SENSE}$ is chosen based on the required output current.

The current comparator has a maximum threshold $V_{SENSE(MAX)}$ determined by the ILIM setting. The current comparator threshold voltage sets the peak of the inductor current, yielding a maximum average output current, $I_{MAX}$, equal to the peak value less half the peak-to-peak ripple current, $\Delta I_L$. To calculate the sense resistor value, use the equation:

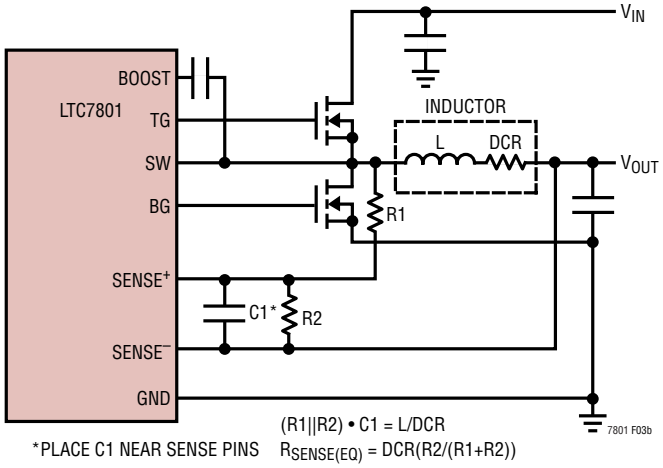
$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

Normally in high duty cycle conditions, the maximum output current level will be reduced due to the internal compensation required to meet stability criterion operating at greater than 50% duty factor. The LTC7801, however, uses a proprietary circuit to nullify the effect of slope compensation on the current limit performance.

## APPLICATIONS INFORMATION




**(3a) Using a Resistor to Sense Current**




**(3b) Using the Inductor DCR to Sense Current**

**Figure 3. Current Sensing Methods**

### Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC7801 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 3b. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor would cost several points of efficiency compared to inductor DCR sensing.

If the external (R1||R2) • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in the Electrical Characteristics table.

Next, determine the DCR of the inductor. When provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value ($R_D$), use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1|| R2 to around 2k, reducing error that might have been caused by the SENSE+ pin's ±1µA current.

The equivalent resistance R1||R2 is scaled to the temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR \text{ at } 20°C) \bullet C1}$$

## APPLICATIONS INFORMATION

The values for R1 and R2 are:

$$R1 = \frac{R1||R2}{R_D}; R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}R1 = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

### Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current, $\Delta I_L$, decreases with higher inductance or higher frequency and increases with higher $V_{IN}$:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of $\Delta I_L$ allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum $\Delta I_L$ occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below the burst clamp, which can be programmed between 10% and 60% of the current limit determined by $R_{SENSE}$. (For more information see the Burst Clamp Programming section.) Lower inductor values (higher $\Delta I_L$) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

### Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

### Power MOSFET Selection

Two external power MOSFETs must be selected for the LTC7801 controller: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

## APPLICATIONS INFORMATION

The peak-to-peak drive levels are set by the $DRV_{CC}$ voltage. This voltage can range from 5V to 10V depending on configuration of the DRVSET pin. Therefore, both logic-level and standard-level threshold MOSFETs can be used in most applications depending on the programmed $DRV_{CC}$ voltage. Pay close attention to the $BV_{DSS}$ specification for the MOSFETs as well.

The LTC7801's ability to adjust the gate drive level between 5V to 10V (OPTI-DRIVE) allows an application circuit to be precisely optimized for efficiency. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, Miller capacitance $C_{MILLER}$, input voltage and maximum output current. Miller capacitance, $C_{MILLER}$, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. $C_{MILLER}$ is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in $V_{DS}$. This result is then multiplied by the ratio of the application applied $V_{DS}$ to the gate charge curve specified $V_{DS}$. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{MAIN SWITCH DUTY CYCLE} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{SYNCHRONOUS SWITCH DUTY CYCLE} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)} +$$

$$(V_{IN})^2\left(\frac{I_{OUT(MAX)}}{2}\right)(R_{DR})(C_{MILLER})\bullet$$

$$\left[\frac{1}{V_{DRVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)}$$

where $\delta$ is the temperature dependency of $R_{DS(ON)}$ and $R_{DR}$ (approximately $2\Omega$) is the effective driver resistance at the MOSFET's Miller threshold voltage. $V_{THMIN}$ is the typical MOSFET minimum threshold voltage.

Both MOSFETs have $I^2R$ losses while the main N-channel equations include an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower $C_{MILLER}$ actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term $(1+\delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

### $C_{IN}$ and $C_{OUT}$ Selection

The selection of $C_{IN}$ is usually based off the worst-case RMS input current. The highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula shown in Equation 1 to determine the maximum RMS capacitor current requirement.

## APPLICATIONS INFORMATION

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN}-V_{OUT})\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC7801, ceramic capacitors can also be used for $C_{IN}$. Always consult the manufacturer if there is any question.

A small (0.1µF to 1µF) bypass capacitor between the chip $V_{IN}$ pin and ground, placed close to the LTC7801, is also suggested. A small (≤10Ω) resistor placed between $C_{IN}$ (C1) and the $V_{IN}$ pin provides further isolation.

The selection of $C_{OUT}$ is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple ($\Delta V_{OUT}$) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L\left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}}\right)$$

where f is the operating frequency, $C_{OUT}$ is the output capacitance and $\Delta I_L$ is the ripple current in the inductor. The output ripple is highest at maximum input voltage since $\Delta I_L$ increases with input voltage.

### Setting Output Voltage

The LTC7801 output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 4. The regulated output voltage is determined by:

$$V_{OUT} = 0.8V\left(1 + \frac{R_B}{R_A}\right)$$

To improve the frequency response, a feedforward capacitor, $C_{FF}$, may be used. Great care should be taken to route the $V_{FB}$ line away from noise sources, such as the inductor or the SW line.

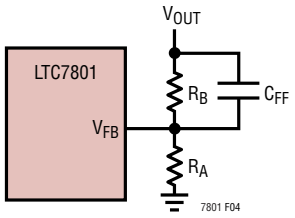



**Figure 4. Setting Output Voltage**

### RUN Pin and Overvoltage/Undervoltage Lockout

The LTC7801 is enabled using the RUN pin. It has a rising threshold of 1.2V with 80mV of hysteresis. Pulling the RUN pin below 1.12V shuts down the main control loop. Pulling it below 0.7V disables the controller and most internal circuits, including the $DRV_{CC}$ and $INTV_{CC}$ LDOs. In this state the LTC7801 draws only 10µA of quiescent current.

The RUN pin is high impedance below 3V and must be externally pulled up/down or driven directly by logic. The RUN pin can tolerate up to 150V (absolute maximum), so it can be conveniently tied to $V_{IN}$ in always-on applications where the controller is enabled continuously and never shut down. Above 3V, the RUN pin has approximately a 15MΩ impedance to an internal 3V clamp.

## APPLICATIONS INFORMATION

The RUN and OVLO pins can alternatively be configured as undervoltage (UVLO) and overvoltage (OVLO) lockouts on the $V_{IN}$ supply with a resistor divider from $V_{IN}$ to ground. A simple resistor divider can be used as shown in Figure 5 to meet specific $V_{IN}$ voltage requirements.

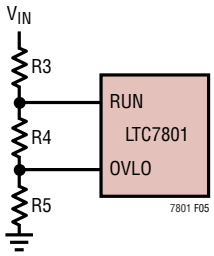



**Figure 5. Adjustable UV and OV Lockout**

The current that flows through the R3-R4-R5 divider will directly add to the shutdown, sleep, and active current of the LTC7801, and care should be taken to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the megaohm range may be required to keep the impact on quiescent shutdown and sleep currents low. To pick resistor values, the sum total of R3 + R3+ R5 ($R_{TOTAL}$) should be chosen first based on the allowable DC current that can be drawn from $V_{IN}$.

The individual values of R3, R4 and R5 can be calculated from the following equations:

$$R5 = R_{TOTAL} \bullet \frac{1.20V}{\text{RISING } V_{IN} \text{ OVLO THRESHOLD}}$$

$$R4 = R_{TOTAL} \bullet \frac{1.20V}{\text{RISING } V_{IN} \text{ OVLO THRESHOLD}} - R5$$

$$R3 = R_{TOTAL} - R5 - R4$$

For applications that do not require a precise OVLO, the OVLO pin can be tied directly to ground. The RUN pin in this type of application can be used as an external UVLO using the previous equations with R5 = 0Ω.

Similarly, for applications that do not require a precise UVLO, the RUN pin can be tied to $V_{IN}$. In this configuration, the UVLO threshold is limited to the internal $DRV_{CC}$ UVLO thresholds as shown in the Electrical Characteristics table. The resistor values for the OVLO can be computed using the previous equations with R3 = 0Ω.

### Soft-Start (SS) Pin

The start-up of $V_{OUT}$ is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the internal 0.8V reference, the LTC7801 regulates the $V_{FB}$ pin voltage to the voltage on the SS pin instead of the internal reference. The SS pin can be used to program an external soft-start function.

Soft-start is enabled by simply connecting a capacitor from the SS pin to ground, as shown in Figure 6. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the SS pin. The LTC7801 will regulate its feedback voltage (and hence $V_{OUT}$) according to the voltage on the SS pin, allowing $V_{OUT}$ to rise smoothly from 0V to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{0.8V}{10\mu A}$$

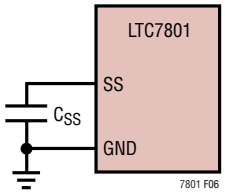



**Figure 6. Using the SS Pin to Program Soft-Start**

## APPLICATIONS INFORMATION

The SS pin also controls the timing of the regulator shutdown (REGSD) feature (as discussed in Regulator Shutdown of the Operation section). If the application does not require the use of the $EXTV_{CC}$ LDO (the $EXTV_{CC}$ pin is grounded), the REGSD feature must be defeated with a pull-up resistor between SS and $INTV_{CC}$, as shown in Figure 7. Any resistor 330k or smaller between SS and $INTV_{CC}$ defeats the 5µA pull-down current on SS that turns on once SS reaches 2.2V (with the $EXTV_{CC}$ LDO not enabled), preventing SS from discharging to 2.0V and shutting down the regulator. Note the current through this pull-up resistor adds to the internal 10µA SS pull-up current at start-up, causing the total soft-start time to be shorter than what it is calculated without the pull-up resistor. The total soft-start time with the pull-up resistor is approximately:

$$t_{SS} \approx C_{SS} \bullet \frac{0.8V}{\left(10\mu A + \frac{4.6V}{R_{SS}}\right)}$$

where $R_{SS}$ is the value of the resistor between the SS and $INTV_{CC}$ pins.

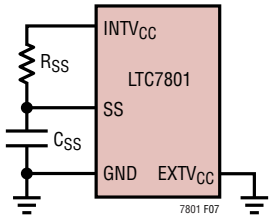



**Figure 7. Using the SS Pin to Program Soft-Start with $EXTV_{CC}$ Unused/Grounded to Defeat REGSD**

### $DRV_{CC}$ Regulators (OPTI-DRIVE)

The LTC7801 features three separate low dropout linear regulators (LDO) that can supply power at the $DRV_{CC}$ pin. The internal $V_{IN}$ LDO uses an internal P-channel pass device between the $V_{IN}$ and $DRV_{CC}$ pins. The internal $EXTV_{CC}$ LDO uses an internal P-channel pass device between the $EXTV_{CC}$ and $DRV_{CC}$ pins. The NDRV LDO utilizes the NDRV pin to drive the gate of an external N-channel MOSFET acting as a linear regulator with its drain connected to $V_{IN}$.

The NDRV LDO provides an alternative method to supply power to $DRV_{CC}$ from the input supply without dissipating the power inside the LTC7801 IC. It has an internal charge pump that allows NDRV to be driven above the $V_{IN}$ supply, allowing for low dropout performance. The $V_{IN}$ LDO has a slightly lower regulation point than the NDRV LDO, such that all $DRV_{CC}$ current flows through the external N-channel MOSFET (and not through the internal P-channel pass device) once $DRV_{CC}$ reaches regulation.

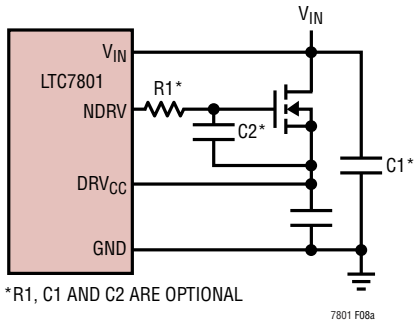
When laying out the PC board, care should be taken to route NDRV away from any switching nodes, especially SW, TG, and BOOST. Coupling to the NDRV node could cause its voltage to collapse and the NDRV LDO to lose regulation. If this occurs, the internal $V_{IN}$ LDO would take over and maintain $DRV_{CC}$ voltage at a slightly lower regulation point. However, internal heating of the IC would become a concern. High frequency noise on the drain of the external NFET could also couple into the NDRV node (through the gate-to-drain capacitance of the NDRV NFET) and adversely affect NDRV regulation. The following are methods that could mitigate this potential issue (refer to Figure 8a).

1. Add local decoupling capacitors right next to the drain of the external NDRV NFET in the PCB layout.
2. Insert a resistor (~100Ω) in series with the gate of the NDRV NFET.
3. Insert a small capacitor (~1nF) between the gate and source of the NDRV NFET.

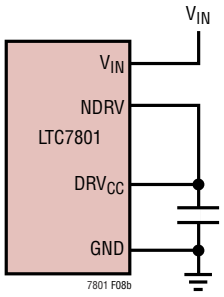
When testing the application circuit, be sure the NDRV voltage does not collapse over the entire input voltage and output current operating range of the buck regulator.

## APPLICATIONS INFORMATION

If the NDRV LDO is not being used, connect the NDRV pin to $DRV_{CC}$ (Figure 8b).




**(8a). Configuring the NDRV LDO**




**(8b). Disabling the NDRV LDO**

**Figure 8.**

The $DRV_{CC}$ supply is regulated between 5V to 10V, depending on how the DRVSET pin is set. The internal $V_{IN}$ and $EXTV_{CC}$ LDOs can supply a peak current of at least 50mA. The $DRV_{CC}$ pin must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers.

The DRVSET pin programs the $DRV_{CC}$ supply voltage and the DRVUV pin selects different $DRV_{CC}$ UVLO and $EXTV_{CC}$ switchover threshold voltages. Table 1 summarizes the different DRVSET pin configurations along with the voltage settings that go with each configuration. Table 2 summarizes the different DRVUV pin settings. Tying the DRVSET pin to $INTV_{CC}$ programs $DRV_{CC}$ to 10V. Tying the DRVSET pin to GND programs $DRV_{CC}$ to 6V. Placing a 50k to 100k resistor between DRVSET and GND the programs $DRV_{CC}$ between 5V to 10V, as shown in Figure 9. See PC Board Layout Checklist in the Applications Information section for additional considerations when using higher DRVSET settings.

**Table 1.**

| DRVSET PIN | $DRV_{CC}$ VOLTAGE |
|---|---|
| GND | 6V |
| $INTV_{CC}$ | 10V |
| Resistor to GND 50k to 100k | 5V to 10V |

**Table 2.**

| DRVUV | $DRV_{CC}$ UVLO RISING/FALLING THRESHOLDS | $EXTV_{CC}$ SWITCHOVER RISING/FALLING THRESHOLD |
|---|---|---|
| GND | 4.0V/3.8V | 4.7V/4.45V |
| $INTV_{CC}$ | 7.5V/6.7V | 7.7V/7.45V |

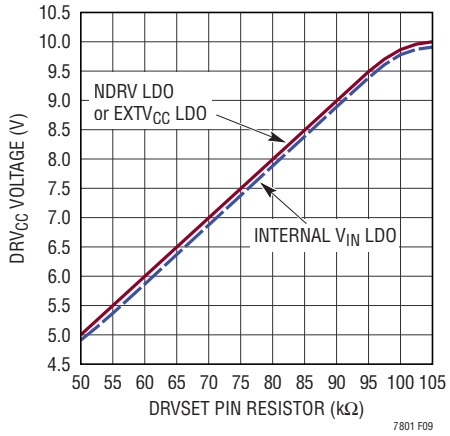



**Figure 9. Relationship Between $DRV_{CC}$ Voltage and Resistor Value at DRVSET Pin**

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC7801 to be exceeded. The $DRV_{CC}$ current, which is dominated by the gate charge current, may be supplied by the $V_{IN}$ LDO, NDRV LDO or the $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than its switchover threshold (4.7V or 7.7V as determined by the DRVUV pin described above), the $V_{IN}$ and NDRV LDOs are enabled. Power dissipation in this case is highest and is equal to $V_{IN} \bullet IDRV_{CC}$. If the NDRV LDO is not being used, this power is dissipated inside the IC. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section.

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The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, if $DRV_{CC}$ is set to 6V, the $DRV_{CC}$ current is limited to less than 32mA from a 40V supply when not using the $EXTV_{CC}$ or NDRV LDOs at a 70°C ambient temperature in the QFN package:

$T_J = 70°C + (32mA)(40V)(43°C/W) = 125°C$

To prevent the maximum junction temperature from being exceeded, the $V_{IN}$ supply current must be checked while operating in forced continuous mode (MODE = $INTV_{CC}$) at maximum $V_{IN}$.

When the voltage applied to $EXTV_{CC}$ rises above its switchover threshold, the $V_{IN}$ and NDRV LDOs are turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above the switchover threshold minus the comparator hysteresis. The $EXTV_{CC}$ LDO attempts to regulate the $DRV_{CC}$ voltage to the voltage as programmed by the DRVSET pin, so while $EXTV_{CC}$ is less than this voltage, the LDO is in dropout and the $DRV_{CC}$ voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than the programmed voltage, up to an absolute maximum of 14V, $DRV_{CC}$ is regulated to the programmed voltage.

Using the $EXTV_{CC}$ LDO allows the MOSFET driver and control power to be derived from the LTC7801's switching regulator output (4.7V/7.7V ≤ $V_{OUT}$ ≤ 14V) during normal operation and from the $V_{IN}$ or NDRV LDO when the output is out of regulation (e.g., start-up, short-circuit). If more current is required through the $EXTV_{CC}$ LDO than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and $DRV_{CC}$ pins. In this case, do not apply more than 10V to the $EXTV_{CC}$ pin and make sure that $EXTV_{CC}$ ≤ $V_{IN}$.

Significant efficiency and thermal gains can be realized by powering $DRV_{CC}$ from the output, since the $V_{IN}$ current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency).

For 5V to 14V regulator outputs, this means connecting the $EXTV_{CC}$ pin directly to $V_{OUT}$. Tying the $EXTV_{CC}$ pin to an 8.5V supply reduces the junction temperature in the previous example from 125°C to:

$T_J = 70°C + (32mA)(8.5V)(43°C/W) = 82°C$

However, for 3.3V and other low voltage outputs, additional circuitry is required to derive $DRV_{CC}$ power from the output.

The following list summarizes the five possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This will cause $DRV_{CC}$ to be powered from the internal $V_{IN}$ or NDRV LDO resulting in an efficiency penalty of up to 10% at high input voltages. If $EXTV_{CC}$ is grounded, the REGSD feature must be defeated with a pull-up resistor 330k or smaller between SS and $INTV_{CC}$.
2. $EXTV_{CC}$ connected directly to the regulator output. This is the normal connection for a 5V to 14V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5V to 14V range, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. Ensure that $EXTV_{CC}$ ≤ $V_{IN}$.
4. $EXTV_{CC}$ connected to the regulator output through an external zener diode. If the output voltage is greater than 14V, a zener diode can be used to drop the necessary voltage between $V_{OUT}$ and $EXTV_{CC}$ such that $EXTV_{CC}$ remains below 14V (Figure 10). In this configuration, a bypass capacitor on $EXTV_{CC}$ of at least 0.1µF is recommended. An optional resistor between $EXTV_{CC}$ and GND can be inserted to ensure adequate bias current through the zener diode.

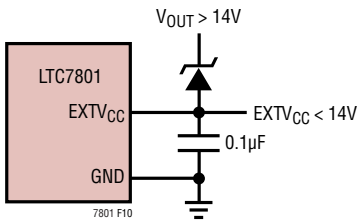



**Figure 10. Using a Zener Diode Between $V_{OUT}$ and $EXTV_{CC}$**

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5. $EXTV_{CC}$ connected to an output-derived boost network off the regulator output. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.7V/7.7V. Ensure that $EXTV_{CC} \leq V_{IN}$.

### $INTV_{CC}$ Regulator

An additional P-channel LDO supplies power at the $INTV_{CC}$ pin from the $DRV_{CC}$ pin. Whereas $DRV_{CC}$ powers the gate drivers, $INTV_{CC}$ powers much of the LTC7801's internal circuitry. The $INTV_{CC}$ supply must be bypassed with a 0.1µF ceramic capacitor. $INTV_{CC}$ is also used as a pull-up to bias other pins, such as MODE, PGOOD, etc.

### Topside MOSFET Driver Supply ($C_B$)

An external bootstrap capacitor $C_B$ connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. The LTC7801 features an internal switch between $DRV_{CC}$ and the BOOST pin. This internal switch eliminates the need for an external bootstrap diode between $DRV_{CC}$ and BOOST in most applications. Adding an external, low leakage diode is recommended for applications that involve higher output voltages and/or higher gate charge top MOSFETs. Capacitor $C_B$ in the Functional Diagram is charged from $DRV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the $C_B$ voltage across the gate-source of the MOSFET. This enhances the top MOSFET switch and turns it on. The switch node voltage, SW, rises to $V_{IN}$ and the BOOST pin follows. With the topside MOSFET on, the BOOST voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{DRVCC}$. The value of the boost capacitor, $C_B$, needs to be 100 times that of the total input capacitance of the topside MOSFET(s).

It is recommended that a placeholder footprint for an external bootstrap diode between DRVCC and BOOST be placed on the PCB board.

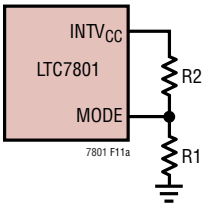
### Burst Clamp Programming

Burst Mode operation is enabled if the voltage on the MODE pin is 0V or in the range between 0.5V to 1V. The burst clamp, which sets the minimum peak inductor current, can be programmed by the MODE pin voltage. If the MODE pin is grounded, the burst clamp is set to 25% of the maximum sense voltage ($V_{SENSE(MAX)}$). A MODE pin voltage between 0.5V and 1V varies the burst clamp linearly between 10% and 60% of $V_{SENSE(MAX)}$ through the following equation:

$$\text{BURST CLAMP} = \frac{V_{MODE} - 0.4V}{1V} \bullet 100$$

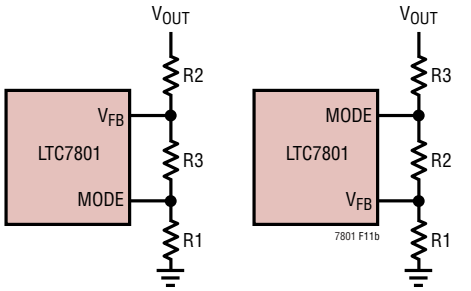
where $V_{MODE}$ is the voltage on the MODE pin and Burst Clamp is the percentage of $V_{SENSE(MAX)}$. The burst clamp level is determined by the desired amount of output voltage ripple at low output loads. As the burst clamp increases, the sleep time between pulses and the output voltage ripple increase.

The MODE pin is high impedance and $V_{MODE}$ can be set by a resistor divider from the $INTV_{CC}$ pin (Figure 11a). Alternatively, the MODE pin can be tied directly to the $V_{FB}$ pin to set the burst clamp to 40% ($V_{MODE}$ = 0.8V), or through an additional divider resistor (R3). As shown in Figure 11b, this resistor can be placed below $V_{FB}$ to




BURST CLAMP = 10% TO 60%

**(11a) Using $INTV_{CC}$ to Program the Burst Clamp**




BURST CLAMP = 10% TO 40% BURST CLAMP = 40% TO 60%

**(11b) Using $V_{FB}$ to Program the Burst Clamp**

**Figure 11. Programming the Burst Clamp**

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program the burst clamp between 10% and 40% ($V_{MODE}$ = 0.5V to 0.8V) or above $V_{FB}$ to program the burst clamp between 40% and 60% ($V_{MODE}$ = 0.8V to 1.0V).

### Fault Conditions: Current Limit and Current Foldback

The LTC7801 includes current foldback to help limit load current when the output is shorted to ground. If the output voltage falls below 70% of its nominal output level, then the maximum sense voltage is progressively lowered from 100% to 40% of its maximum selected value. Under short-circuit conditions with very low duty cycles, the LTC7801 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)}$, of the LTC7801 (≈80ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)}\left(\frac{V_{IN}}{L}\right)$$

The resulting average short-circuit current is:

$$I_{SC} = 45\% \bullet I_{LIM(MAX)} - \frac{1}{2}\Delta I_{L(SC)}$$

### Fault Conditions: Overvoltage Protection (Crowbar)

The overvoltage crowbar is designed to blow a system input fuse when the output voltage of the regulator rises much higher than nominal levels. The crowbar causes huge currents to flow, that blow the fuse to protect against a shorted top MOSFET if the short occurs while the controller is operating.

A comparator monitors the output for overvoltage conditions. The comparator detects faults greater than 10% above the nominal output voltage. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared. The bottom MOSFET remains on continuously for as long as the overvoltage condition persists; if $V_{OUT}$ returns to a safe level, normal operation automatically resumes.

A shorted top MOSFET will result in a high current condition which will open the system fuse. The switching regulator will regulate properly with a leaky top MOSFET by altering the duty cycle to accommodate the leakage.

### Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self heating on chip, the overtemperature shutdown circuitry will shut down the LTC7801. When the junction temperature exceeds approximately 175°C, the overtemperature circuitry disables the $DRV_{CC}$ LDO, causing the $DRV_{CC}$ supply to collapse and effectively shutting down the entire LTC7801 chip. Once the junction temperature drops back to the approximately 155°C, the $DRV_{CC}$ LDO turns back on. Long term overstress ($T_J$ > 125°C) should be avoided as it can degrade the performance or shorten the life of the part.

### Phase-Locked Loop and Frequency Synchronization

The LTC7801 has an internal phase-locked loop (PLL) comprised of a phase frequency detector, a lowpass filter, and a voltage-controlled oscillator (VCO). This allows the turn-on of the top MOSFET to be locked to the rising edge of an external clock signal applied to the PLLIN pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

If the external clock frequency is greater than the internal oscillator's frequency, $f_{OSC}$, then current is sourced continuously from the phase detector output, pulling up the VCO input. When the external clock frequency is less than $f_{OSC}$, current is sunk continuously, pulling down the VCO input.

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If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage at the VCO input is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the internal filter capacitor, $C_{LP}$, holds the voltage at the VCO input.

Note that the LTC7801 can only be synchronized to an external clock whose frequency is within range of the LTC7801's internal VCO, which is nominally 55kHz to 1MHz. This is guaranteed to be between 75kHz and 850kHz. The LTC7801 is guaranteed to synchronize to an external clock that swings up to at least 2.8V and down to 0.5V or less.

Rapid phase-locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. The VCO's input voltage is prebiased at a frequency corresponding to the frequency set by the FREQ pin. Once prebiased, the PLL only needs to adjust the frequency slightly to achieve phase lock and synchronization. Although it is not required that the free-running frequency be near the external clock frequency, doing so will prevent the operating frequency from passing through a large range of frequencies as the PLL locks.

Table 3 summarizes the different states in which the FREQ pin can be used. When synchronized to an external clock, the LTC7801 operates in forced continuous mode at light loads if the MODE pin is set to Burst Mode operation or forced continuous operation. If the MODE pin is set to pulse-skipping operation, the LTC7801 maintains pulse-skipping operation when synchronized.

**Table 3.**

| FREQ PIN | PLLIN PIN | FREQUENCY |
|---|---|---|
| 0V | DC Voltage | 350kHz |
| $INTV_{CC}$ | DC Voltage | 535kHz |
| Resistor to GND | DC Voltage | 50kHz to 900kHz |
| Any of the Above | External Clock 75kHz to 850kHz | Phase Locked to External Clock |

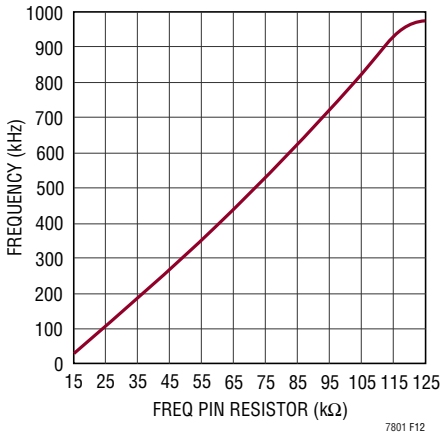



**Figure 12. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin**

### Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC7801 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC7801 is approximately 80ns. However, as the peak sense voltage decreases the minimum on-time gradually increases up to about 130ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

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### Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC7801 circuits: 1) IC $V_{IN}$ current, 2) $DRV_{CC}$ regulator current, 3) $I^2R$ losses, 4) Topside MOSFET transition losses.

1. The $V_{IN}$ current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. $V_{IN}$ current typically results in a small (< 0.1%) loss.

2. $DRV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from $DRV_{CC}$ to ground. The resulting dQ/dt is a current out of $DRV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where $Q_T$ and $Q_B$ are the gate charges of the topside and bottom side MOSFETs.

   Supplying $DRV_{CC}$ from an output-derived source power through $EXTV_{CC}$ will scale the $V_{IN}$ current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 20V to 5V application, 10mA of $DRV_{CC}$ current results in approximately 2.5mA of $V_{IN}$ current. This reduces the midcurrent loss from 10% or more (if the driver was powered directly from $V_{IN}$) to only a few percent.

3. $I^2R$ losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor and input and output capacitor ESR. In continuous mode the average output current flows through L and $R_{SENSE}$, but is chopped between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, $R_{SENSE}$ and ESR to obtain $I^2R$ losses. For example, if each $R_{DS(ON)}$ = 30mΩ, $R_L$ = 50mΩ, $R_{SENSE}$ = 10mΩ and $R_{ESR}$ = 40mΩ (sum of both input and output capacitance losses), then the total resistance is 130mΩ. This results in losses ranging from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. Efficiency varies as the inverse square of $V_{OUT}$ for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the top MOSFET(s) and become significant only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

   $$\text{Transition Loss} = (1.7) \bullet V_{IN}^2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$$

Other hidden losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that $C_{IN}$ has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

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### Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, $V_{OUT}$ shifts by an amount equal to $\Delta I_{LOAD}$ (ESR), where ESR is the effective series resistance of $C_{OUT}$. $\Delta I_{LOAD}$ also begins to charge or discharge $C_{OUT}$ generating the feedback error signal that forces the regulator to adapt to the current change and return $V_{OUT}$ to its steady-state value. During this recovery time $V_{OUT}$ can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the first page circuit will provide an adequate starting point for most applications.

The ITH series $R_C$-$C_C$ filter sets the dominant pole-zero loop compensation. The values can be modified slightly to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing $R_C$ and the bandwidth of the loop will be increased by decreasing $C_C$. If $R_C$ is increased by the same factor that $C_C$ is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with $C_{OUT}$, causing a rapid drop in $V_{OUT}$. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of $C_{LOAD}$ to $C_{OUT}$ is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • $C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

### Design Example

As a design example, assume $V_{IN}$ = 12V (nominal), $V_{IN}$ = 22V (max), $V_{OUT}$ = 3.3V, $I_{MAX}$ = 5A, $V_{SENSE(MAX)}$ = 75mV and f = 350kHz. The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Tie the FREQ pin to GND, generating 350kHz operation. The inductor ripple current can be calculated from the following equation:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN(NOM)}}\right)$$

A 4.7µH inductor will produce 29% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 5.73A. Increasing the ripple

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current will also help ensure that the minimum on-time of 80ns is not violated. The minimum on-time occurs at maximum $V_{IN}$:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}(f)} = \frac{3.3V}{22V(350kHz)} = 429ns$$

The equivalent $R_{SENSE}$ resistor value can be calculated by using the minimum value for the maximum current sense threshold (66mV):

$$R_{SENSE} \leq \frac{66mV}{5.73A} \simeq 0.01\Omega$$

Choosing 1% resistors: $R_A$ = 24.9k and $R_B$ = 78.7k yields an output voltage of 3.33V.

The power dissipation on the topside MOSFET can be easily estimated. Choosing a Fairchild FDS6982S dual MOSFET results in: $R_{DS(ON)}$ = 0.035Ω/0.022Ω, $C_{MILLER}$ = 215pF. With 6V gate drive and maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} = \frac{3.3V}{22V}(5A)^2\left[1+(0.005)(50°C-25°C\right]$$

$$(0.035\Omega)+(22V)^2\frac{5A}{2}(2.5\Omega)(215pF)\bullet$$

$$\left[\frac{1}{6V-2.3V}+\frac{1}{2.3V}\right](350kHz) = 308mW$$

A short-circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{34mV}{0.01\Omega} - \frac{1}{2}\left(\frac{80ns(22V)}{4.7\mu H}\right) = 3.21A$$

with a typical value of $R_{DS(ON)}$ and δ = (0.005/°C)(25°C) = 0.125. The resulting power dissipated in the bottom MOSFET is:

$$P_{SYNC} = (3.21A)^2\ (1.125)\ (0.022\Omega) = 255mW$$

which is less than under full-load conditions. $C_{IN}$ is chosen for an RMS current rating of at least 3A at temperature. $C_{OUT}$ is chosen with an ESR of 0.02Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}\ (\Delta I_L) = 0.02\Omega\ (1.45A) = 29mV_{P-P}$$

### PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of $C_{DRVCC}$ must return to the combined $C_{OUT}$ (–) terminals. The path formed by the top N-channel MOSFET, bottom N-channel MOSFET and the $C_{IN}$ capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other.
2. Does the LTC7801 $V_{FB}$ pin's resistive divider connect to the (+) terminal of $C_{OUT}$? The resistive divider must be connected between the (+) terminal of $C_{OUT}$ and signal ground. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).
3. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.
4. Is the $DRV_{CC}$ and decoupling capacitor connected close to the IC, between the $DRV_{CC}$ and the ground pin? This capacitor carries the MOSFET drivers' current peaks.
5. Keep the SW, TG, and BOOST nodes away from sensitive small-signal nodes. All of these nodes have very large and fast moving signals and therefore should be kept on the output side of the LTC7801 and occupy minimum PC trace area.
6. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $DRV_{CC}$

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decoupling capacitor, the bottom of the voltage feedback resistive divider and the GND pin of the IC.

7. The TG and BG traces from the controller IC to the gates of the external MOSFETs should be kept as short as possible to minimize the parasitic inductance. This inductance can cause voltages spikes that can potentially significantly exceed the supply rails of the drivers and damage them, especially with high gate charge MOSFETs and when using gate drive settings above 8V. Small capacitors (~1nF) placed as close as possible to the TG/SW and BG/GND pins can be used to filter these spikes.
8. It is recommended that a placeholder footprint for an external bootstrap diode between DRVCC and BOOST be placed on the PCB board.

### PC Board Layout Debugging

It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 25% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required.

Reduce $V_{IN}$ from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering $V_{IN}$ while monitoring the output to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between $C_{IN}$, the top MOSFET and the bottom MOSFET to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

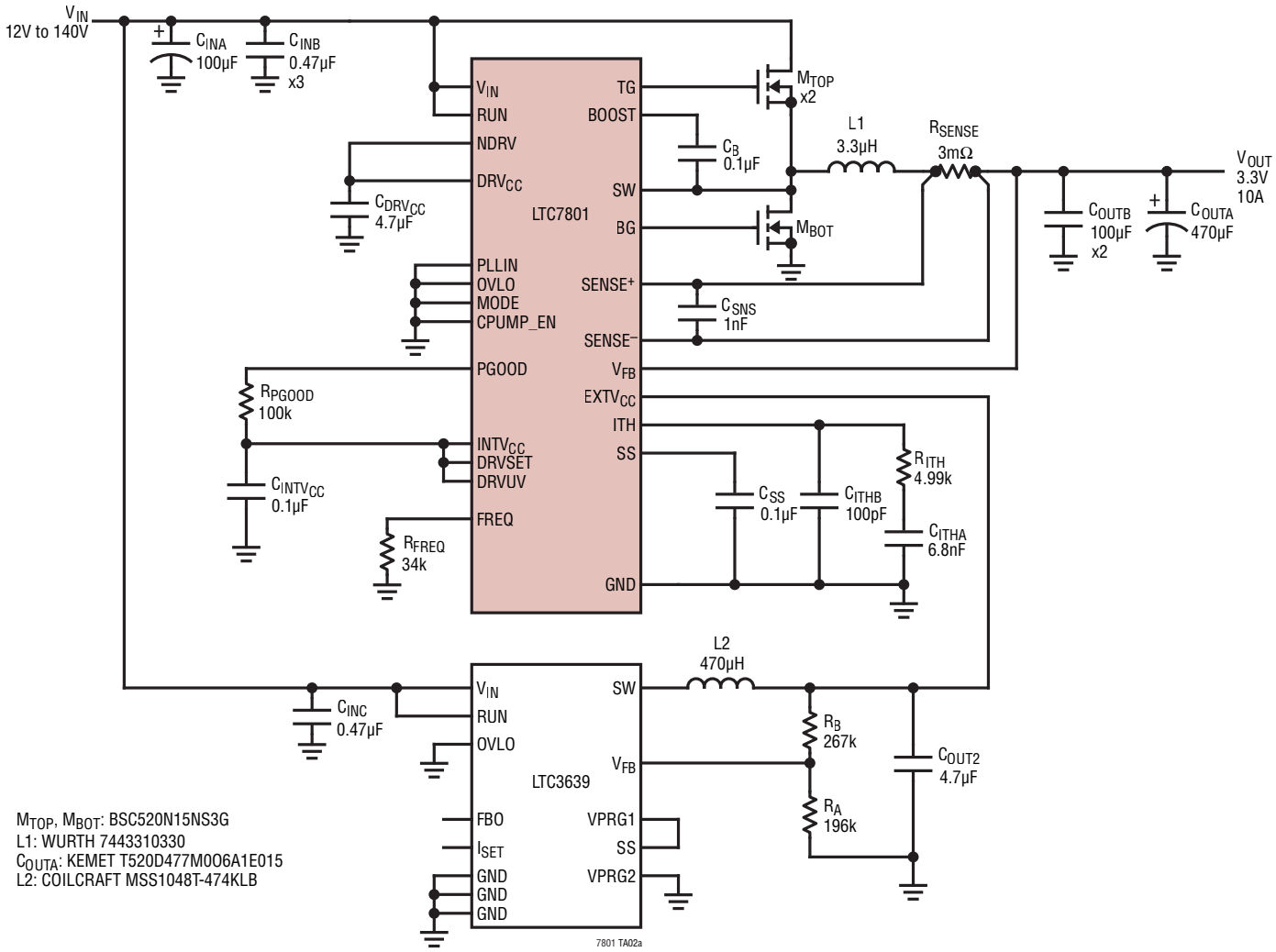
An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

### Pin Clearance/Creepage Considerations

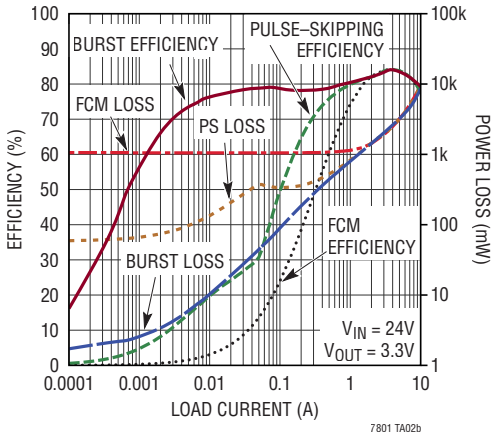
The LTC7801 is available in two packages (QFN and TSSOP) with identical functionality. However, the space between adjacent pins on the LTC7801 may not provide sufficient PC board trace clearance between high and low voltage pins in some higher voltage applications. In applications where clearance is required, the LTC3895 should be used. The LTC3895 has removed pins between all the adjacent high voltage and low voltage pins, providing 0.68mm clearance which is sufficient for most applications. For more information, refer to the printed circuit board design standards described in IPC-2221 (www.ipc.org).

# TYPICAL APPLICATIONS

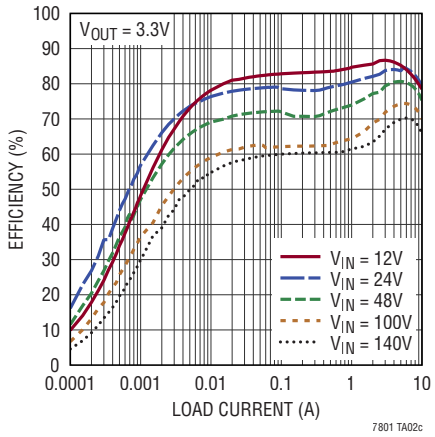
### High Efficiency 140V to 3.3V Step-Down Regulator



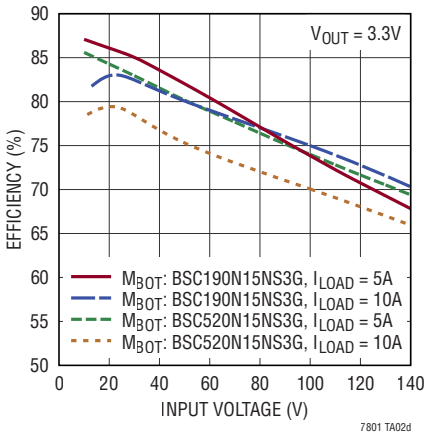

### Efficiency and Power Loss vs Load Current




### Efficiency vs Load Current



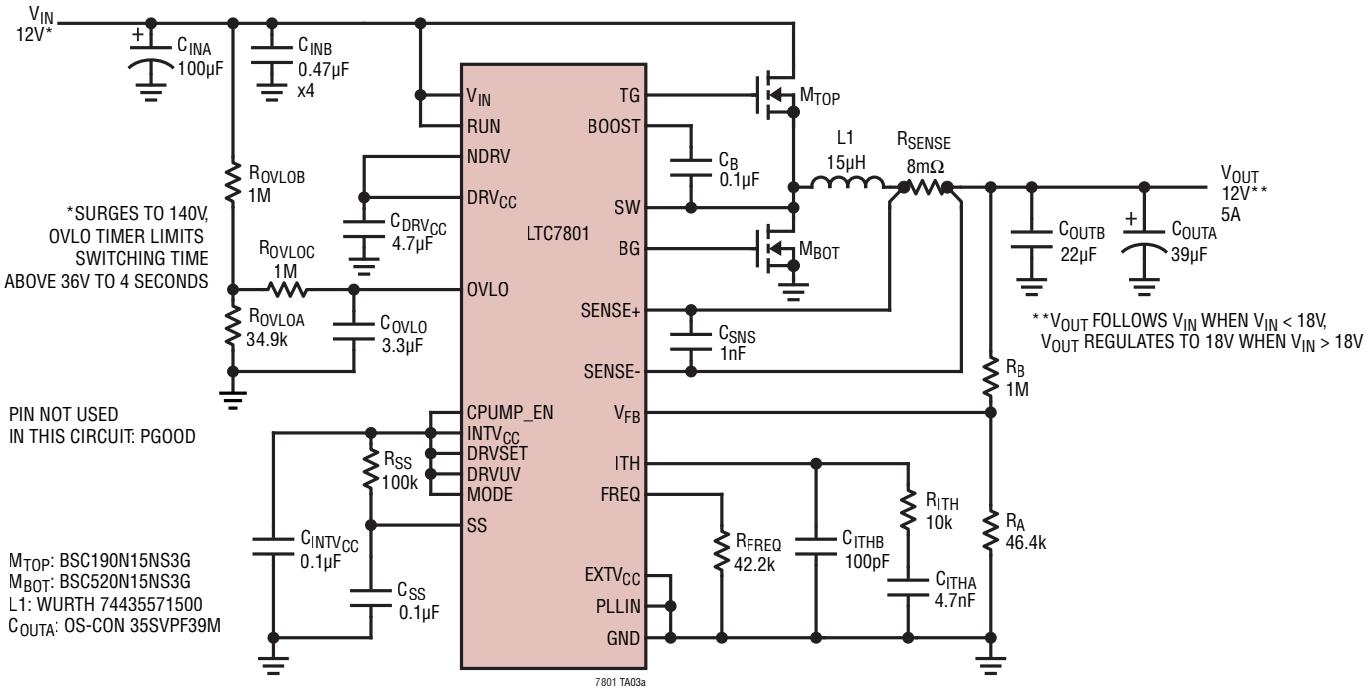

### Efficiency vs Input Voltage

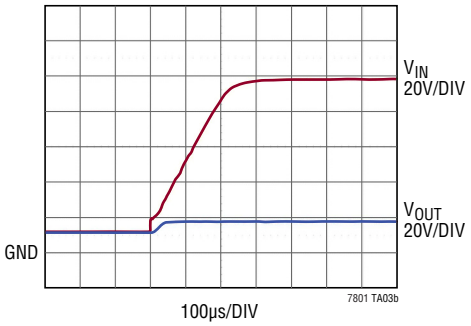


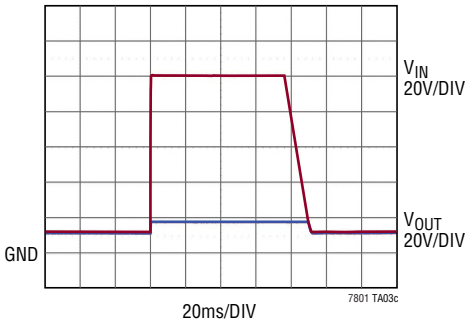

Rev. A

# TYPICAL APPLICATIONS

### High Efficiency Switching Surge Stopper

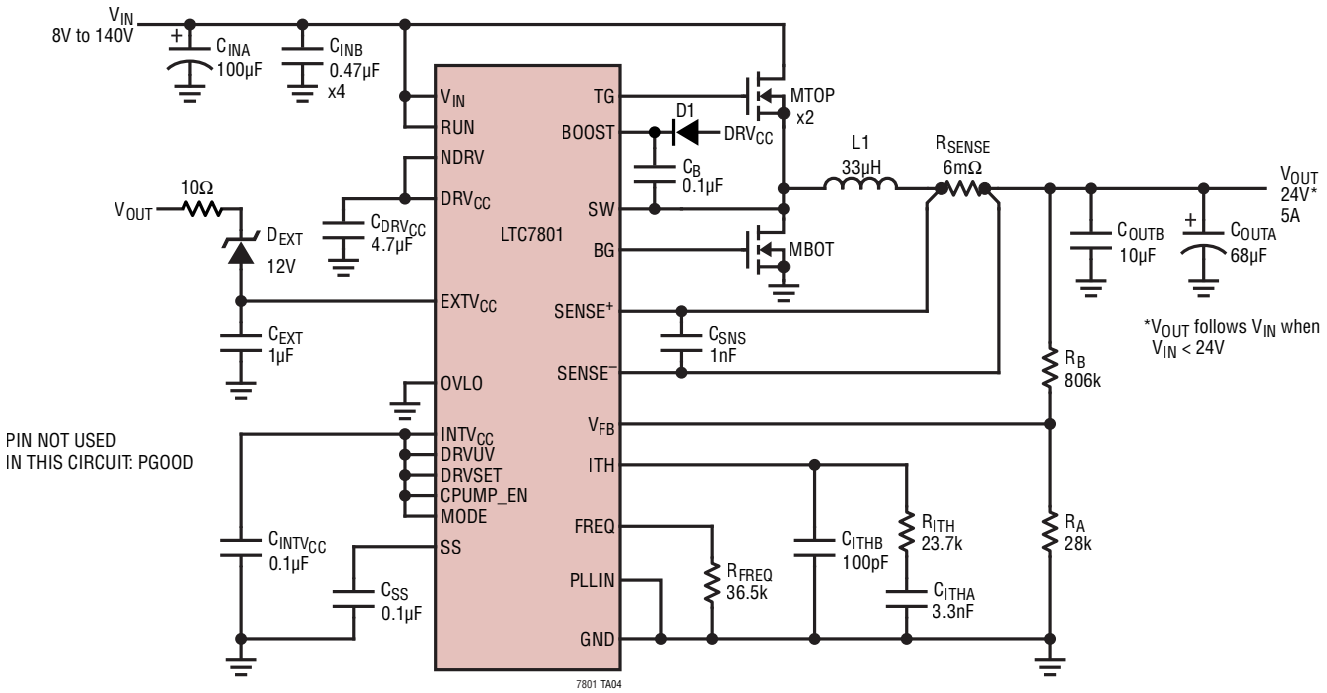


# TYPICAL APPLICATIONS

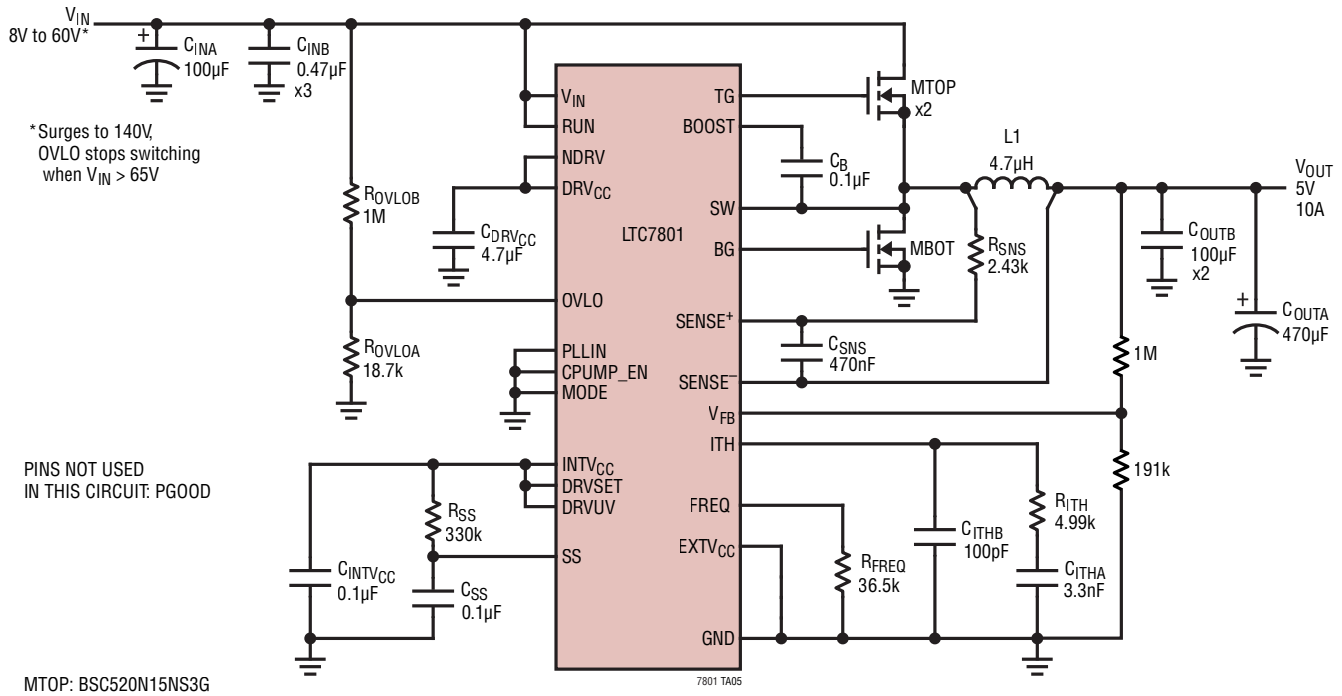
**High Efficiency 140V to 24V Step-Down Regulator**




MTOP, MBOT: BSC520N15NS3G
$D_{EXT}$: DIODES INC. SMAZ12-13-F
L1: WURTH 7443633300
$C_{OUTA}$: SUNCON 35CE68LX
D1: NEXPERIA PNE20010ER

# TYPICAL APPLICATIONS

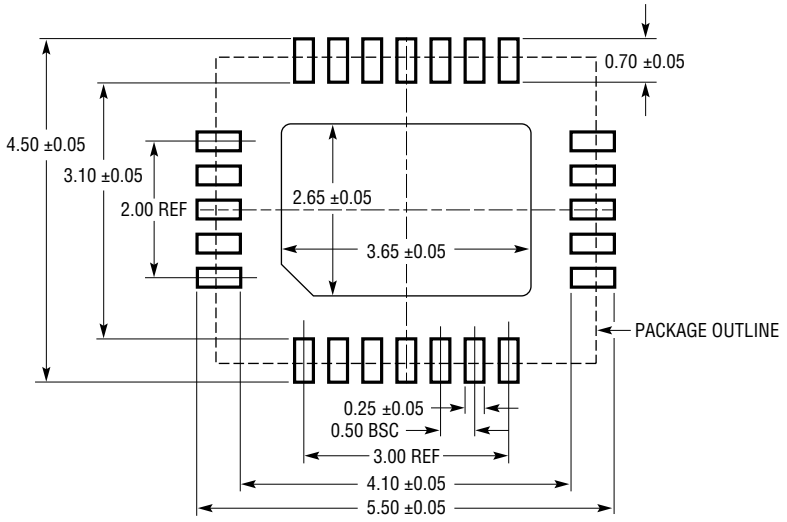
**High Efficiency 60V to 5V Step-Down Regulator with Surge Protection to 140V**



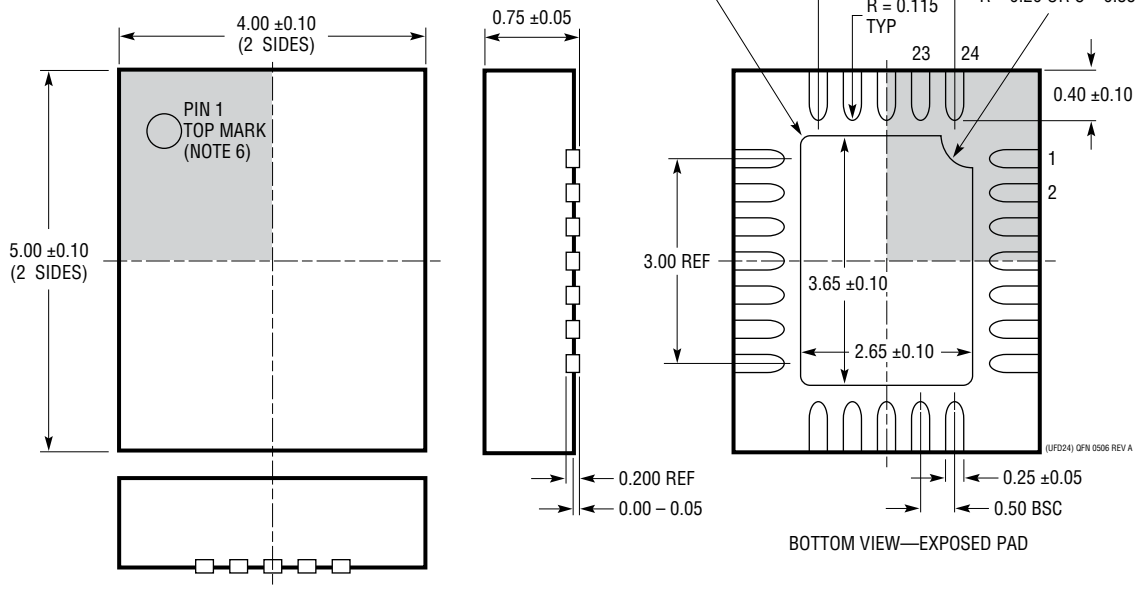

MTOP: BSC520N15NS3G
MBOT: BSC042NE7NS3G
L1: COILCRAFT XAL1010-472ME
$C_{OUTA}$: KEMET T520D477M006ATE015

# PACKAGE DESCRIPTION

**UFD Package**
**24-Lead Plastic QFN (4mm × 5mm)**
(Reference LTC DWG # 05-08-1696 Rev A)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

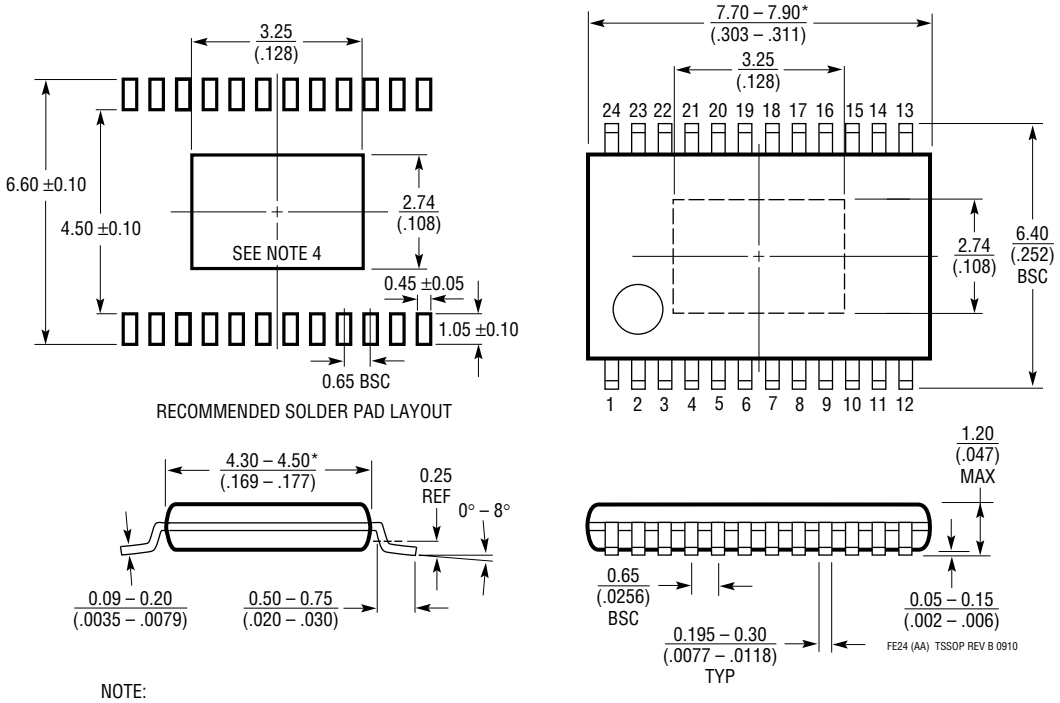



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**FE Package**
**24-Lead Plastic TSSOP (4.4mm)**
(Reference LTC DWG # 05-08-1771 Rev B)
**Exposed Pad Variation AA**




NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

# REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 12/20 | Added #7 and #8 to the PC Board Layout Checklist section<br>Added D1 Diode to the High Efficiency 140V to 24V Step-Down Regulator schematic | 31<br>34 |



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## TYPICAL APPLICATION

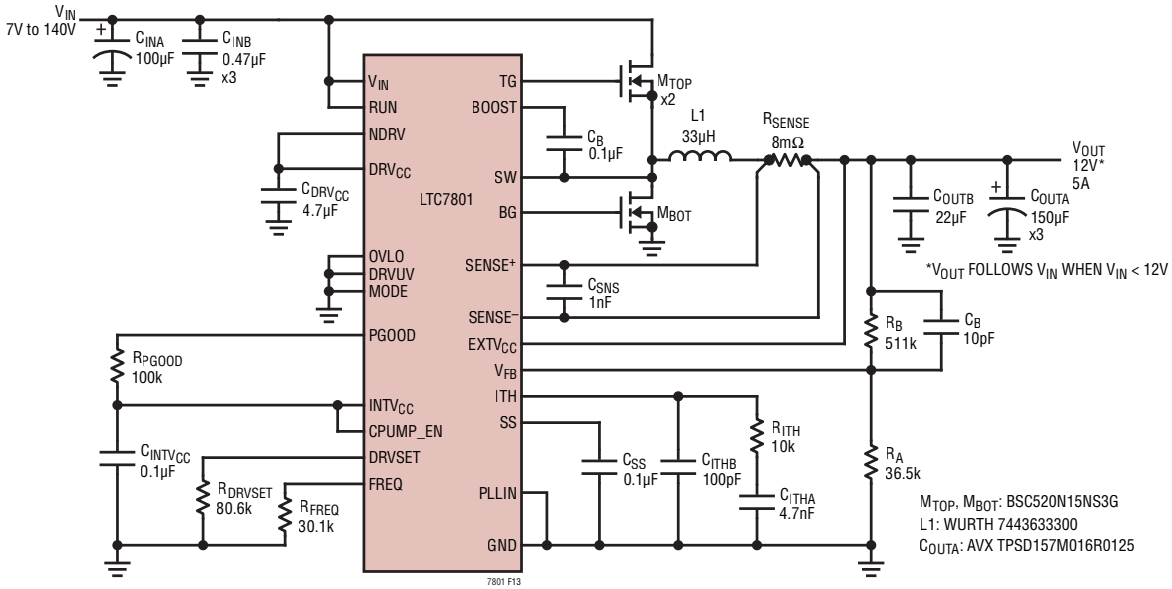



**Figure 13. High Efficiency 140V to 12V Step-Down Regulator**

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC3895 | 150V Low $I_Q$, Synchronous Step-Down DC/DC Controller 100% Duty Cycle Capability, Adjustable 5V to 10V Gate Drive | $4V \le V_{IN} \le 140V$, $150V_{PK}$, $0.8V \le V_{OUT} \le 60V$, $I_Q$ = 40µA PLL Fixed Frequency 50kHz to 900kHz |
| LTC7800 | 60V, Low $I_Q$, Synchronous Step-Down DC/DC Controller with 99% Duty Cycle | $4V \le V_{IN} \le 60V$, $0.8V \le V_{OUT} \le 24V$, $I_Q$ = 50µA PLL Fixed Frequency 320kHz to 2.25MHz |
| LTC3871 | Bidirectional PolyPhase® Synchronous Buck or Boost Controller | $V_{HIGH}$ Up to 100V, $V_{LOW}$ Up to 30V, High Power Buck or Boost On Demand |
| LTC3892/ LTC3892-1 | 60V Low $I_Q$, Dual, 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle | $4V \le V_{IN} \le 60V$, $0.8V \le V_{OUT} \le 0.99V_{IN}$, PLL Fixed Frequency 50kHz to 900kHz, Adjustable 5V to 10V Gate Drive, $I_Q$ = 29µA |
| LTC3639 | High Efficiency, 140V 100mA Synchronous Step-Down Regulator | Integrated Power MOSFETs, $4V \le V_{IN} \le 150V$, $0.8V \le V_{OUT} \le V_{IN}$, $I_Q$ = 12µA, MSOP-16 (12) |
| LTC3638 | High Efficiency, 150V 250mA Synchronous Step-Down Regulator | Integrated Power MOSFETs, $4V \le V_{IN} \le 150V$, $0.8V \le V_{OUT} \le V_{IN}$, $I_Q$ = 12µA, MSOP-16 (12) |
| LTC7138 | High Efficiency, 150V 400mA Synchronous Step-Down Regulator | Integrated Power MOSFETs, $4V \le V_{IN} \le 150V$, $0.8V \le V_{OUT} \le V_{IN}$, $I_Q$ = 12µA, MSOP-16 (12) |
| LTC3899 | 60V Triple Output, Buck/Buck/Boost Synchronous Controller with 30µA Burst Mode $I_Q$ | 4.5V(Down to 2.2V After Start-Up) $\le V_{IN} \le$ 60V, Buck $V_{OUT}$ Range: 0.8V to 60V, Boost $V_{OUT}$ Up to 60V |
| LTC7860 | High Efficiency Switching Surge Stopper | $3.5V \le V_{IN} \le 60V$, Expandable to 200V+, Adjustable $V_{OUT}$ Clamp and Current Limit, Power Inductor Improves EMI, MSOP-12 |
| LT8631 | 100V, 1A Synchronous Micropower Step-Down Regulator | Integrated Power MOSFETs, $3V \le V_{IN} \le 100V$, $0.8V \le V_{OUT} \le 60V$, $I_Q$ = 7µA, TSSOP-20(16) |
| LTC3896 | 150V Low $I_Q$, Synchronous Inverting DC/DC Controller | $4V \le V_{IN} \le 140V$, $150V_{PK}$, $-60V \le V_{OUT} \le -0.8V$, Ground-Reference Interface Pins, Adjustable 5V to 10V Gate Drive, $I_Q$ = 40µA |
| LTC3897 | PolyPhase Synchronous Boost Controller with Input/Output Protection and Adjustable Gate Drive Voltage | $4.5V \le V_{IN} \le 65V$, $V_{OUT}$ Up to 60V, $I_Q$ = 55µA Fixed Frequency 50kHz to 900kHz |
| LTC7103 | 105V, 2.3A Low EMI Synchronous Step-Down Regulator | $4.4V \le V_{IN} \le 105V$, $1V \le V_{OUT} \le V_{IN}$, $I_Q$ = 2µA Fixed Frequency 200kHz to 2MHz, 5mm × 6mm QFN |


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