# DRV8300U: 100V Three-Phase BLDC Gate Driver

## 1 Features

- 100V Three Phase Half-Bridge Gate driver
  - Drives N-Channel MOSFETs (NMOS)
  - Gate Driver Supply (GVDD): 5-20V
  - MOSFET supply (SHx) support up to 100V
- Integrated Bootstrap Diodes (DRV8300UD devices)
- Supports Inverting and Non-Inverting INLx inputs
- Bootstrap gate drive architecture
  - 750mA source current
  - 1.5A sink current
- Supports up to 15S battery powered applications
- Higher BSTUV (8V typ) and GVDDUV (7.6V typ) threshold to support standard MOSFETs
- Low leakage current on SHx pins (<55µA)
- Absolute maximum BSTx voltage up to 125V
- Supports negative transients up to -22V on SHx
- Built-in cross conduction prevention
- Adjustable deadtime through DT pin for QFN package variants
- Fixed deadtime insertion of 200nS for TSSOP package variants
- Supports 3.3V and 5V logic inputs with 20V Abs max
- 4nS typical propagation delay matching
- Compact QFN and TSSOP packages
- Efficient system design with Power Blocks
- Integrated protection features
  - BST undervoltage lockout (BSTUV)
  - GVDD undervoltage (GVDDUV)

## 2 Applications

- E-Bikes, E-Scooters, and E-Mobility
- Fans, Pumps, and Servo Drives
- Brushless-DC (BLDC) Motor Modules and PMSM
- Cordless Garden and Power Tools, Lawnmowers
- Cordless Vacuum Cleaners
- Drones, Robotics, and RC Toys
- Industrial and Logistics Robots

## 3 Description

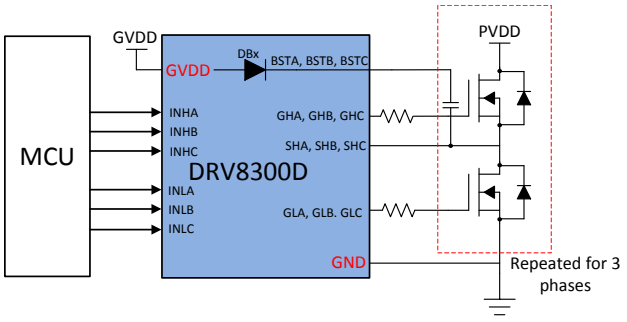
DRV8300U is 100V three half-bridge gate drivers, capable of driving high-side and low-side N-channel power MOSFETs. The DRV8300UD generates the correct gate drive voltages using an integrated bootstrap diode and external capacitor for the high-side MOSFETs. GVDD is used to generate gate drive voltage for the low-side MOSFETs. The Gate Drive architecture supports peak up to 750mA source and 1.5A sink currents.

The phase pins SHx is able to tolerate the significant negative voltage transients; while high side gate driver supply BSTx and GHx is able to support to higher positive voltage transients (125V) abs max voltage which improves robustness of the system. Small propagation delay and delay matching specifications minimize the dead-time requirement which further improves efficiency. Undervoltage protection is provided for both low and high side through GVDD and BST undervoltage lockout.

**Device Information** (1)

| PART NUMBER | PACKAGE | PACKAGE SIZE (NOM)(2) |
|---|---|---|
| DRV8300UDPW | TSSOP (20) | 6.50mm × 6.40mm |
| DRV8300UDIPW | TSSOP (20) | 6.50mm × 6.40mm |
| DRV8300UDRGE | VQFN (24) | 4.00mm × 4.00mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable




**Simplified Schematic for DRV8300UD**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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# 4 Device Comparison Table

| Device Variants | Package | Integrated Bootstrap Diode | GLx polarity with Respect to INLx Input | Deadtime |
|---|---|---|---|---|
| DRV8300UD | 20-Pin TSSOP | Yes | Non-Inverted | Fixed |
| DRV8300UDI | | Yes | Inverted | Fixed |
| DRV8300UD | 24-Pin VQFN | Yes | Non-Inverted or Inverted | Variable |

**Table 4-1. DRV8300 vs DRV8300U comparison**

| Parameters | DRV8300 | DRV8300U |
|---|---|---|
| GVDDUV rising | 4.6V (typ) | 8.3V (typ) |
| GVDDUV falling | 4.35V (typ) | 8V (typ) |
| BSTUV rising | 4.2V (typ) | 8V (typ) |
| BSTUV falling | 4V (typ) | 7.6V(typ) |

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# 5 Pin Configuration and Functions

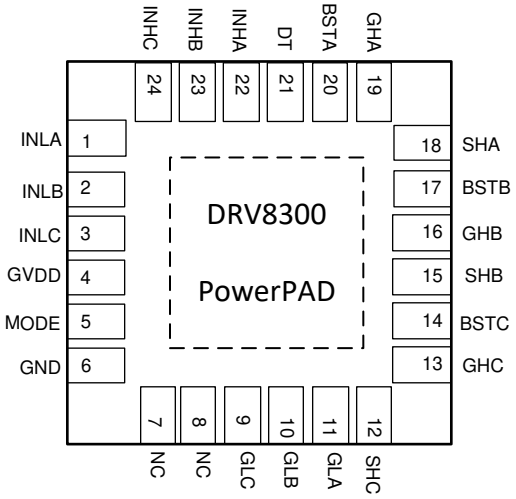


**Figure 5-1. DRV8300UD RGE Package 24-Pin VQFN With Exposed Thermal Pad Top View**

**Table 5-1. Pin Functions—24-Pin DRV8300U Devices**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| BSTA | 20 | O | Bootstrap output pin. Connect capacitor between BSTA and SHA |
| BSTB | 17 | O | Bootstrap output pin. Connect capacitor between BSTB and SHB |
| BSTC | 14 | O | Bootstrap output pin. Connect capacitor between BSTC and SHC |
| DT | 21 | I | Deadtime input pin. Connect resistor to ground for variable deadtime, fixed deadtime when left floating |
| GHA | 19 | O | High-side gate driver output. Connect to the gate of the high-side power MOSFET. |
| GHB | 16 | O | High-side gate driver output. Connect to the gate of the high-side power MOSFET. |
| GHC | 13 | O | High-side gate driver output. Connect to the gate of the high-side power MOSFET. |
| GLA | 11 | O | Low-side gate driver output. Connect to the gate of the low-side power MOSFET. |
| GLB | 10 | O | Low-side gate driver output. Connect to the gate of the low-side power MOSFET. |
| GLC | 9 | O | Low-side gate driver output. Connect to the gate of the low-side power MOSFET. |
| INHA | 22 | I | High-side gate driver control input. This pin controls the output of the high-side gate driver. |
| INHB | 23 | I | High-side gate driver control input. This pin controls the output of the high-side gate driver. |
| INHC | 24 | I | High-side gate driver control input. This pin controls the output of the high-side gate driver. |
| INLA | 1 | I | Low-side gate driver control input. This pin controls the output of the low-side gate driver. |
| INLB | 2 | I | Low-side gate driver control input. This pin controls the output of the low-side gate driver. |
| INLC | 3 | I | Low-side gate driver control input. This pin controls the output of the low-side gate driver. |
| MODE | 5 | I | Mode Input controls polarity of GLx compared to INLx inputs.<br>Mode pin floating: GLx output polarity same(Non-Inverted) as INLx input<br>Mode pin to GVDD: GLx output polarity inverted compared to INLx input |
| NC | 7, 8 | NC | No internal connection. This pin can be left floating or connected to system ground. |
| GND | 6 | PWR | Device ground. |
| SHA | 18 | I | High-side source sense input. Connect to the high-side power MOSFET source. |
| SHB | 15 | I | High-side source sense input. Connect to the high-side power MOSFET source. |
| SHC | 12 | I | High-side source sense input. Connect to the high-side power MOSFET source. |
| GVDD | 4 | PWR | Gate driver power supply input. Connect a X5R or X7R, GVDD-rated ceramic and greater then or equal to 10uF local capacitance between the GVDD and GND pins. |

(1) PWR = power, I = input, O = output, NC = no connection


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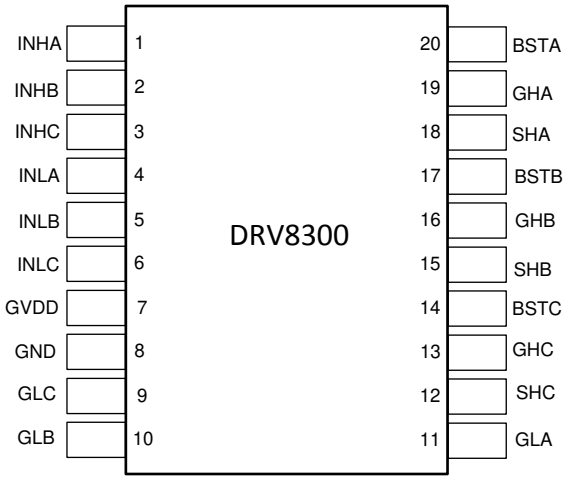


**Figure 5-2. DRV8300UD, DRV8300UDI PW Package 20-Pin TSSOP Top View**

**Table 5-2. Pin Functions—20-Pin DRV8300U Devices**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| BSTA | 20 | O | Bootstrap output pin. Connect capacitor between BSTA and SHA |
| BSTB | 17 | O | Bootstrap output pin. Connect capacitor between BSTB and SHB |
| BSTC | 14 | O | Bootstrap output pin. Connect capacitor between BSTC and SHC |
| GHA | 19 | O | High-side gate driver output. Connect to the gate of the high-side power MOSFET. |
| GHB | 16 | O | High-side gate driver output. Connect to the gate of the high-side power MOSFET. |
| GHC | 13 | O | High-side gate driver output. Connect to the gate of the high-side power MOSFET. |
| GLA | 11 | O | Low-side gate driver output. Connect to the gate of the low-side power MOSFET. |
| GLB | 10 | O | Low-side gate driver output. Connect to the gate of the low-side power MOSFET. |
| GLC | 9 | O | Low-side gate driver output. Connect to the gate of the low-side power MOSFET. |
| INHA | 1 | I | High-side gate driver control input. This pin controls the output of the high-side gate driver. |
| INHB | 2 | I | High-side gate driver control input. This pin controls the output of the high-side gate driver. |
| INHC | 3 | I | High-side gate driver control input. This pin controls the output of the high-side gate driver. |
| INLA | 4 | I | Low-side gate driver control input. This pin controls the output of the low-side gate driver. |
| INLB | 5 | I | Low-side gate driver control input. This pin controls the output of the low-side gate driver. |
| INLC | 6 | I | Low-side gate driver control input. This pin controls the output of the low-side gate driver. |
| GND | 8 | PWR | Device ground. |
| SHA | 18 | I | High-side source sense input. Connect to the high-side power MOSFET source. |
| SHB | 15 | I | High-side source sense input. Connect to the high-side power MOSFET source. |
| SHC | 12 | I | High-side source sense input. Connect to the high-side power MOSFET source. |
| GVDD | 7 | PWR | Gate driver power supply input. Connect a X5R or X7R, GVDD-rated ceramic and greater then or equal to 10uF local capacitance between the GVDD and GND pins. |

1. PWR = power, I = input, O = output, NC = no connection

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Gate driver regulator pin voltage | GVDD | -0.3 | 21.5 | V |
| Bootstrap pin voltage | BSTx | -0.3 | 125 | V |
| Bootstrap pin voltage | BSTx with respect to SHx | -0.3 | 21.5 | V |
| Logic pin voltage | INHx, INLx, MODE, DT | -0.3 | $V_{GVDD}$+0.3 | V |
| High-side gate drive pin voltage | GHx | -22 | 125 | V |
| High-side gate drive pin voltage | GHx with respect to SHx | -0.3 | 22 | V |
| Transient 500-ns high-side gate drive pin voltage | GHx with respect to SHx | -5 | 22 | V |
| Low-side gate drive pin voltage | GLx | -0.3 | $V_{GVDD}$+0.3 | V |
| Transient 500-ns low-side gate drive pin voltage | GLx | -5 | $V_{GVDD}$+0.3 | V |
| High-side source pin voltage | SHx | -22 | 110 | V |
| Ambient temperature, $T_A$ | | –40 | 125 | °C |
| Junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

## 6.2 ESD Ratings Comm

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{GVDD}$ | Power supply voltage | GVDD | 8.7 | | 20 | V |
| $V_{SHx}$ | High-side source pin voltage | SHx | -2 | | 85 | V |
| $V_{SHx}$ | Transient 2µs high-side source pin voltage | SHx | -22 | | 85 | V |
| $V_{BST}$ | Bootstrap pin voltage | BSTx | 5 | | 105 | V |
| $V_{BST}$ | Bootstrap pin voltage | BSTx with respect to SHx | 5 | | 20 | V |
| $V_{IN}$ | Logic input voltage | INHx, INLx, MODE, DT | 0 | | GVDD | V |
| $f_{PWM}$ | PWM frequency | INHx, INLx | 0 | | 200 | kHz |
| $V_{SHSL}$ | Slew rate on SHx pin (DRV8300UD and DRV8300UDI) | | | | 2 | V/ns |
| $C_{BOOT}$ (1) | Capacitor between BSTx and SHx (DRV8300UD and DRV8300UDI) | | | | 1 | µF |
| $T_A$ | Operating ambient temperature | | –40 | | 125 | °C |
| $T_J$ | Operating junction temperature | | –40 | | 150 | °C |

(1) Current flowing through boot diode ($D_{BOOT}$) needs to be limited for $C_{BOOT}$ > 1µF


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## 6.4 Thermal Information

| THERMAL METRIC[1] | | DRV8300U | | UNIT |
|---|---|---|---|---|
| | | PW (TSSOP) | RGE (VQFN) | |
| | | 20 PINS | 24 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 97.4 | 49.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 38.3 | 42.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 48.8 | 26.5 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 4.3 | 2.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 48.4 | 26.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | 11.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

8.7 V ≤ $V_{GVDD}$ ≤ 20 V, –40°C ≤ $T_J$ ≤ 150°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES (GVDD, BSTx)** | | | | | | |
| $I_{GVDD}$ | GVDD standby mode current | INHx = INLX = 0; $V_{BSTx}$ = $V_{GVDD}$ | 400 | 800 | 1400 | µA |
| | GVDD active mode current | INHx = INLX = Switching @20kHz; $V_{BSTx}$ = $V_{GVDD}$; NO FETs connected | 400 | 825 | 1400 | µA |
| $IL_{BSx}$ | Bootstrap pin leakage current | $V_{BSTx}$ = $V_{SHx}$ = 85V; $V_{GVDD}$ = 0V | 2 | 4 | 7 | µA |
| $IL_{BS_TRAN}$ | Bootstrap pin active mode transient leakage current | INHx = Switching@20kHz | 30 | 105 | 220 | µA |
| $IL_{BS_DC}$ | Bootstrap pin active mode leakage static current | INHx = High | 30 | 85 | 150 | µA |
| $IL_{SHx}$ | High-side source pin leakage current | INHx = INLX = 0; $V_{BSTx}$ - $V_{SHx}$ = 12V; $V_{SHx}$ = 0 to 85V | 30 | 55 | 80 | µA |
| **LOGIC-LEVEL INPUTS (INHx, INLx, MODE)** | | | | | | |
| $V_{IL_MODE}$ | Input logic low voltage | Mode pin | | | 0.6 | V |
| $V_{IL}$ | Input logic low voltage | INLx, INHx pins | | | 0.8 | V |
| $V_{IH_MODE}$ | Input logic high voltage | Mode pin | 3.7 | | | V |
| $V_{IH}$ | Input logic high voltage | INLx, INHx pins | 2.0 | | | V |
| $V_{HYS_MODE}$ | Input hysteresis | Mode pin | 1600 | 2000 | 2400 | mV |
| $V_{HYS}$ | Input hysteresis | INLx, INHx pins | 40 | 100 | 260 | mV |
| $I_{IL_INLx}$ | INLx Input logic low current | $V_{PIN}$ (Pin Voltage) = 0 V; INLx in non-inverting mode | -1 | 0 | 1 | µA |
| | | $V_{PIN}$ (Pin Voltage) = 0 V; INLx in inverting mode | 5 | 20 | 30 | µA |
| $I_{IH_INLx}$ | INLx Input logic high current | $V_{PIN}$ (Pin Voltage) = 5 V; INLx in non-inverting mode | 5 | 20 | 30 | µA |
| | | $V_{PIN}$ (Pin Voltage) = 5 V; INLx in inverting mode | 0 | 0.5 | 1.5 | µA |
| $I_{IL}$ | INHx, MODE Input logic low current | $V_{PIN}$ (Pin Voltage) = 0 V; | -1 | 0 | 1 | µA |
| $I_{IH}$ | INHx, MODE Input logic high current | $V_{PIN}$ (Pin Voltage) = 5 V; | 5 | 20 | 30 | µA |
| $R_{PD_INHx}$ | INHx Input pulldown resistance | To GND | 120 | 200 | 280 | kΩ |
| $R_{PD_INLx}$ | INLx Input pulldown resistance | To GND, INLx in non-inverting mode | 120 | 200 | 280 | kΩ |
| $R_{PU_INLx}$ | INLx Input pullup resistance | To INT_5V, INLx in inverting mode | 120 | 200 | 280 | kΩ |
| $R_{PD_MODE}$ | MODE Input pulldown resistance | To GND | 120 | 200 | 280 | kΩ |
| **GATE DRIVERS (GHx, GLx, SHx, SLx)** | | | | | | |

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8.7 V ≤ $V_{GVDD}$ ≤ 20 V, –40°C ≤ $T_J$ ≤ 150°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{GHx_LO}$ | High-side gate drive low level voltage | $I_{GLx}$ = -100 mA; $V_{GVDD}$ = 12V; No FETs connected | 0 | 0.15 | 0.35 | V |
| $V_{GHx_HI}$ | High-side gate drive high level voltage ($V_{BSTx}$ - $V_{GHx}$) | $I_{GHx}$ = 100 mA; $V_{GVDD}$ = 12V; No FETs connected | 0.3 | 0.6 | 1.2 | V |
| $V_{GLx_LO}$ | Low-side gate drive low level voltage | $I_{GLx}$ = -100 mA; $V_{GVDD}$ = 12V; No FETs connected | 0 | 0.15 | 0.35 | V |
| $V_{GLx_HI}$ | Low-side gate drive high level voltage ($V_{GVDD}$ - $V_{GHx}$) | $I_{GHx}$ = 100 mA; $V_{GVDD}$ = 12V; No FETs connected | 0.3 | 0.6 | 1.2 | V |
| $I_{DRIVEP_HS}$ | High-side peak source gate current | GHx-SHx = 12V | 400 | 750 | 1200 | mA |
| $I_{DRIVEN_HS}$ | High-side peak sink gate current | GHx-SHx = 0V | 850 | 1500 | 2100 | mA |
| $I_{DRIVEP_LS}$ | Low-side peak source gate current | GLx = 12V | 400 | 750 | 1200 | mA |
| $I_{DRIVEN_LS}$ | Low-side peak sink gate current | GLx = 0V | 850 | 1500 | 2100 | mA |
| $t_{PD}$ | Input to output propagation delay | INHx, INLx to GHx, GLx; $V_{GVDD}$ = $V_{BSTx}$ - $V_{SHx}$ > 8V; SHx = 0V, No load on GHx and GLx | 70 | 125 | 180 | ns |
| $t_{PD_match}$ | Matching propagation delay per phase | GHx turning OFF to GLx turning ON, GLx turning OFF to GHx turning ON; $V_{GVDD}$ = $V_{BSTx}$ - $V_{SHx}$ > 8V; SHx = 0V, No load on GHx and GLx | -30 | ±4 | 30 | ns |
| $t_{PD_match}$ | Matching propagation delay phase to phase | GHx/GLx turning ON to GHy/GLy turning ON, GHx/GLx turning OFF to GHy/GLy turning OFF; $V_{GVDD}$ = $V_{BSTx}$ - $V_{SHx}$ > 8V; SHx = 0V, No load on GHx and GLx | -30 | ±4 | 30 | ns |
| $t_{R_GLx}$ | GLx rise time (10% to 90%) | $C_{LOAD}$ = 1000 pF; $V_{GVDD}$ = $V_{BSTx}$ - $V_{SHx}$ > 8V; SHx = 0V | 10 | 24 | 50 | ns |
| $t_{R_GHx}$ | GHx rise time (10% to 90%) | $C_{LOAD}$ = 1000 pF; $V_{GVDD}$ = $V_{BSTx}$ - $V_{SHx}$ > 8V; SHx = 0V | 10 | 24 | 50 | ns |
| $t_{F_GLx}$ | GLx fall time (90% to 10%) | $C_{LOAD}$ = 1000 pF; $V_{GVDD}$ = $V_{BSTx}$ - $V_{SHx}$ > 8V; SHx = 0V | 5 | 12 | 30 | ns |
| $t_{F_GHx}$ | GHx fall time (90% to 10%) | $C_{LOAD}$ = 1000 pF; $V_{GVDD}$ = $V_{BSTx}$ - $V_{SHx}$ > 8V; SHx = 0V | 5 | 12 | 30 | ns |
| $t_{DEAD}$ | Gate drive dead time | DT pin floating | 150 | 215 | 280 | ns |
| | | DT pin connected to GND | 150 | 215 | 280 | ns |
| | | 40 kΩ between DT pin and GND | 150 | 200 | 260 | ns |
| | | 400 kΩ between DT pin and GND | 1500 | 2000 | 2600 | ns |
| $t_{PW_MIN}$ | Minimum input pulse width on INHx, INLx that changes the output on GHx, GLx | | 40 | 70 | 150 | ns |
| **BOOTSTRAP DIODES(DRV8300UD, DRV8300UDI)** | | | | | | |
| $V_{BOOTD}$ | Bootstrap diode forward voltage | $I_{BOOT}$ = 100 µA | 0.45 | 0.7 | 0.85 | V |
| | | $I_{BOOT}$ = 100 mA | 2 | 2.3 | 3.1 | V |
| $R_{BOOTD}$ | Bootstrap dynamic resistance ($\Delta V_{BOOTD}/\Delta I_{BOOT}$) | $I_{BOOT}$ = 100 mA and 80 mA | 11 | 15 | 25 | Ω |
| **PROTECTION CIRCUITS** | | | | | | |
| $V_{GVDDUV}$ | Gate Driver Supply undervoltage lockout (GVDDUV) | Supply rising | 8 | 8.3 | 8.6 | V |
| | | Supply falling | 7.8 | 8 | 8.25 | V |
| $V_{GVDDUV_HYS}$ | Gate Driver Supply UV hysteresis | Rising to falling threshold | 295 | 330 | 360 | mV |
| $t_{GVDDUV}$ | Gate Driver Supply undervoltage deglitch time | | 5 | 10 | 13 | µs |


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8.7 V ≤ $V_{GVDD}$ ≤ 20 V, –40°C ≤ $T_J$ ≤ 150°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{BSTUV}$ | Boot Strap undervoltage lockout ($V_{BSTx}$ - $V_{SHx}$) | Supply rising | 7.5 | 8 | 8.7 | V |
| | Boot Strap undervoltage lockout ($V_{BSTx}$ - $V_{SHx}$) | Supply falling | 6.9 | 7.6 | 8.4 | V |
| $V_{BSTUV_HYS}$ | Bootstrap UV hysteresis | Rising to falling threshold | 250 | 400 | 850 | mV |
| $t_{BSTUV}$ | Bootstrap undervoltage deglitch time | | 5.5 | 10 | 22 | µs |

## 6.6 Timing Diagrams

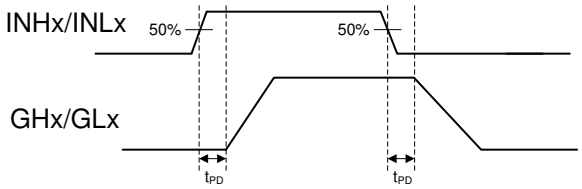


**Figure 6-1. Propagation Delay($t_{PD}$)**

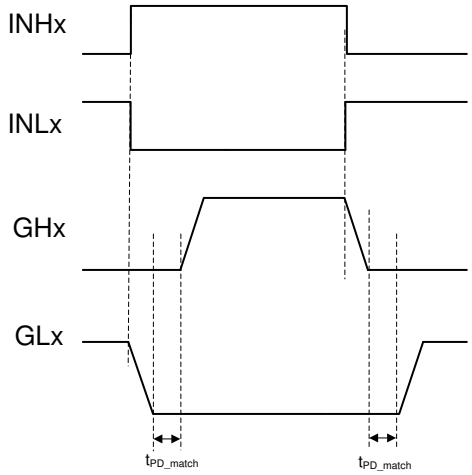


**Figure 6-2. Propagation Delay Match ($t_{PD_match}$)**

## 6.7 Typical Characteristics

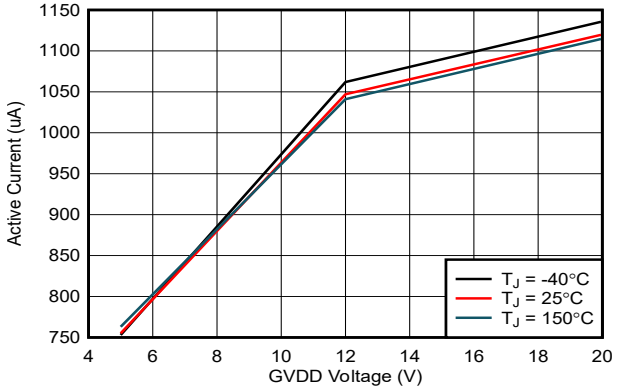


**Figure 6-3. Supply Current Over GVDD Voltage**

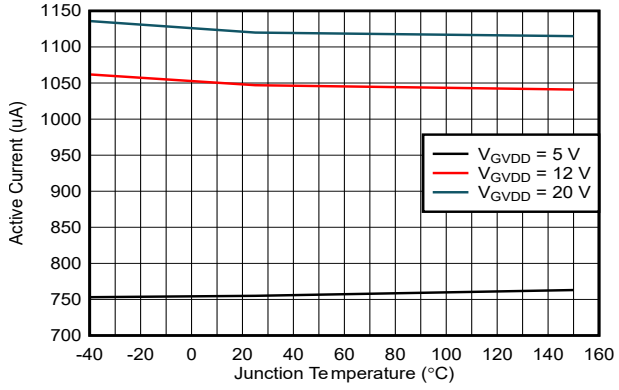


**Figure 6-4. Supply Current Over Temperature**

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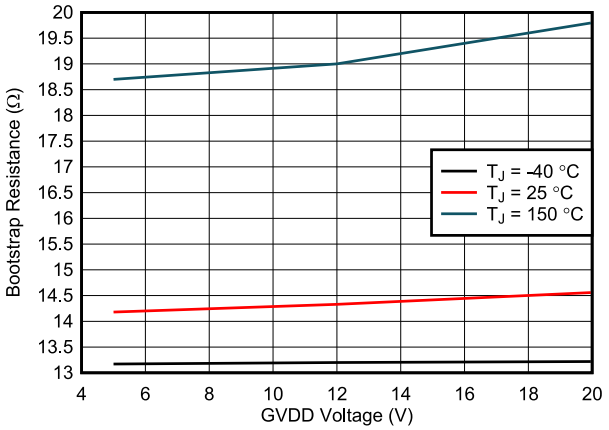


**Figure 6-5. Bootstrap Resistance Over GVDD Voltage**

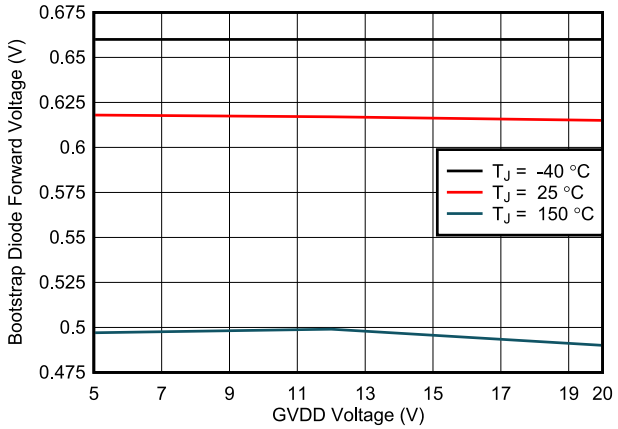


**Figure 6-6. Bootstrap Diode Forward Voltage over GVDD Voltage**


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# 7 Detailed Description

## 7.1 Overview

The DRV8300U family of devices is a gate driver for three-phase motor drive applications. These devices decrease system component count, saves PCB space and cost by integrating three independent half-bridge gate drivers and optional bootstrap diodes.

DRV8300U supports external N-channel high-side and low-side power MOSFETs and can drive 750mA source, 1.5A sink peak currents with total combined 30mA average output current. The DRV8300U family of devices are available in 0.5mm pitch QFN and 0.65mm pitch TSSOP surface-mount packages. The QFN size is 4 × 4mm (0.5mm pin pitch) for the 24-pin package, and TSSOP body size is 6.5 × 4.4mm (0.65mm pin pitch) for the 20-pin package.

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## 7.2 Functional Block Diagram

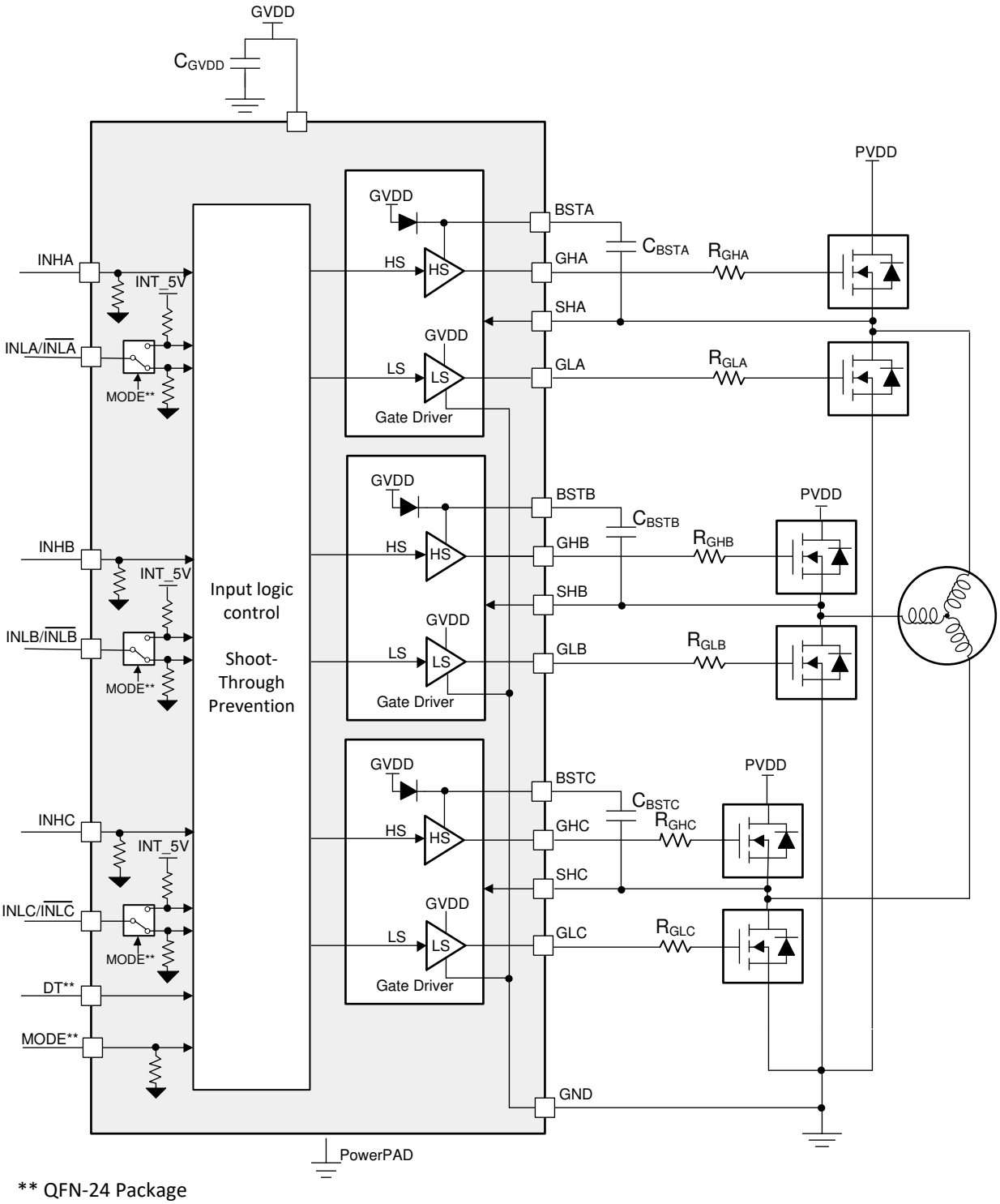


**Figure 7-1. Block Diagram for DRV8300UD**


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## 7.3 Feature Description

### 7.3.1 Three BLDC Gate Drivers

The DRV8300U integrates three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. Input on GVDD provides the gate bias voltage for the low-side MOSFETs. The high voltage is generated using bootstrap capacitor and GVDD supply. The half-bridge gate drivers can be used in combination to drive a three-phase motor or separately to drive other types of loads.

#### 7.3.1.1 Gate Drive Timings

##### 7.3.1.1.1 Propagation Delay

The propagation delay time ($t_{pd}$) is measured as the time between an input logic edge to a detected output change. This time has two parts consisting of the input deglitcher delay and the delay through the analog gate drivers.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. The analog gate drivers have a small delay that contributes to the overall propagation delay of the device.

##### 7.3.1.1.2 Deadtime and Cross-Conduction Prevention

In the DRV8300U, high-side and low-side inputs operate independently, with an exception to prevent cross conduction when high and low side are turned ON at same time. The DRV8300U turns OFF high-side and low-side output to prevent shoot through when the both high-side and low-side inputs are at logic HIGH at same time.

The DRV8300U also provides option to insert additional deadtime to prevent the external high-side and low-side MOSFET from switching on at the same time. In the devices with DT pin (QFN package), deadtime can be linearly adjusted between 200 ns to 2000 ns by configuring resistor value between DT and GND. When the DT pin is left floating, fixed deadtime of 200 nS (typical value) is inserted. The value of resistor can be calculated using Equation 1.

$$R_{DT}\,(k\Omega) = \frac{Deadtime\ (nS)}{5} \tag{1}$$

In the devices without DT pin (TSSOP package), fixed deadtime of 200 ns (typical value) is inserted to prevent high and low side gate output turning ON at same time.

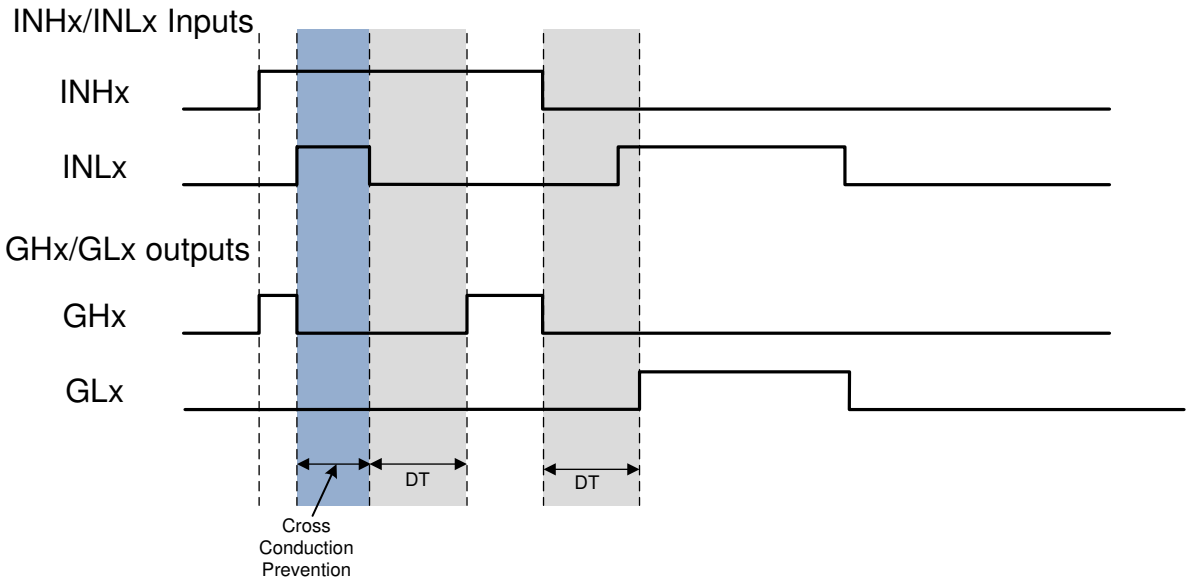


**Figure 7-2. Cross Conduction Prevention and Deadtime Insertion**

#### 7.3.1.2 Mode (Inverting and non inverting INLx)

The DRV8300U has flexibility of accepting different kind of inputs on INLx. In the devices with MODE pin (QFN package), the DRV8300U provides option of configuring the GLx outputs to be inverted or non-inverted compared to polarity of signal on INLx pins. When the MODE pin is left floating, the INLx is configured to be in non-inverting mode and GLx output is in phase with respect to INLx (see Figure 7-3), whereas when the MODE pin is connected to GVDD, GLx output is out of phase with respect to INLx (see Figure 7-4). In devices without MODE pin (TSSOP package device), there are different device option available for inverting and non inverting inputs (see Section 4).

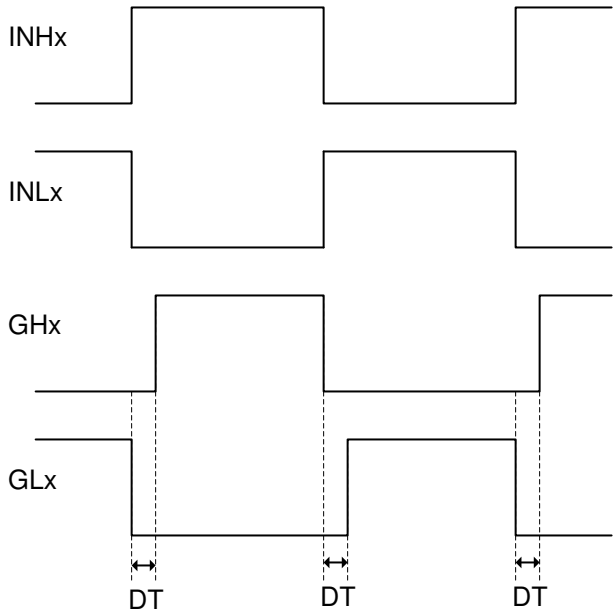


**Figure 7-3. Non-Inverted INLx inputs**

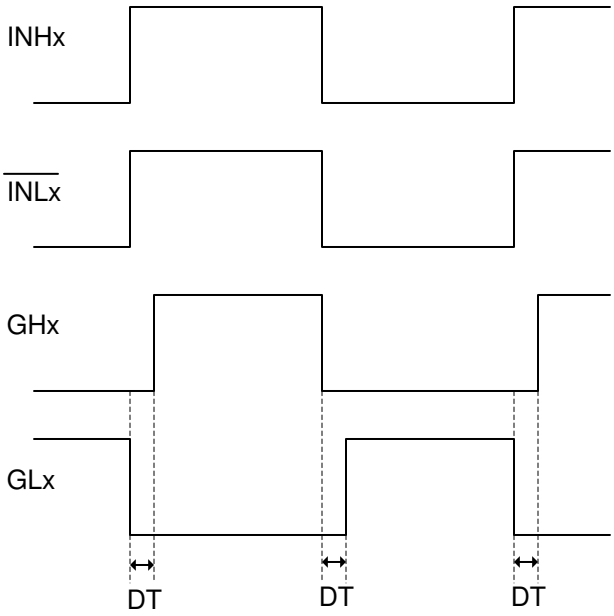


**Figure 7-4. Inverted INLx inputs**


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### 7.3.2 Pin Diagrams

Figure 7-5 shows the input structure for the logic level pins INHx, INLx. INHx and non-inverted INLx has passive pull down, so when inputs are floating the output the gate driver is pulled low. Figure 7-6 shows the input structure for the inverted INLx pins. The inverted INLx has passive pull up, so when inputs are floating the output of the low-side gate driver is pulled low.

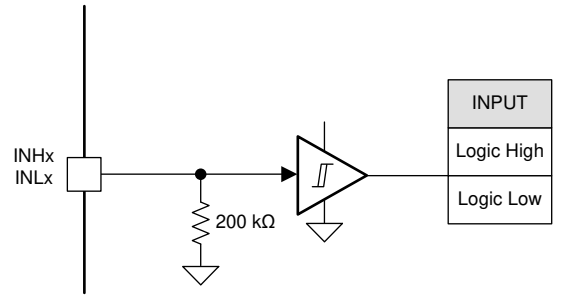


**Figure 7-5. INHx and non-inverted INLx Logic-Level Input Pin Structure**

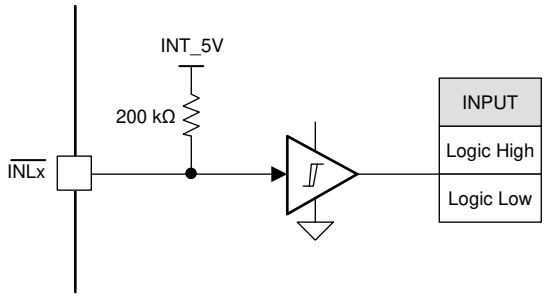


**Figure 7-6. Inverted INLx Logic-Level Input Pin Structure**

### 7.3.3 Gate Driver Protective Circuits

The DRV8300U is protected against BSTx undervoltage and GVDD undervoltage events.

**Table 7-1. Fault Action and Response**

| FAULT | CONDITION | GATE DRIVER | RECOVERY |
|---|---|---|---|
| $V_{BSTx}$ undervoltage (BSTUV) | $V_{BSTx} < V_{BSTUV}$ | GHx - Hi-Z | Automatic: $V_{BSTx} > V_{BSTUV}$ and low to high PWM edge detected on INHx pin |
| GVDD undervoltage (GVDDUV) | $V_{GVDD} < V_{GVDDUV}$ | Hi-Z | Automatic: $V_{GVDD} > V_{GVDDUV}$ |

#### 7.3.3.1 $V_{BSTx}$ Undervoltage Lockout (BSTUV)

The DRV8300U has separate voltage comparator to detect undervoltage condition for each phases. If at any time the voltage on the BSTx pin falls lower than the $V_{BSTUV}$ threshold, high side external MOSFETs of that particular phase is disabled by disabling (Hi-Z) GHx pin. Normal operation starts again when the BSTUV condition clears and low to high PWM edge is detected on INHx input of the same phase that BSTUV condition is detected. BSTUV protection maintains that high-side MOSFETs are not driven when the BSTx pins has lower value.

#### 7.3.3.2 GVDD Undervoltage Lockout (GVDDUV)

If at any time the voltage on the GVDD pin falls lower than the $V_{GVDDUV}$ threshold voltage, all of the external MOSFETs are disabled. Normal operation starts again when the GVDDUV condition clears. GVDDUV protection maintains that external MOSFETs are not driven when the GVDD input is at lower value.

## 7.4 Device Functional Modes

The DRV8300U is in operating (active) mode, whenever the GVDD and BST pins are higher than the UV threshold (GVDD > $V_{GVDDUV}$and $V_{BSTX}$ > $V_{BSTUV}$). In active mode, the gate driver output GHx and GLX follows respective inputs INHx and INLx.

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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The DRV8300U family of devices is primarily used in applications for three-phase brushless DC motor control. The design procedures in the *Section 8.2* section highlight how to use and configure the DRV8300U.


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## 8.2 Typical Application

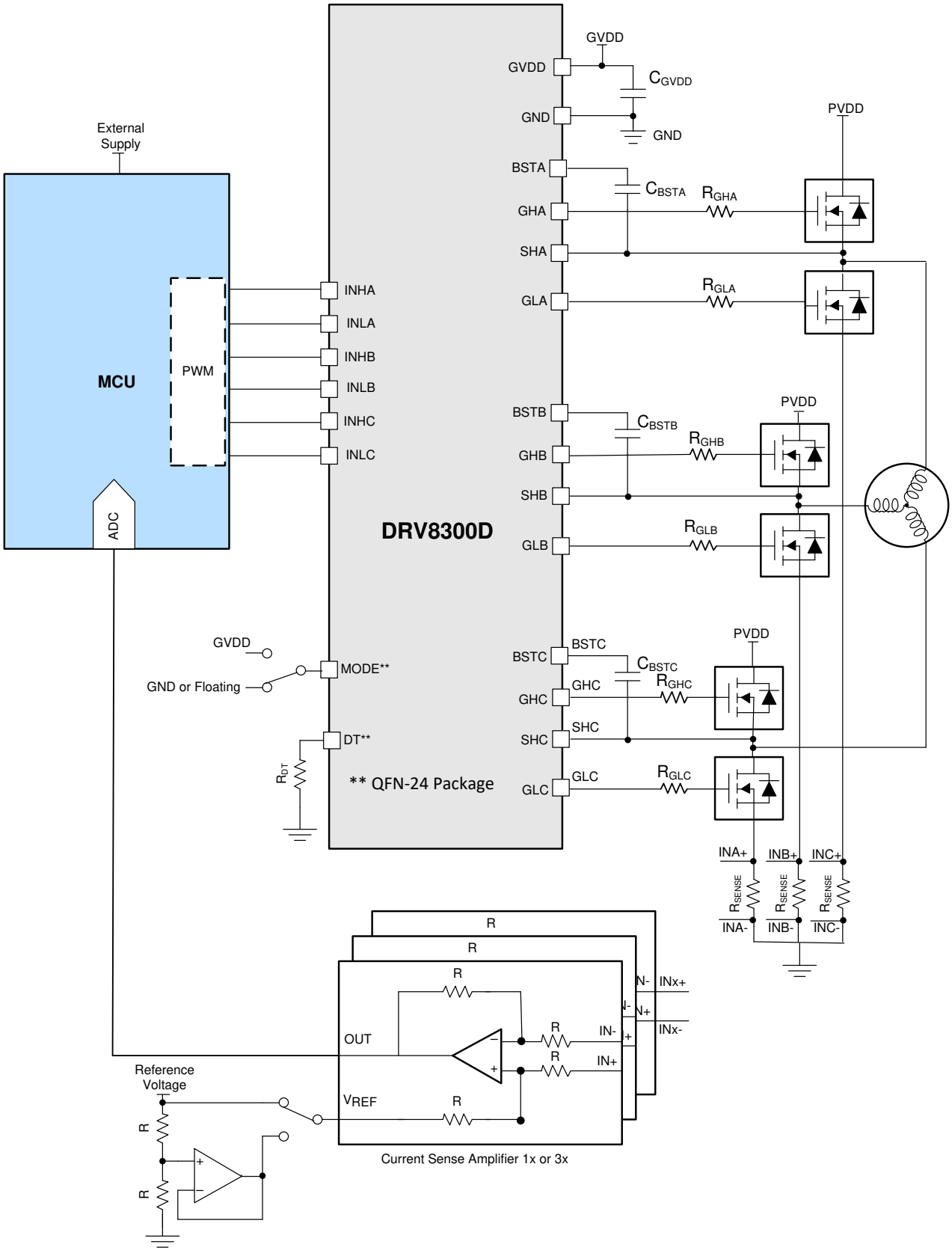


**Figure 8-1. Application Schematic**

### 8.2.1 Design Requirements

Table 8-1 lists the example design input parameters for system design.

**Table 8-1. Design Parameters**

| EXAMPLE DESIGN PARAMETER | REFERENCE | EXAMPLE VALUE |
|---|---|---|
| MOSFET | - | CSD19532Q5B |
| Gate Supply Voltage | $V_{GVDD}$ | 12 V |
| Gate Charge | $Q_G$ | 48 nC |

### 8.2.2 Bootstrap Capacitor and GVDD Capacitor Selection

The bootstrap capacitor must be sized to maintain the bootstrap voltage above the undervoltage lockout for normal operation. Equation 2 calculates the maximum allowable voltage drop across the bootstrap capacitor:

$$\Delta V_{BSTX} = V_{GVDD} - V_{BOOTD} - V_{BSTUV} \quad (2)$$

=12V – 0.85V – 4.5V = 6.65V

where:

- $V_{GVDD}$ is the supply voltage of the gate drive
- $V_{BOOTD}$ is the forward voltage drop of the bootstrap diode
- $V_{BSTUV}$ is the threshold of the bootstrap undervoltage lockout

In this example the allowed voltage drop across bootstrap capacitor is 6.65V. Minimizing ripple voltage as much as possible on both the bootstrap capacitor and GVDD capacitor is generally recommended. Many of commercial, industrial, and automotive applications use ripple value between 0.5V to 1V.

The total charge needed per switching cycle can be estimated with Equation 3:

$$Q_{TOT} = Q_G + \frac{IL_{BS_TRANS}}{f_{SW}} \quad (3)$$

=48nC + 220µA/20kHz = 50nC + 11nC = 59nC

where

- $Q_G$ is the total MOSFET gate charge
- $I_{LBS_TRAN}$ is the bootstrap pin leakage current
- $f_{SW}$ is the is the PWM frequency

The minimum bootstrap capacitor an then be estimated as below assuming 1V $\Delta V_{BSTx}$:

$$C_{BST_MIN} = {Q_{TOT}}/{\Delta V_{BSTX}} \quad (4)$$

= 59nC / 1V = 59nF

The calculated value of minimum bootstrap capacitor is 59nF. Note that, this value of capacitance is needed at full bias voltage. In practice, the value of the bootstrap capacitor must be greater than the calculated value to allow for situations where the power stage skip pulses due to various transient conditions. TI recommends to use a 100nF bootstrap capacitor in this example. TI recommends to include enough margin and place the bootstrap capacitor as close to the BSTx and SHx pins as possible.

$$C_{GVDD} \geq 10 \times C_{BSTX} \quad (5)$$

= 10*100nF= 1µF


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For this example application choose 1µF $C_{GVDD}$ capacitor. Choose a capacitor with a voltage rating at least twice the maximum voltage that the capacitor is exposed to because most ceramic capacitors lose significant capacitance when biased. This value also improves the long term reliability of the system.

### *8.2.3 Application Curves*

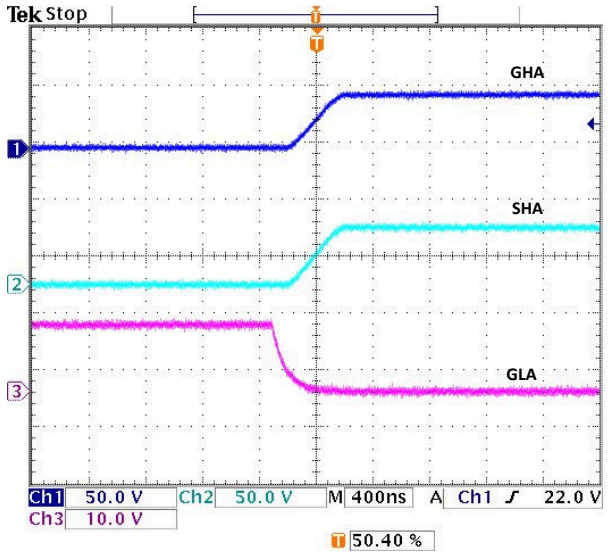


**Figure 8-2. Gate voltages, SHx rising with 15 ohm gate resistor and CSD19532Q5B MOSFET**

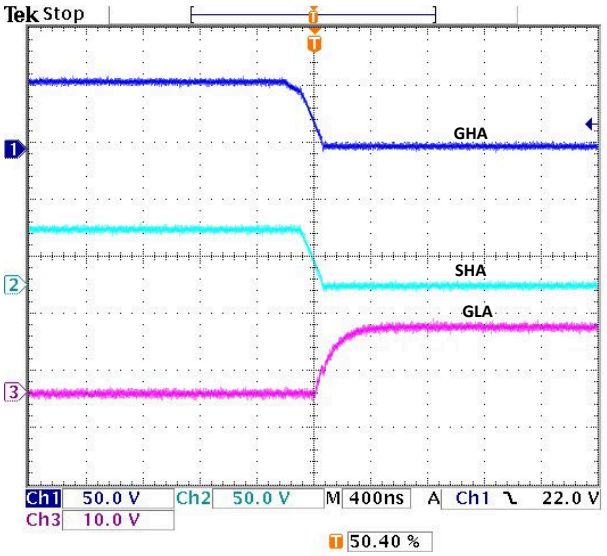


**Figure 8-3. Gate voltages, SHx falling with 15 ohm gate resistor and CSD19532Q5B MOSFET**

## 8.3 Power Supply Recommendations

The DRV8300U is designed to operate from an input voltage supply (GVDD) range from 4.8V to 20V. A local bypass capacitor is placed between the GVDD and GND pins. This capacitor is located as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. TI recommends to use two capacitors across GVDD and GND: a low capacitance ceramic surface-mount capacitor for high frequency filtering placed very close to GVDD and GND pin, and another high capacitance value surface mount capacitor for device bias requirements. In a similar manner, the current pulses delivered by the GHx pins are sourced from the BSTx pins. Therefore, capacitor across the BSTx to SHx is recommended, this capacitor is high enough capacitance value capacitor to deliver GHx pulses

## 8.4 Layout

### *8.4.1 Layout Guidelines*

- Low ESR/ESL capacitors must be connected close to the device between GVDD and GND and between BSTx and SHx pins to support high peak currents drawn from GVDD and BSTx pins during the turn-on of the external MOSFETs.
- To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the high side MOSFET drain and ground.
- To avoid large negative transients on the switch node (SHx) pin, the parasitic inductances between the source of the high-side MOSFET and the source of the low-side MOSFET must be minimized.
- To avoid unexpected transients, the parasitic inductance of the GHx, SHx, and GLx connections must be minimized. Minimize the trace length and number of vias wherever possible. Minimum 10 mil and typical 15 mil trace width is recommended.
- Resistance between DT and GND must be place as close as possible to device
- Place the gate driver as close to the MOSFETs as possible. Confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area by reducing trace length. This confinement decreases the loop inductance and minimize noise issues on the gate terminals of the MOSFETs.

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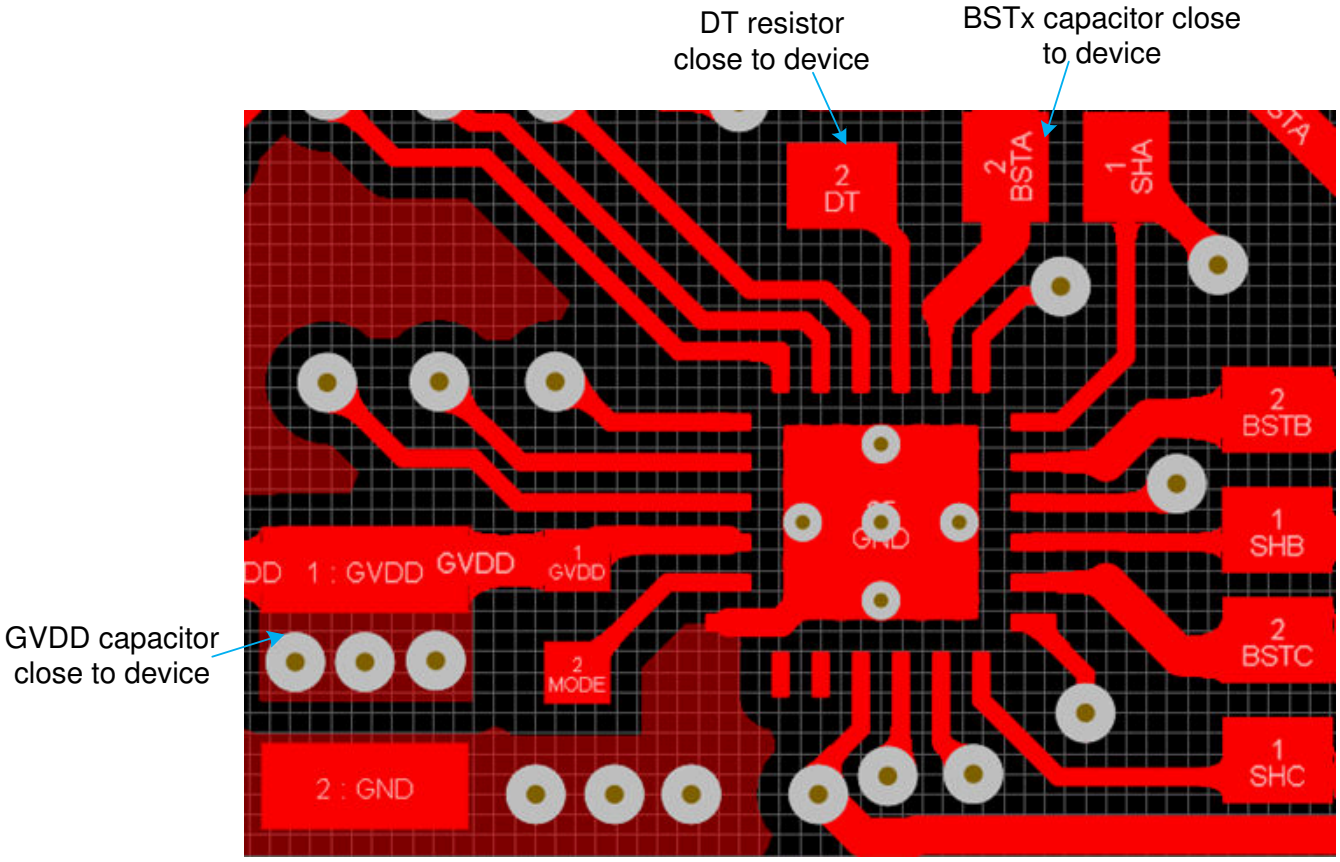
- In QFN package device variants, NC pins can be connected to GND to increase ground connection between thermal pad and external ground plane.
- Refer to sections *General Routing Techniques and MOSFET Placement and Power Stage Routing* in Application Report

### *8.4.2 Layout Example*





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# 9 Device and Documentation Support

## 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (October 2022) to Revision B (June 2025) | Page |
|---|---|
| • Removed "Preview" status from PW devices | 1 |
| • Updated GLx polarity with respect to INLx input for DRV8300UD and DRV8300UDI | 3 |

| Changes from Revision * (July 2022) to Revision A (October 2022) | Page |
|---|---|
| • Updated device status to Production Data | 1 |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| DRV8300UDIPWR | Active | Production | TSSOP (PW) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 8300UDI |
| DRV8300UDIPWR.A | Active | Production | TSSOP (PW) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 8300UDI |
| DRV8300UDPWR | Active | Production | TSSOP (PW) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 8300UD |
| DRV8300UDPWR.A | Active | Production | TSSOP (PW) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 8300UD |
| DRV8300UDRGER | Active | Production | VQFN (RGE) \| 24 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 8300UD |
| DRV8300UDRGER.A | Active | Production | VQFN (RGE) \| 24 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 8300UD |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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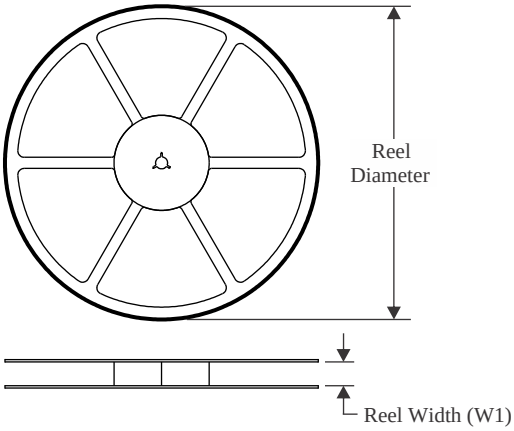
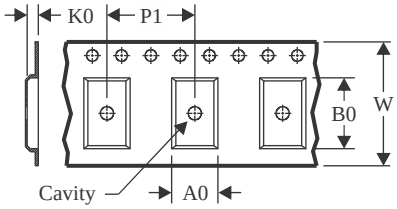
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

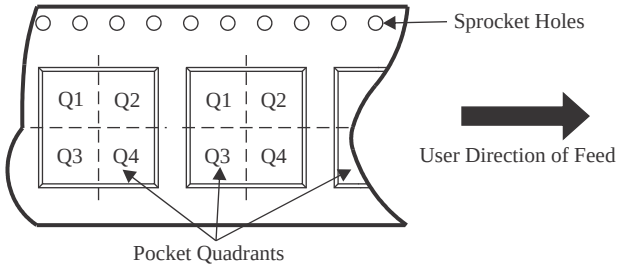



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

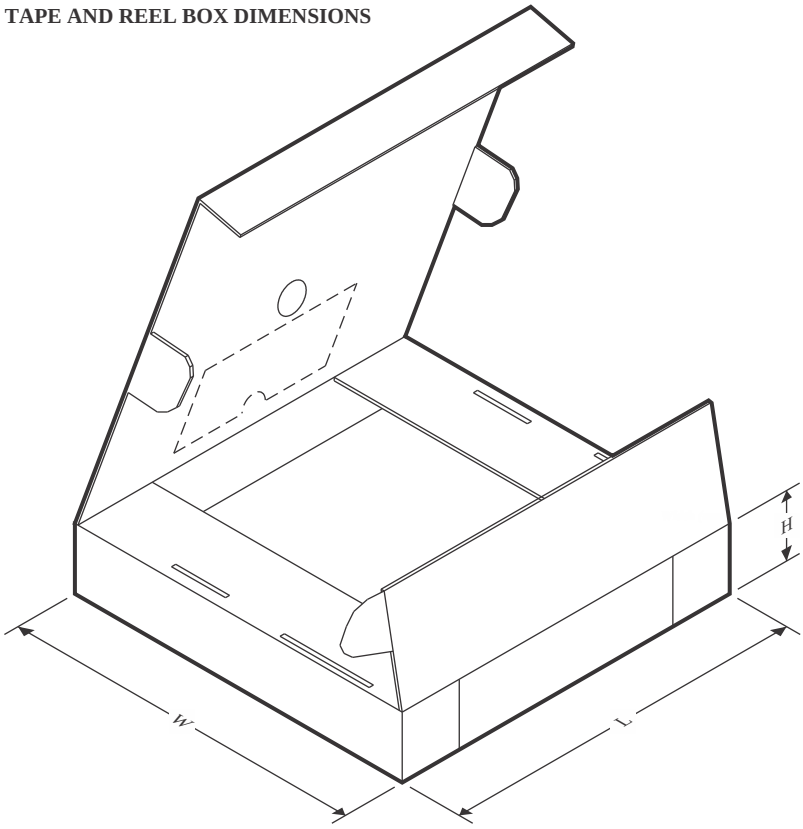
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8300UDIPWR | TSSOP | PW | 20 | 3000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| DRV8300UDPWR | TSSOP | PW | 20 | 3000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| DRV8300UDRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

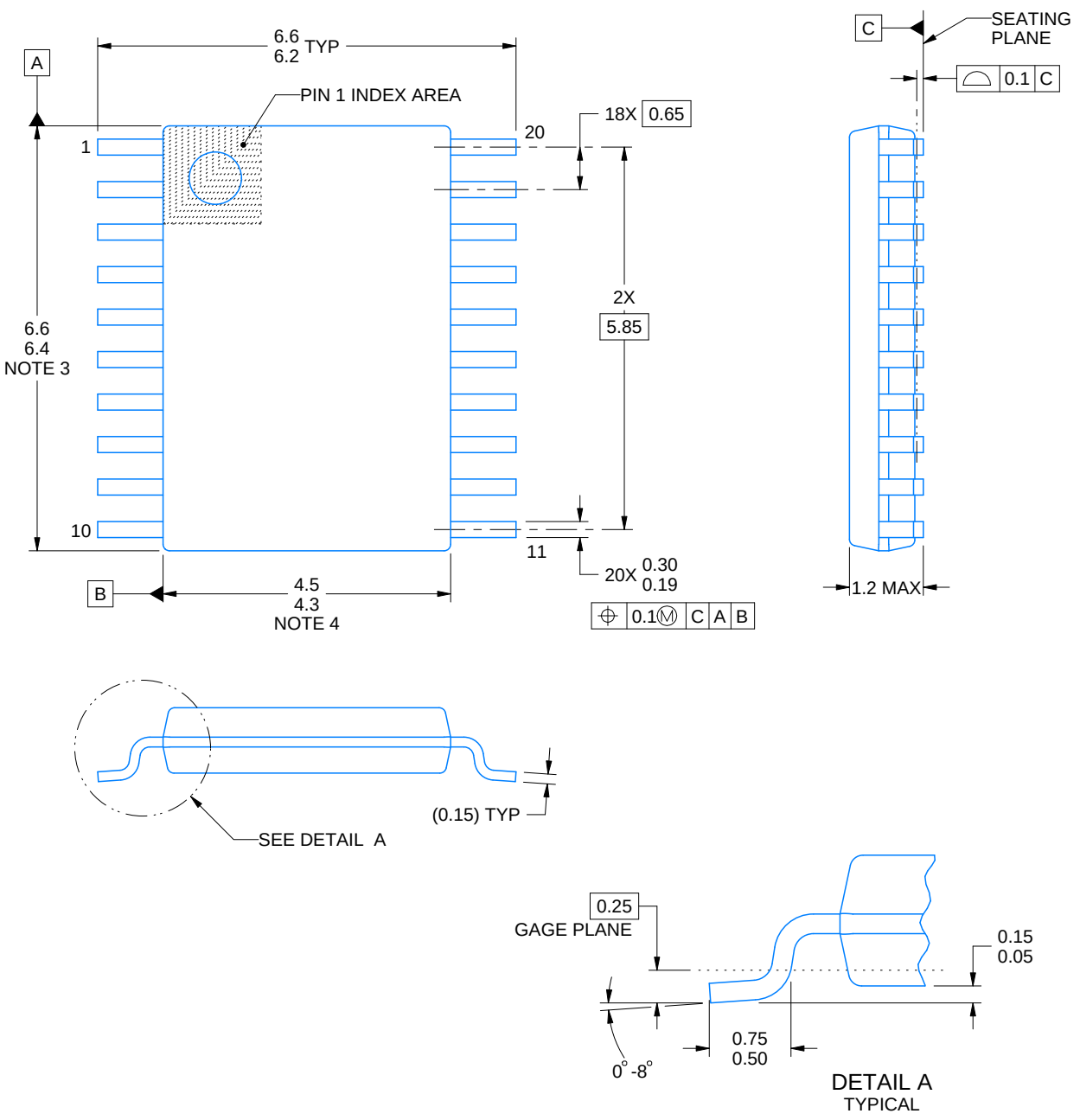
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV8300UDIPWR | TSSOP | PW | 20 | 3000 | 353.0 | 353.0 | 32.0 |
| DRV8300UDPWR | TSSOP | PW | 20 | 3000 | 353.0 | 353.0 | 32.0 |
| DRV8300UDRGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |

# PACKAGE OUTLINE

## PW0020A

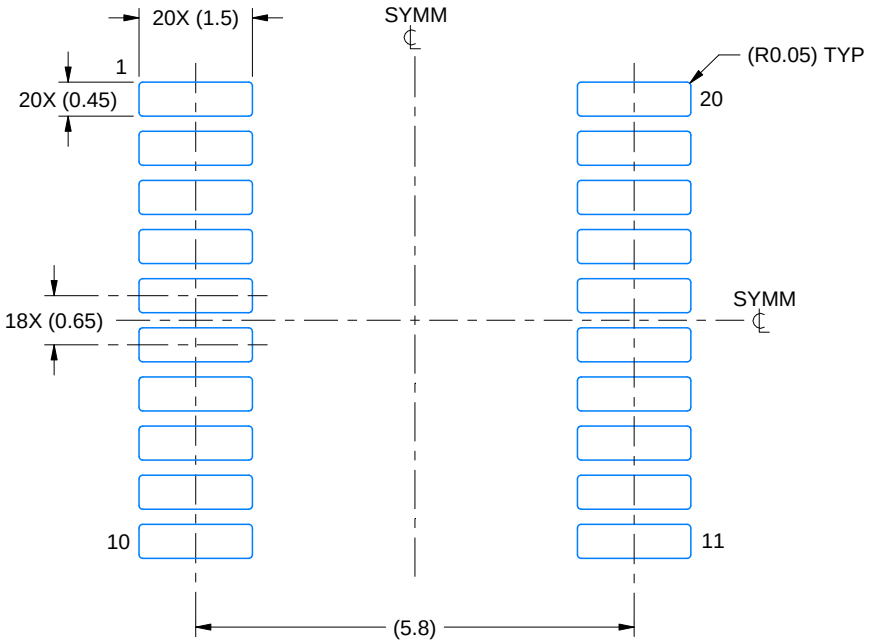
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

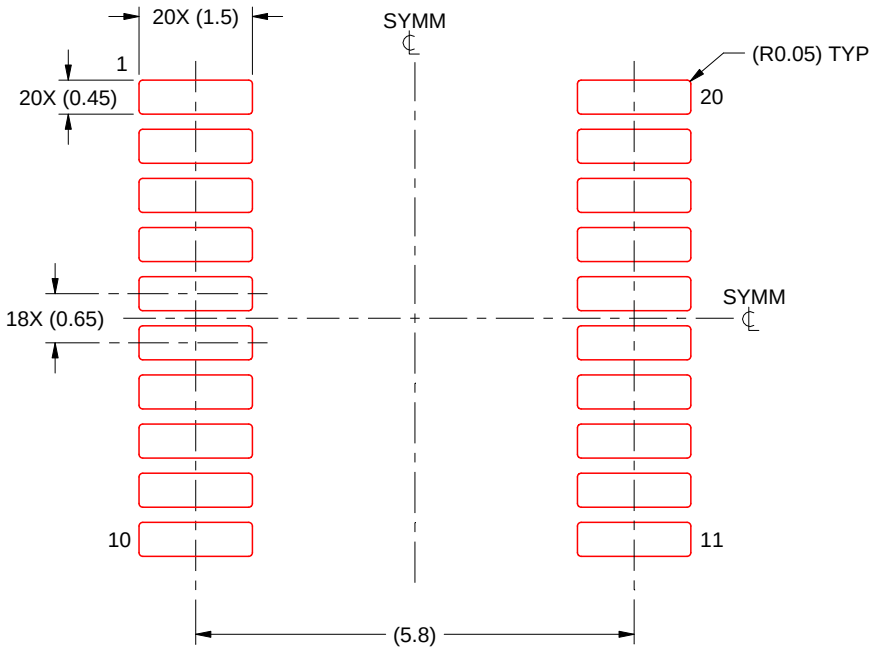



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

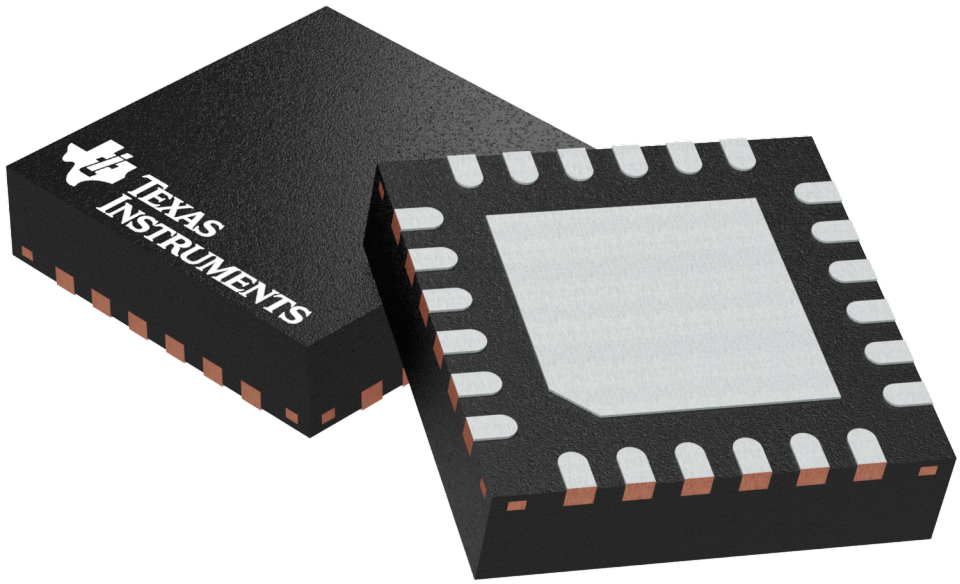
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

## RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

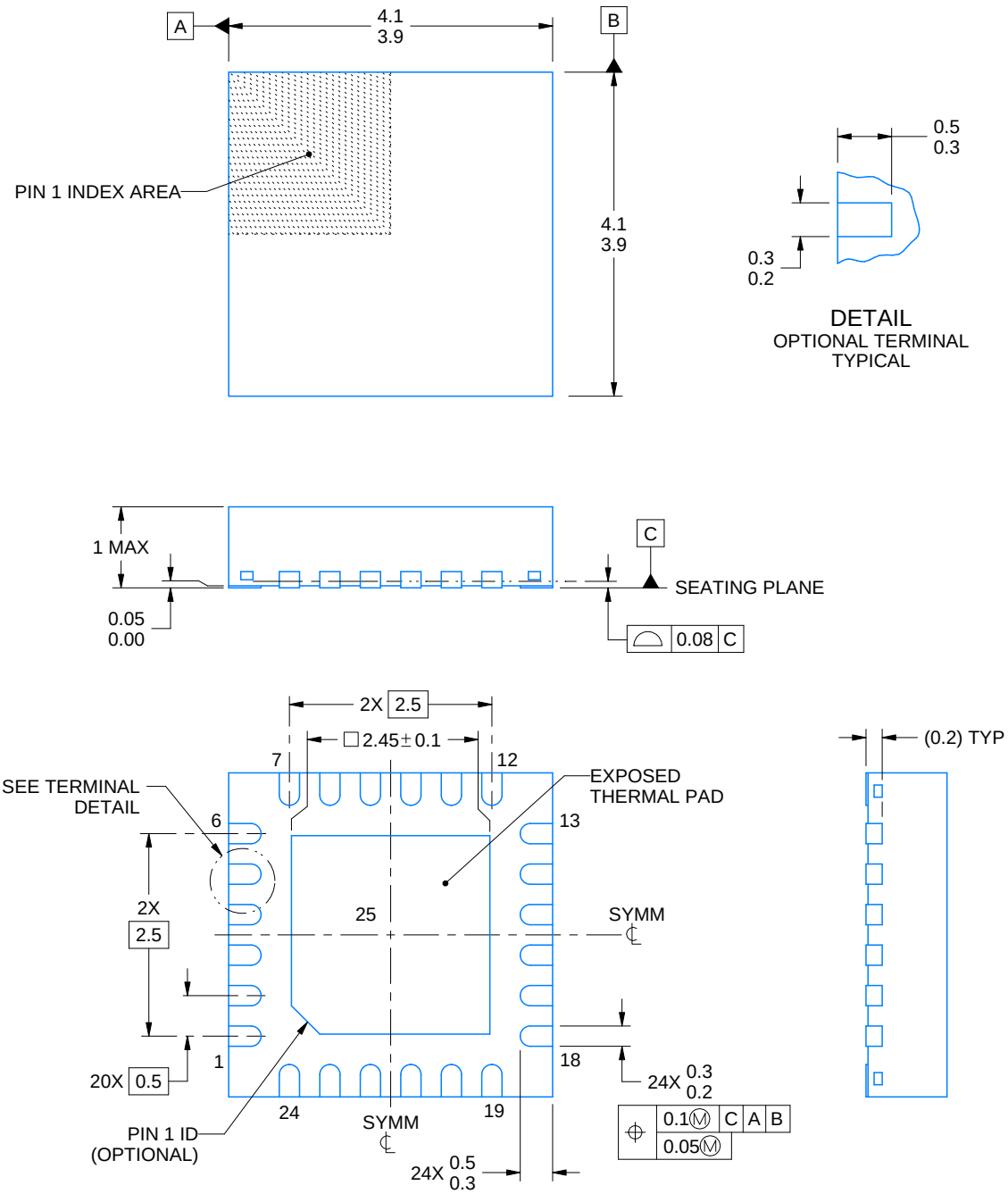
4204104/H

# PACKAGE OUTLINE

## RGE0024B

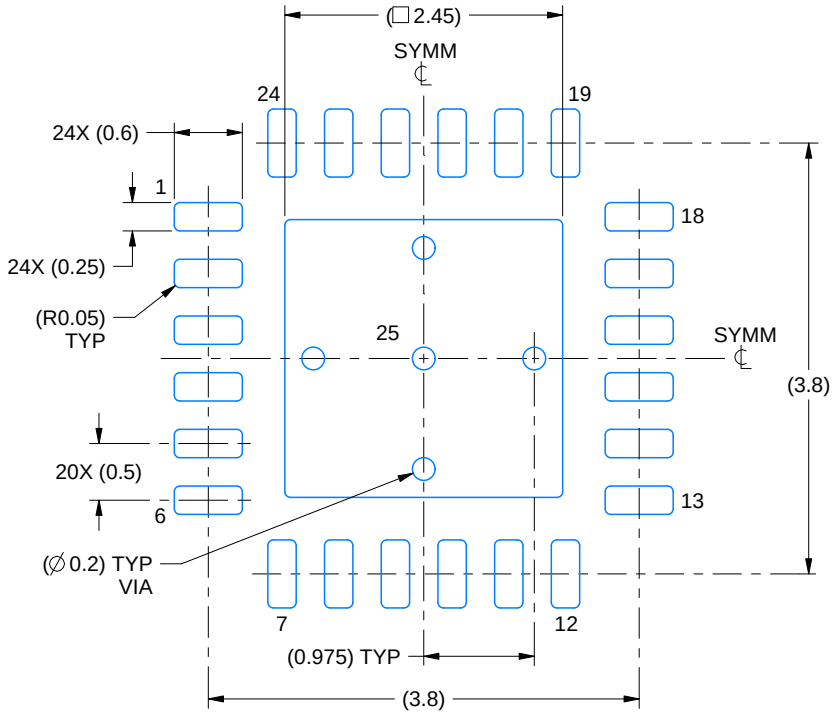
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

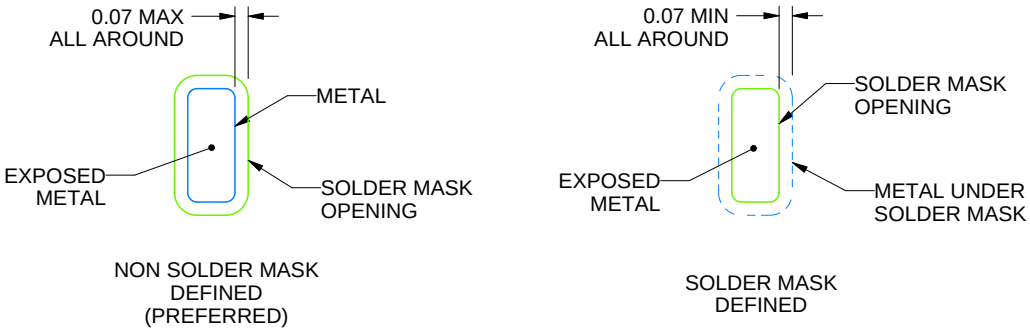



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

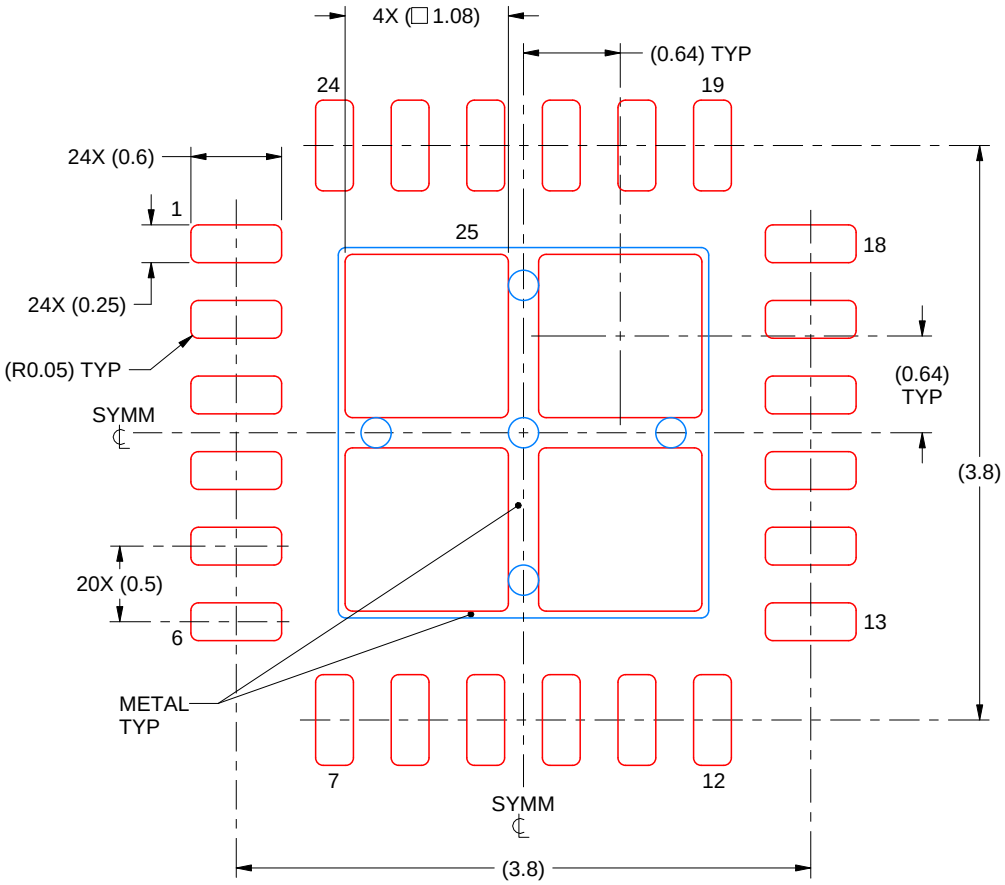



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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