GXA3485

2.7V-5V Powered, ±15kV HBM ESD-Protected, 12Mbps RS-485/RS-422 Transceivers

Datasheet_V1.2
Apr. 2025

1 Features

- Support 2.7V-5V power supply
- Guaranteed 12Mbps data rate
- Low-current shutdown mode
- -7V to +12V common-mode input voltage range
- Half-duplex, allowing up to 256 transceivers to be connected to the bus
- Driver short-circuit overcurrent protection
- RS-485 I/O pin ESD protection : ±15kV HBM
- Package Information：

PART NUMBER	PACKAGE	BODY SIZE (mm^2)
GXA3485D	DFN-8	3.00 × 3.00
GXA3485Z	SOP-8	3.90 × 4.90

2 Applications

- Industrial control
- Communications
- Local area network
- Transceivers for applications sensitive to electromagnetic interference
- Encoder interface

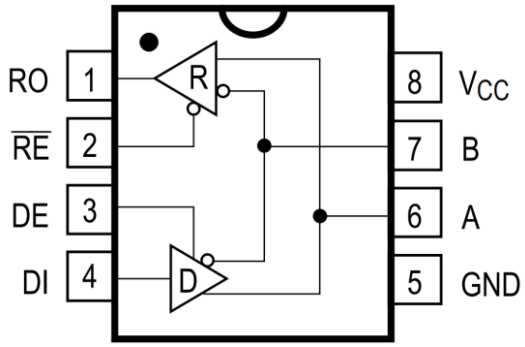
3 Description

The GXA3485 is a low power transceiver for ±15kV electrostatic discharge (ESD) protection for RS-485 and RS-422 communications, supporting a voltage range of 2.7V-5V. Each device contains a driver and a receiver. Transfer rates up to 12Mbps.

Drivers are short-circuit current limited. The receiver input has a fail-safe feature that guarantees a logic-high output if both inputs are open circuit.

The GXA3485 supports SOP-8, MSOP-8, and DFN-8 packages. The GXA3485 is designed for half-duplex communication with 1/8 unit load, allowing up to 256 GXA3485 transceivers to be connected to the same bus. Data transmission up to 12Mbps can be achieved.

Figure 1 The Block Diagram of GXA3485



Copyright © 2025 Beijing Galaxy-CAS Technology Co., Ltd.

Table of Contents

1 Features 1
2 Applications 1
3 Description 1
4 Revision History 2
5 Pin Configuration and Functions 3
6 Specifications 4
6.1 Absolute Maximum Ratings 4
6.2 Electrostatic Protection 4
6.3 Recommended Operating Conditions 4
6.4 Electrical Characteristics 4
6.5 Driver Switching Characteristics 6
6.6 Receiver Switching Characteristics 6
6.7 Test circuit 8
7 Function Tables 11
8 Application Information 11
9 Package Information 14
9.1 DFN-8 14
9.2 SOP-8 15
9.3 Reel and Tape Information 16
10 Ordering Information 17

4 Revision History

V1.2（Apr. 2025）

- Revise the SOP8 package dimensions.（见Section 9.2）.

V1.1（Jan. 2025）

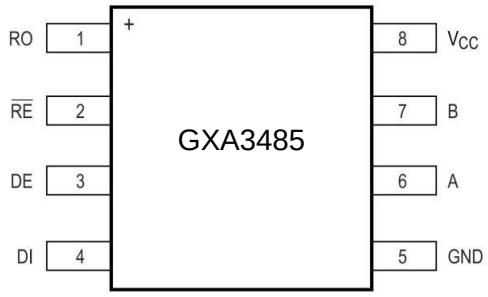
- Update some parameters of the Driver Switching Characteristics（see Section 6.5）;
- Update some parameters of the Receiver Switching Characteristics（see Section 6.6）.

V1.0（Jan. 2025）

- Original version.

5 Pin Configuration and Functions

DFN-8 Top View



Pin Function

PIN		DESCRIPTION
NAME	NO.	
RO	1	Receiver output.
REN	2	Receiver Output Enable. RO is enabled when REN is low; RO is high impedance when REN is high. If REN is high and DE is low, the device will enter a low-power shutdown mode.
DE	3	Driver Output Enable.They are high impedance when DE is low. If the driver output enablement is high, these devices are used as drivers; They are used as receivers when they are in a high impedance state and REN is low.
DI	4	Driver Input. A low on DI forces output A low and output B high. Similarly, a high on DI forces output A high and output B low.
GND	5	Ground.
A	6	Noninverting Receiver Input and Noninverting Driver Output.
B	7	Inverting Receiver Input and Inverting Driver Output.
VDD	8	Supply voltage pin. The voltage range is 2.7V~5V.

6 Specifications

6.1 Absolute Maximum Ratings

	MIN	MAX	UNIT
Power Supply Voltage VDD		6	V
DE、REN、Driver Input Voltage DI、Receiver Output Voltage RO	-0.3	VDD+0.3V	V
Bus Input and Output VoltageA、B	-10	15	V
Operating Conditions	-40	125	℃
Junction Temperature		150	℃
Storage Temperature	-60	150	℃

Unless otherwise noted, the specifications in the above table apply within the atmospheric temperature range. Stresses beyond the range may cause permanent damage to the device.

6.2 Electrostatic Protection

		Value	UNIT
Electrostatic Discharge Voltage V_{ESD} of A or B port	Human Body Mode (HBM), per ANSI/ESDA/JEDEC JS-001	±15000	V
All ports	Human Body Mode (HBM)	±8000	V

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V+	2.7		5	V
Operating Temperature T_A	-40		125	℃

Unless otherwise noted, the specifications in the above table apply within the atmospheric temperature range.

6.4 Electrical Characteristics

Unless otherwise specified, the following data are the characteristics of the chip at + 25 ℃ and the power supply voltage is in the range of 2.7V~5.5V.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential Driver Output	V_{OD}	R_L=54Ω（RS-485），figure 2	1.4			V
		R_L=100Ω（RS-422），figure 2	1.8			V
Change in Magnitude of Driver Diferential Output Voltage	ΔV_{OD}	R_L=54Ω or 100Ω，figure 2			0.2	V

(continued)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver Common-Mode Output Voltage	V_{OC}	R_L=54Ω or 100Ω，figure 2			V_{DD}/2	3	V
Change in Magnitude of Common-Mode Output Voltage	ΔV_{OC}	R_L=54Ω or 100Ω，figure 2				0.2	V
Input High Voltage	V_{IH}	DE，REN，DI		2			V
Input Low Voltage	V_{IL}	DE，REN，DI				0.8	V
Logic Input Current	I_{IN1}	DE，REN，DI		-2		2	μA
Input Current (A, B)	I_{IN2}	DE=0V，V_{DD}=0V或3.3V，V_{IN2}=12V				100	μA
		DE=0V，V_{DD}=0V或3.3V，V_{IN2}=-7V		-80			
Receiver Differential Threshold Voltage	V_{TH}	-7V≤V_{CM}≤12V		-200		-10	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM}=0V			40		mV
Receiver Output High Voltage	V_{OH}	I_{OUT}=-1.5mA，V_{ID}=200mV		V_{DD} - 0.4V			V
Receiver Output Low Voltage	V_{OL}	I_{OUT}=2.5mA，V_{ID}=200mV				0.4	V
Three-State Output Current at Receiver	I_{OZR}	V_{DD}=3.6V，0 ≤ V_{OUT} ≤ V_{DD}				±1	μA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		96			kΩ
Supply Voltage Range	V_{DD}			2.7		5	V
Supply Current	I_{CC}	No load, DI=0 or V_{DD}	DE=0，REN=0		0.23	0.3	mA
			DE=V_{DD}，EN=V_{DD}		0.25	0.3	
Supply Current in Shutdown Mode	I_{SHDN}	DI=0或V_{DD}，DE=0，REN=V_{DD}			0.1	2	μA
Driver Short-Circuit Output Current	I_{OSD}	V_{OUT}=12V				250	mA
		V_{OUT}=-7V				-250	
Receiver Short-Circuit Output Current	I_{OSR}	0 ≤ V_{RO} ≤ V_{DD}		±8		±60	mA

6.5 Driver Switching Characteristics

Unless otherwise specified, the following data are the characteristics of the chip at + 25 ℃ and the power supply voltage is in the range of 2.7V~5.5V.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Data Rate			12			Mbps
Driver Output Delay	t_{DPLH}	R_L=54Ω， C_L=50pF, figure 3、 figure 4		20	40	ns
	t_{DPHL}			20	40	
Driver Differential Output Transition Time	t_{HL},t_{LH}	R_L=54Ω， C_L=50pF, figure 3、 figure 4		10	20	ns
$\|t_{DPLH} - t_{DPHL}\|$	t_{DSKEW}	R_L=54Ω， C_L=50pF, figure 3、 figure 4		1	8	ns
Driver-Output Enable Time to Low Level	t_{DZL}	R_L=54Ω， C_L=50pF, figure 5、 figure 6		20	60	ns
Driver-Output Enable Time to High Level	t_{DZH}	R_L=54Ω， C_L=50pF, figure 5、 figure 6		20	60	ns
Driver-Output Disable Time from High Level	t_{DHZ}	R_L=54Ω， C_L=50pF, figure 5、figure 6		35	80	ns
Driver-Output Disable Time from Low Level	t_{DLZ}	R_L=54Ω， C_L=50pF, figure 5、 figure 6		25	80	ns
Driver-Output Enable Time from Shutdown to Low Level	$t_{DZL(SHDN)}$	R_L=54Ω， C_L=50pF, figure 5、figure 6			100	ns
Driver-Output Enable Time from Shutdown to High Level	$t_{DZH(SHDN)}$	R_L=54Ω， C_L=50pF, figure 5、figure 6			100	ns

6.6 Receiver Switching Characteristics

Unless otherwise specified, the following data are the characteristics of the chip at + 25 ℃ and the power supply voltage is in the range of 2.7V~5.5V.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Time to Shutdown	t_{SHDN}	DE=0,REN=1	50		300	ns
Receiver Propagation Delay, Low-to-High Level	t_{RPLH}	C_L=15pF, figure 7		65	120	ns
Receiver Propagation Delay, High-to-Low Level	t_{RPHL}	C_L=15pF, figure 7		65	120	ns
$\|t_{RPLH} - t_{RPHL}\|$	t_{RSKEW}	C_L=15pF, figure 7		3	10	ns

(continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver Output Enable Time to Low Level	t_{RZL}	R_L=1kΩ，C_L=15pF, figure 8		15	40	ns
Receiver Output Enable Time to High Level	t_{RZH}	R_L=1kΩ，C_L=15pF, figure 8		15	40	ns
Receiver Output Disable Time from High Level	t_{RHZ}	R_L=1kΩ，C_L=15pF, figure 8		10	40	ns
Receiver Output Disable Time from Low Level	t_{RLZ}	R_L=1kΩ，C_L=15pF, figure 8		10	40	ns
Receiver Output Enable Time from Shutdown to Low Level	$t_{RZL(SHDN)}$	R_L=1kΩ，C_L=15pF, figure 8		400	1200	ns
Receiver Output Enable Time from Shutdown to High Level	$t_{RZH(SHDN)}$	R_L=1kΩ，C_L=15pF, figure 8		400	1200	ns

6.7 Test circuits

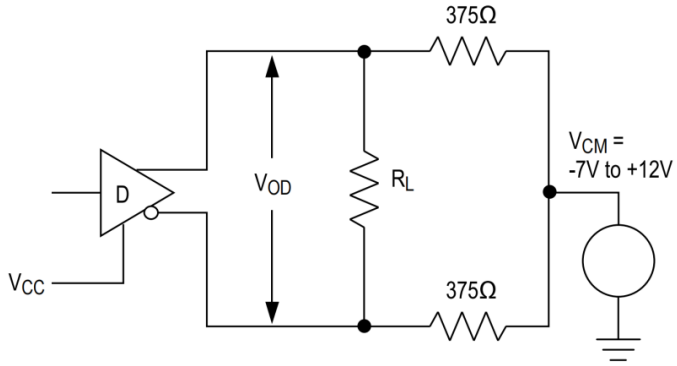


Figure 2 Driver DC test circuit

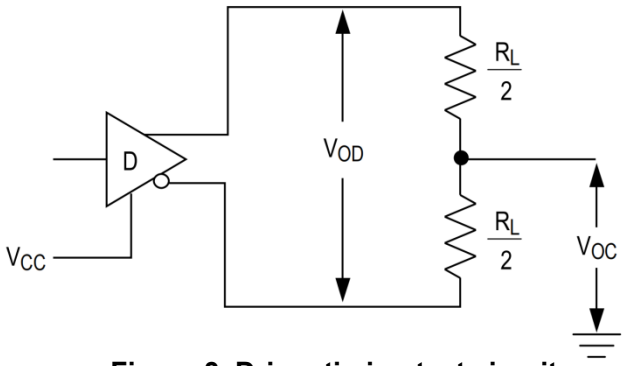


Figure 3. Driver timing test circuit

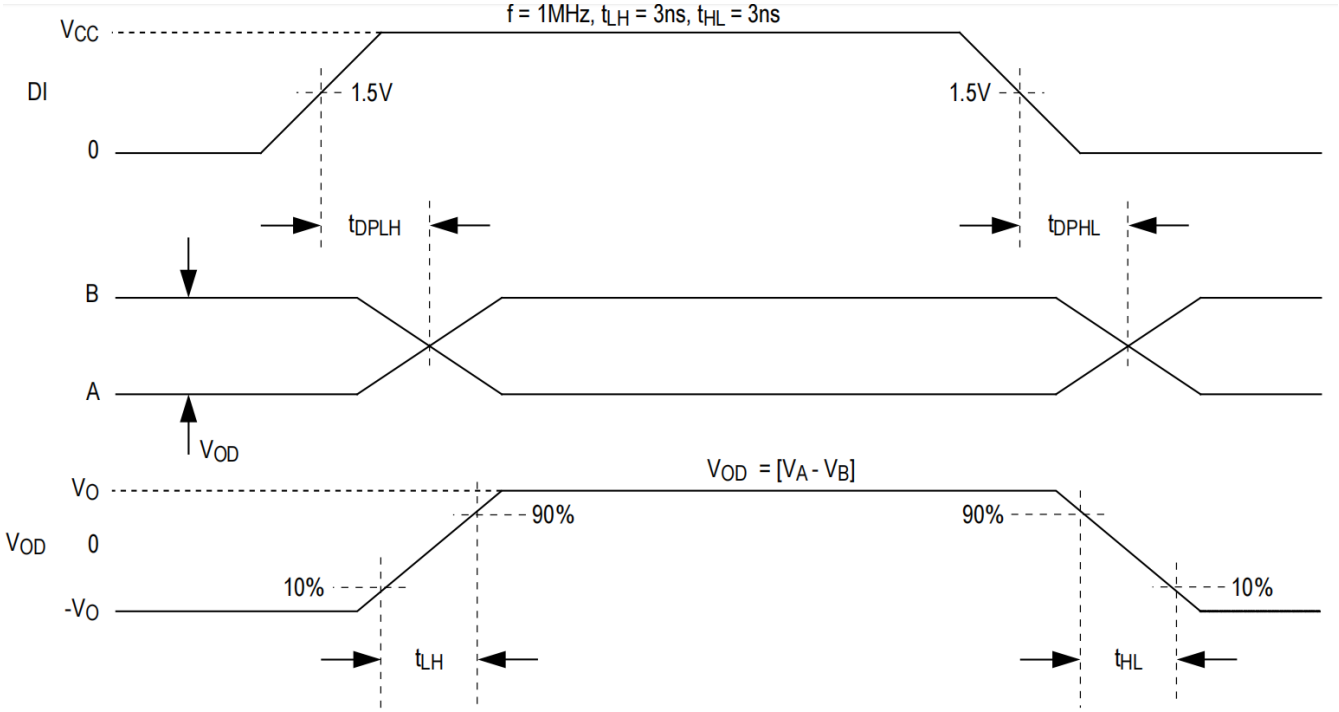


Figure 4. Drive transmission delay

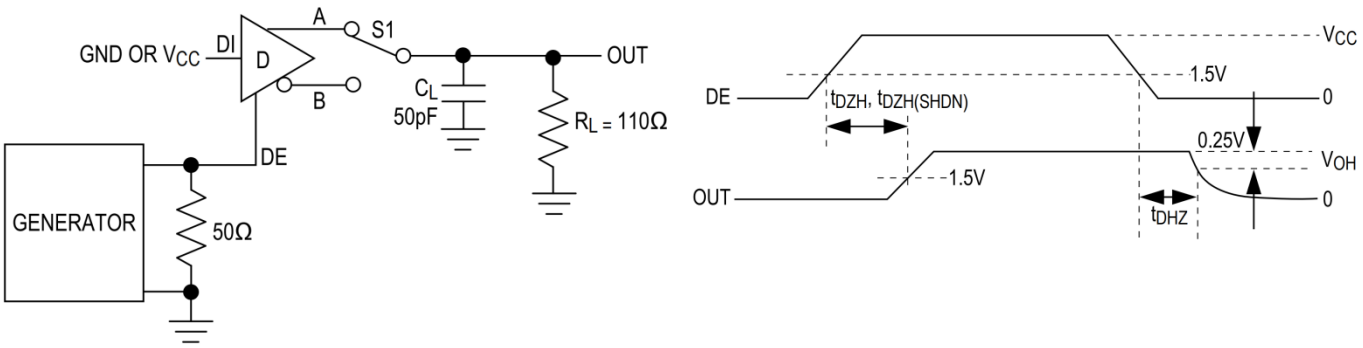


Figure 5. Driver enable and disable time（t_{DZH}，t_{DHZ}）

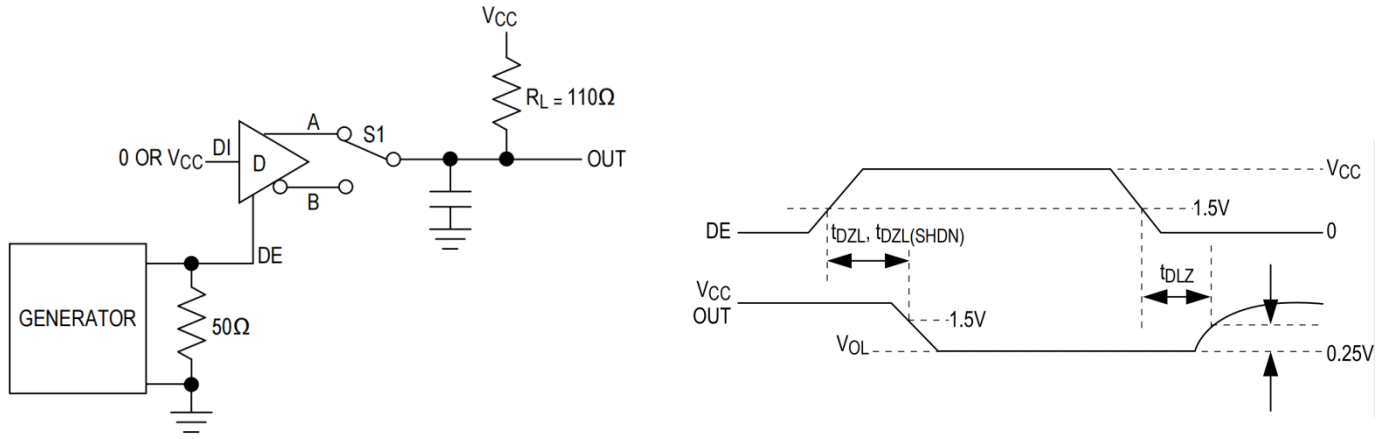


Figure 6. Drive enable and disable time（t_{DZL}，t_{DLZ}）

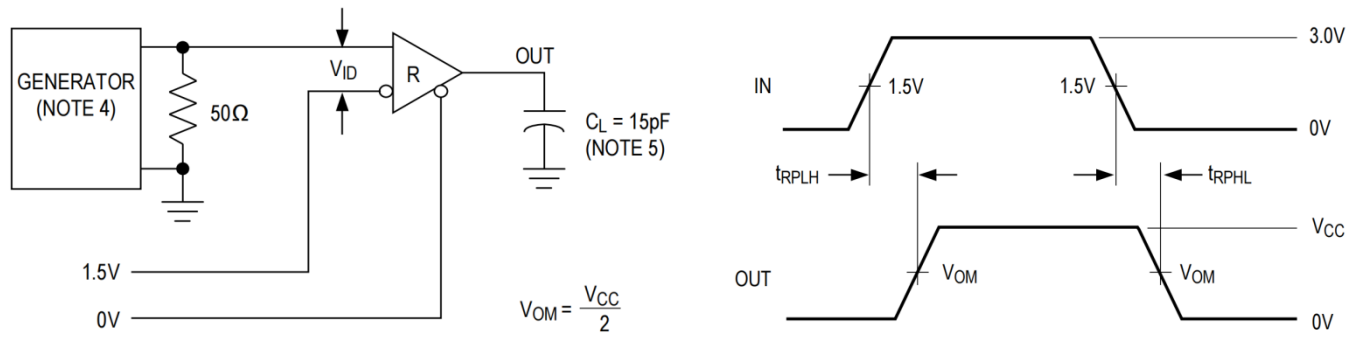


Figure 7. Receiver transmission delay test circuit and receiver transmission delay

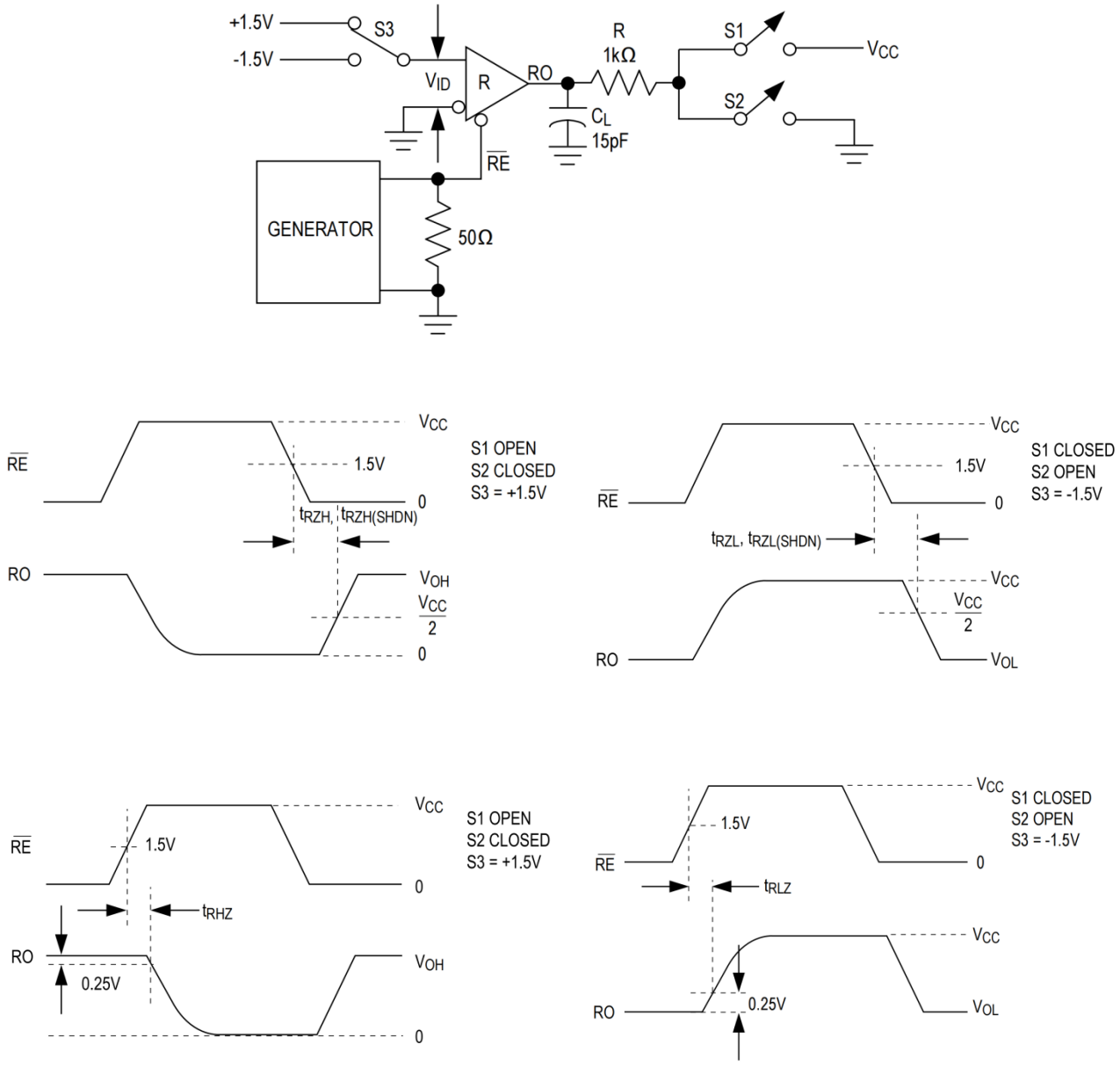


Figure 8. Receiver enable and disable time

7 Function Tables

Table 1. Driver Function Table

INPUTS			OUTPUTS		MODE
REN	DE	DI	B	A	
X	1	1	0	1	Enable
X	1	0	1	0	Enable
0	0	X	High resistance		Driver Disable
1	0	X	High resistance		Shutdown

Table 2. Receiver Function Table

INPUTS			OUTPUTS	MODE
REN	DE	A-B	RO	
0	0	≥-10mV	1	Enable
0	0	≤-200mV	0	Enable
0	0	Open/Short	1	Enable
1	1	X	High resistance	Receiver Disable
1	0	X	High resistance	Shutdown

8 Application Information

NOTE

The following contents are the precautions and usage suggestions for GXA3485 in specific applications by Beijing Galaxy-CAS Technology Co., Ltd. which does not make promises about its accuracy or completeness. Customers are responsible for determining suitability of components for their purposes based on their own usage needs and application scenarios. Customers should test and verify their design implementation to confirm system functionality and avoid losses.

Brief description

GXA3485 is a low-power transceiver for RS-485 and RS-422 communications, which can transmit and receive at data rates up to12Mbps. Driver Enable (DE) and Receiver Enable (REN) pins are included on the

GXA3485. When disabled, the driver and receiver outputs are high impedance. When both the driver and receiver are disabled (in a high impedance state), the chip starts low-power shutdown mode.

Driver Output Protection

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two mechanisms. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage rang. In addition, a thermal shut--down circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Supports 256 transceivers to be attached to the bus

The receiver input impedance of the GXA3485 chip is 96kΩ (1/8-unit load) that allows up to 256 transceivers on the bus. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit loads to the line.

15kV ESD Protection

ESD-protection structures are incorporated on all pins of the GXA3485 to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the GXA3485 of devices have extra protection against static electricity to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the devices will keep working without latch up or damage.

Specific Applications

The GXA3485 transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figure 9 show typical net work applications circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet. To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible.

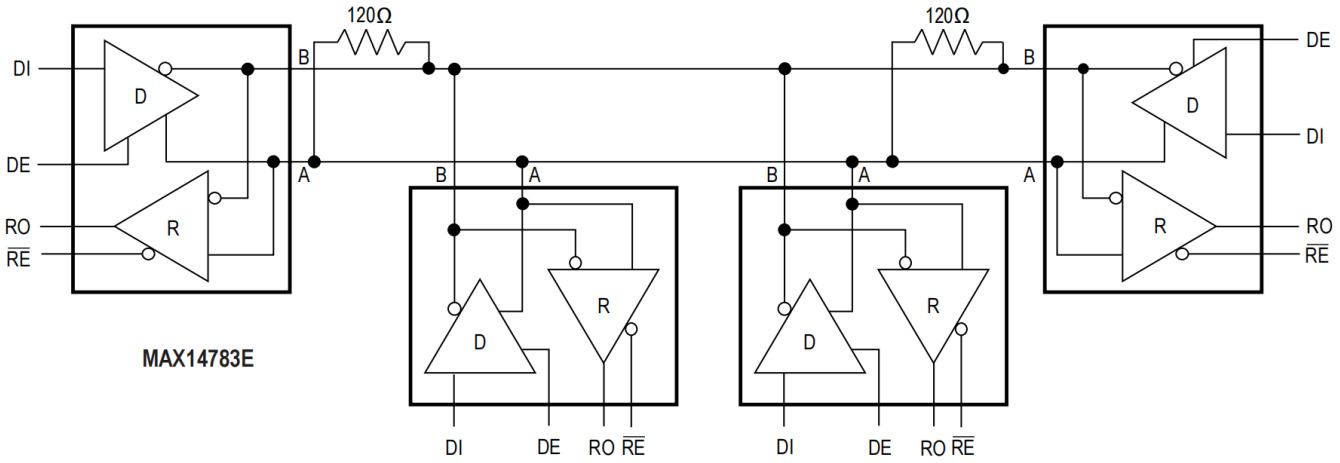
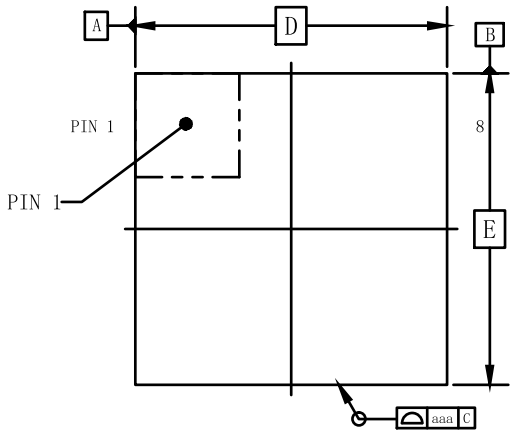


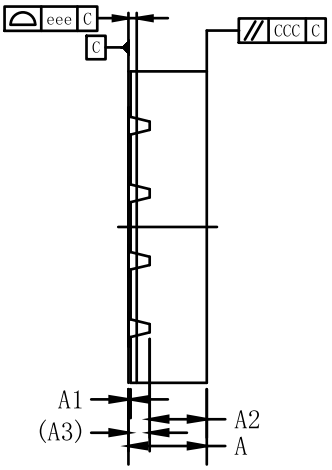
Figure 9. Typical Connections of the GXA3485

9 Package Information

9.1 DFN-8

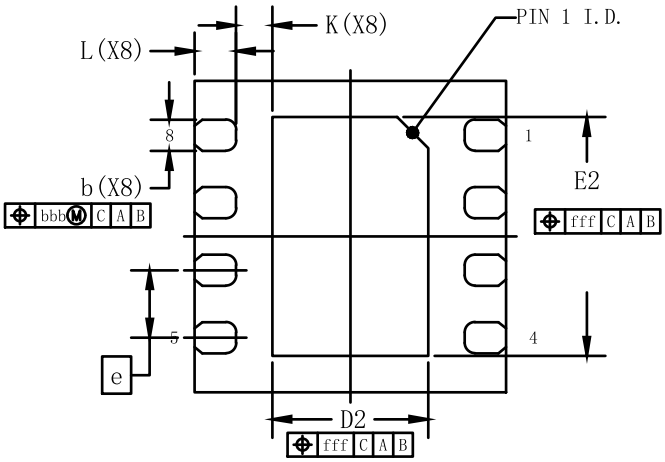


TOP VIEW



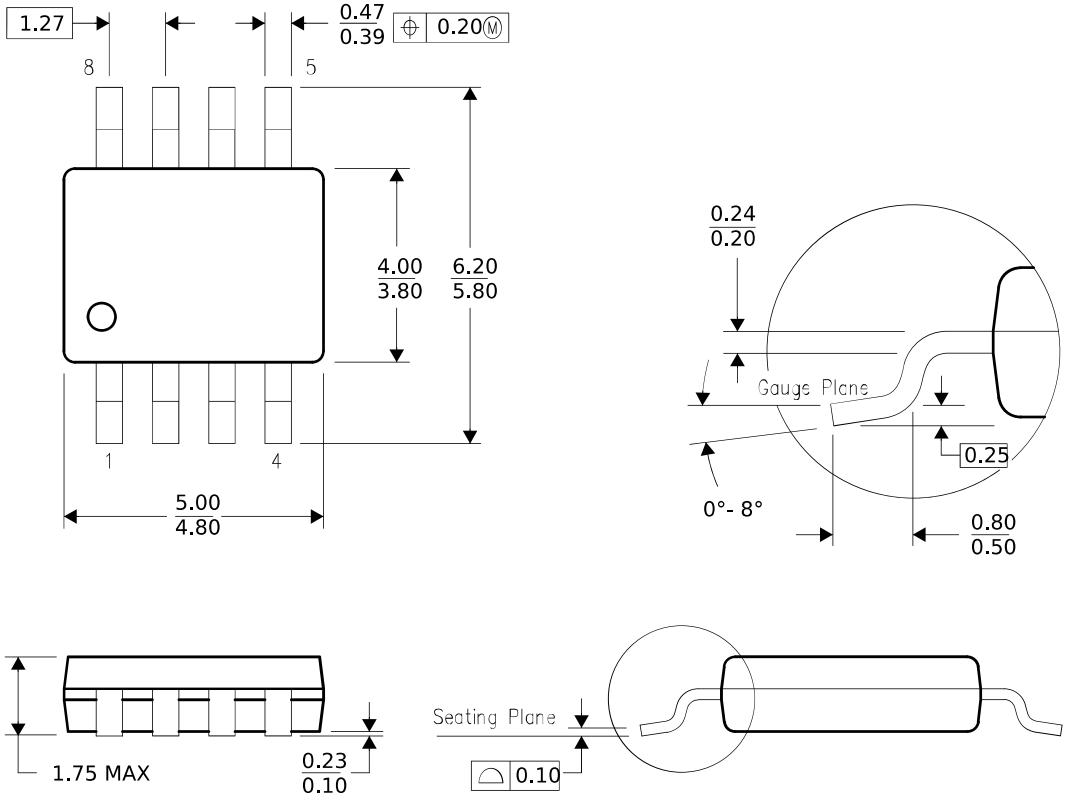
SIDE VIEW

Item		Symbol	Minimum	Normal	Maximum
Body Size	X	D		3.0 BSC	
	Y	E		3.0 BSC	
Exposed Pad Size	X	D2	1.40	1.50	1.60
	Y	E2	2.20	2.30	2.40
Total Thickness		A	0.70	0.75	0.80
Stand Off		A1	0	0.02	0.05
Molding Thickness		A2		0.55	
LF Thickness		A3		0.203 REF	
Lead Width		b	0.25	0.30	0.35
Lead Length		L	0.30	0.40	0.50
Lead Pitch		e		0.65 BSC	
Lead tip to Exposed Pad		K		0.35 REF	
Package Edge Tolerance		aaa		0.10	
Lead Offset		bbb		0.10	
Molding Flatness		ccc		0.10	
Coplanarity		eee		0.08	
Exposed Pad Offset		fff		0.10	

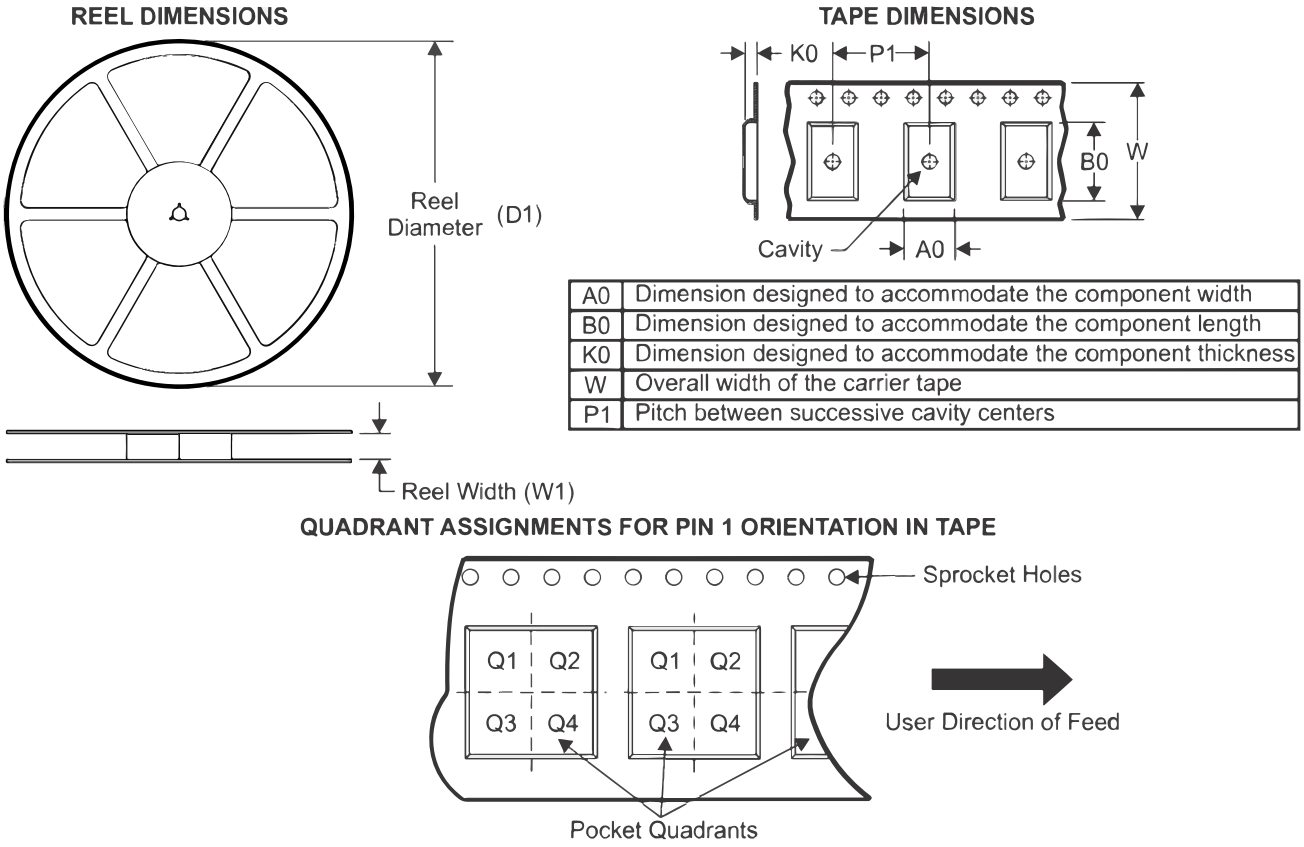


BOTTOM VIEW

9.2 SOP-8


1.27
0.47
0.39
0.20Ⓜ
8
5
4.00
3.80
6.20
5.80
1
4
5.00
4.80
0.24
0.20
Gauge Plane
0.25
0°- 8°
0.80
0.50
1.75 MAX
0.23
0.10
Seating Plane
0.10

9.3 Reel and Tape Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Package Type	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SOP-8	330	12.40	6.55	5.30	2.00	8.00	12.00	Q1

10 Ordering Information

Order Number	Chip Model	Package	SPQ	Note
GXA3485Z-EC-T&R	GXA3485Z	SOP-8	Undetermined	Sample
GXA3485Z-EE-T&R	GXA3485Z	SOP-8	Undetermined	Sample