Single Digital Potentiometer with SPI Interface

Features

- ZJC2741-10: 10 kΩ Normal Resistance
- ZJC2741-100: 100 kΩ Normal Resistance
- 256 Tap Position Variable Resistance Device
- INL: ±0.25 LSB
- DNL: ±0.15 LSB
- SINAD: 73 dB at 1 kHz
- SPI™ Serial Interface
- 1 μA maximum supply current in static operation
- Single Supply: 2.7 V ~ 5.5 V
- Package: TSOT23-8
- Extended Temperature Range: -40 °C to +125 °C

Applications

- Precision Data Acquisition
- Automated Testing
- Precision Instrument
- Medical Instrument

General Description

The ZJC2741 devices is 256-position, digital potentiometers available in 10 kΩ and 100 kΩ resistance versions. The ZJC2741 is a single-channel device in 8-pin TSOT23 package. The wiper position of the ZJC2741 varies linearly and is controlled via an industry-standard SPI interface. The devices consume <1 μA during static operation. These devices operate from a single 2.7 V ~ 5.5 V supply and are specified over the extended and industrial temperature ranges.

Block Diagram

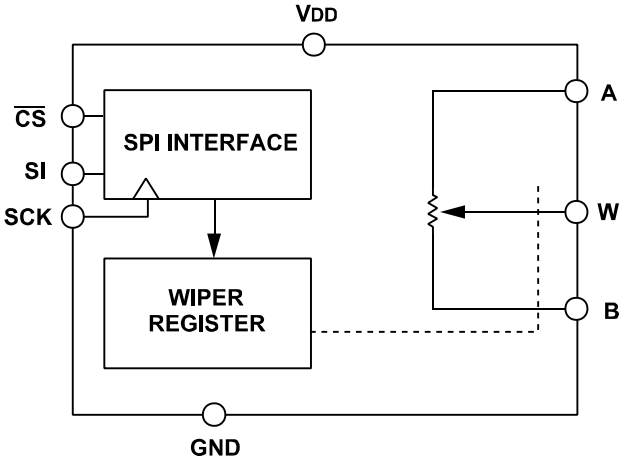

Figure 1. Block Diagram

Typical Characteristics

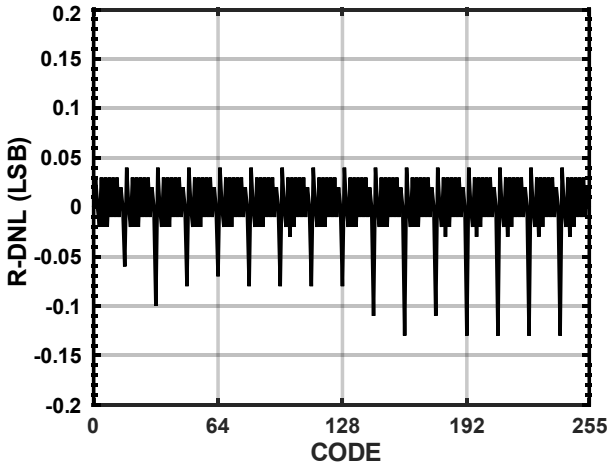

Figure 2. R-DNL vs. Code (10 kΩ)

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Version (Release A)[1]

Jun. 2026 — Release A

Update Interface Timing Specifications

Apr. 2026

Update Specifications and Typical Performance Characteristics

Jun. 2025 — Initial

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Pin Configurations and Function Descriptions

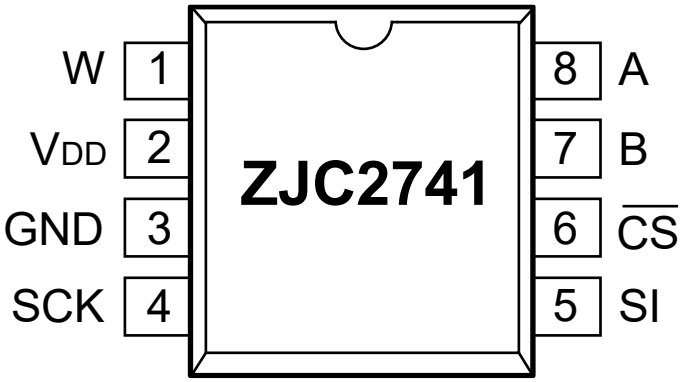

Figure 3. ZJC2741 Pin Configuration (8-lead TSOT23)

Mnemonic	Pin No.	I/O[1]	Description
W	1	AI	Wiper. Potentiometer Wiper Connection.
V_{DD}	2	P	Power Supply. Bypass with at least a 0.1 µF capacitor to GND.
GND	3	G	Ground
SCK	4	DI	Serial Clock. Positive edge triggered.
SI	5	DI	Serial Data Input.
$\overline{CS}$	6	DI	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data loads into the DAC register.
B	7	AI	Terminal B. Potentiometer Terminal B Connection.
A	8	AI	Terminal A. Potentiometer Terminal A Connection.

[1]AI: Analog Input; G: Ground; P: Power; DI: Digital Input.

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Absolute Maximum Ratings[1]

Parameter	Rating
V_{DD}	6.0 V
All inputs and outputs to GND	-0.3 V to V_{DD} + 0.3 V
Maximum Continuous Current into Pins A, B, and W	5 mA (10 kΩ) 1.5 mA (100 kΩ)
Storage Temperature Range	-60 °C to +150 °C
Junction Temperature Range	150 °C
Reflow Soldering	
Peak Temperature	260 °C
Electrostatic Discharge (ESD)[2]	
Human Body Model (HBM)[3]	3 kV
Charged Device Model (CDM)	2 kV

Thermal Resistance[4]

Package Type	θ_{JA}	θ_{JC}	Unit
TSOT23-8	195	47	°C/W

[1] These ratings apply at 25°C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[3] ANSI/ESDA/JEDEC JS-001 Compliant.

[4] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

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Specifications

DC Characteristics: R_{AB} = 10 kΩ

The ● denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V. Typical specifications represent values for V_{DD} = 5 V, V_B = 0 V, T_A = +25 °C.

Parameter	Symbol	Conditions		Min	Typ.[1]	Max	Unit
Rheostat Mode							
Nominal Resistance [2]	R	T_A = +25 °C			10		kΩ
Rheostat Integral Nonlinearity [3]	R-INL	V_{DD} ≥ 3.3 V	●	-0.6	±0.25	+0.6	LSB
		V_{DD} < 3.3 V	●	-0.8	±0.4	+0.8	
Rheostat Differential Nonlinearity [3]	R-DNL		●	-0.5	±0.15	+0.5	LSB
Nominal Resistor Tolerance	Δ R_{AB}/R_{AB}		●	-15		+15	%
Resistance Temperature Coefficient	$\Delta R_{AB}/R_{AB}/\Delta T$		●		±35		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5.5 V, I_W = 1 mA, Code 00h	●		50	100	Ω
Wiper Current	I_W					5	mA
Potentiometer Divider							
Resolution	N			8			Bits
Monotonicity	N			8			Bits
Integral Nonlinearity [4]	INL		●	-0.5	±0.15	+0.5	LSB
Differential Nonlinearity [4]	DNL		●	-0.3	±0.1	+0.3	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$				±5		ppm/°C
Full Scale Error	V_{WFSE}	Code FFh	●	-2.0	-1.2		LSB
Zero Scale Error	V_{WZSE}	Code 00h	●		1.2	2.0	LSB
Resistor Terminals							
Terminal Voltage Range[5]	$V_{A,B,W}$			0		V_{DD}	V
Capacitance (C_A or C_B)	$C_{A,B}$	f = 1 MHz, Code = 80h,			15		pF
Capacitance W	C_W	f = 1 MHz, Code = 80h,			15		pF
Dynamic Characteristics (All dynamic characteristics use V_{DD} = 5 V)							
-3 dB Bandwidth	BW	V_B = 0 V, Measured at Code 80h, Output Load = 30 pF			3		MHz
Settling Time	T_S	V_A = V_{DD}, V_B = 0 V, ±1% Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF			2		µS
Resistor Noise Voltage	e_{NWB}	V_A = Open, Code 80h, f =1 kHz			9		nV/√Hz

[1] Typical values represent average readings at 25 °C, V_{DD} = 5 V.
[2] V_{AB} = V_{DD}, no connection on wiper.
[3] Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. I_W = 50 µA for V_{DD} = 3 V and I_W = 400 µA for V_{DD} = 5 V for 10 kΩ version.
[4] INL and DNL are measured at V_W with the device configured in the voltage divider or potentiometer mode. V_A = V_{DD} and V_B = 0 V.
[5] Resistor terminals A, B and W have no restrictions on polarity with respect to each other.

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DC Characteristics: R_{AB} = 100 kΩ

The ●denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V. Typical specifications represent values for V_{DD} = 5 V, V_B = 0 V, T_A = +25 °C.

Parameter	Symbol	Conditions		Min	Typ.[1]	Max	Unit
Rheostat Mode							
Nominal Resistance [2]	R	T_A = +25 °C			100		kΩ
Rheostat Integral Nonlinearity [3]	R-INL	V_{DD} ≥ 3.3 V	●	-0.6	±0.2	+0.6	LSB
		V_{DD} < 3.3 V	●	-0.8	±0.4	+0.8	
Rheostat Differential Nonlinearity [3]	R-DNL		●	-0.5	±0.15	+0.5	LSB
Nominal Resistor Tolerance	Δ R_{AB}/R_{AB}		●	-15		+15	%
Resistance Temperature Coefficient	$\Delta R_{AB}/R_{AB}/\Delta T$		●		±10		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5.5 V, I_W = 1 mA, Code 00h	●		50	100	Ω
Wiper Current	I_W		●			1.5	mA
Potentiometer Divider							
Resolution	N			8			Bits
Monotonicity	N			8			Bits
Integral Nonlinearity [4]	INL		●	-0.5	±0.2	+0.5	LSB
Differential Nonlinearity [4]	DNL		●	-0.3	±0.1	+0.3	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$				±5		ppm/°C
Full Scale Error	V_{WFSE}	Code FFh	●	-0.5	-0.2		LSB
Zero Scale Error	V_{WZSE}	Code 00h	●		0.15	+0.5	LSB
Resistor Terminals							
Terminal Voltage Range [5]	$V_{A,B,W}$			0		V_{DD}	V
Capacitance (C_A or C_B)	$C_{A,B}$	f = 1 MHz, Code = 80h,			15		pF
Capacitance	C_W	f = 1 MHz, Code = 80h,			15		pF
Dynamic Characteristics (All dynamic characteristics use V_{DD} = 5 V)							
-3 dB Bandwidth	BW	V_B = 0 V, Measured at Code 80h, Output Load = 30 pF			0.3		MHz
Settling Time	T_S	$V_A = V_{DD}$, V_B = 0 V, ±1% Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF			18		μS
Resistor Noise Voltage	e_{NWB}	V_A = Open, Code 80h, f =1 kHz			27		nV/√Hz

[1] Typical values represent average readings at 25°C, V_{DD} = 5 V.
[2] $V_{AB} = V_{DD}$, no connection on wiper.
[3] Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. I_W = 5 μA for V_{DD} = 3 V and I_W = 40 μA for V_{DD} = 5 V for 100 kΩ version.
[4] INL and DNL are measured at V_W with the device configured in the voltage divider or potentiometer mode. $V_A = V_{DD}$ and V_B = 0 V.
[5] Resistor terminals A, B and W have no restrictions on polarity with respect to each other.

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Digital I/O and Power Characteristics

The ●denotes the full temperature range (-40 °C to +125 °C) for specified performance. Unless otherwise noted, V_{DD} = 2.7 V to 5.5 V. Typical specifications represent values for V_{DD} = 5 V, V_{SS} = 0 V, V_B = 0 V, T_A = +25 °C.

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
Digital Inputs ($\overline{CS}$, SCK, SI)							
Schmitt Trigger High-Level Input Voltage	V_{IH}	V_{DD} = 5 V	●	0.7 × V_{DD}			V
Schmitt Trigger Low-Level Input Voltage	V_{IL}	V_{DD} = 5 V	●			0.3 × V_{DD}	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		●	0.1 × V_{DD}			V
Input Leakage Current	I_{LI}	$\overline{CS}$ = V_{DD}, V_{IN} = V_{DD}				1	µA
Pin Capacitance (All Inputs)	C_{IN}	V_{DD} = 5.0 V, T_A = +25 °C, f_C = 1 MHz			3		pF
Power Requirements							
Operating Voltage Range	V_{DD}		●	2.7		5.5	V
Supply Current, Static [1]	I_{DDS}		●		0.2		µA
Temperature Range							
Specified Performance				-40		+125	°C

[1] Supply current is independent of current through the potentiometers.

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Timing Specifications

Unless otherwise specified, V_{DD} = 2.7 V to 5.5 V, T_A = -40 °C to +125 °C

Parameter	Symbol	Min	Typ.	Max	Unit
Clock Frequency (V_{DD} = 5 V)	F_{CLK}			25	MHz
Clock High Time	t_{HI}	18			ns
Clock Low Time	t_{LO}	18			ns
$\overline{CS}$ Fall to First Rising SCK Edge	t_{CSSR}	15			ns
Data Input Setup Time	t_{SU}	12			ns
Data Input Hold Time	t_{HD}	5			ns
SCK Rise to $\overline{CS}$ Rise Hold Time	t_{CHS}	30			ns
SCK Rise to $\overline{CS}$ Fall Delay	t_{CS0}	10			ns
$\overline{CS}$ Rise to SCK Rise Hold	t_{CS1}	100			ns
$\overline{CS}$ High Time	t_{CSH}	10			ns

For one frame ($\overline{CS}$ is low) of serial data write operation, if the number of SCK cycles during the chip select low level is more than 8, the last 8-bit data is valid, and the redundant high bits are ignored.

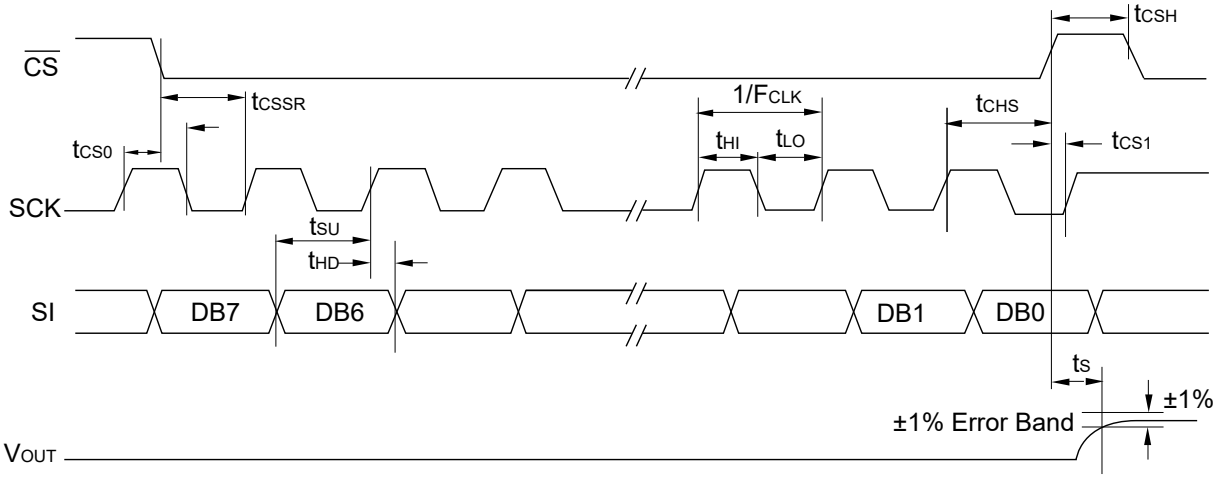

Figure 4. Detailed Serial Interface Timing

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Typical Performance Characteristics

Unless otherwise stated, T_A = 25 °C, V_{DD} = 5.0 V.

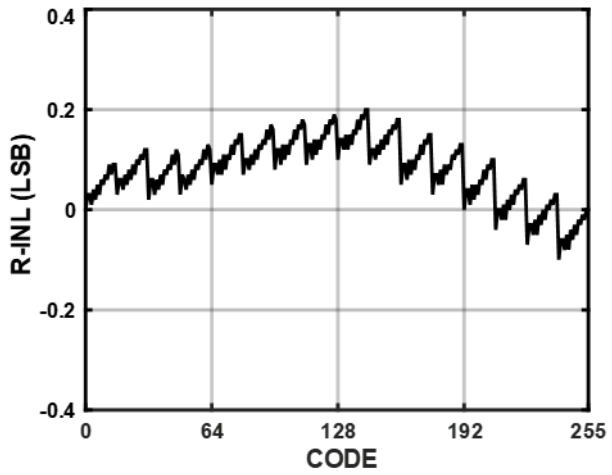

Figure 5. Rheostat-INL vs. Code (10 kΩ)

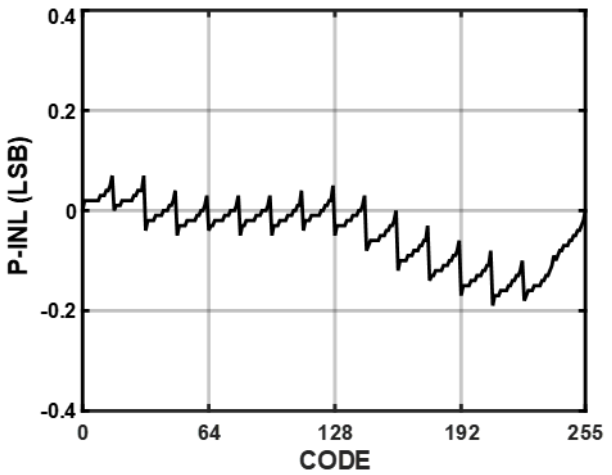

Figure 6. Potentio-INL vs. Code (10 kΩ)

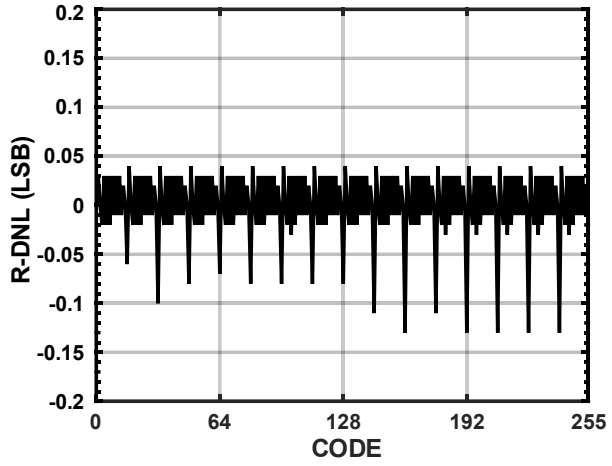

Figure 7. Rheostat-DNL vs. Code (10 kΩ)

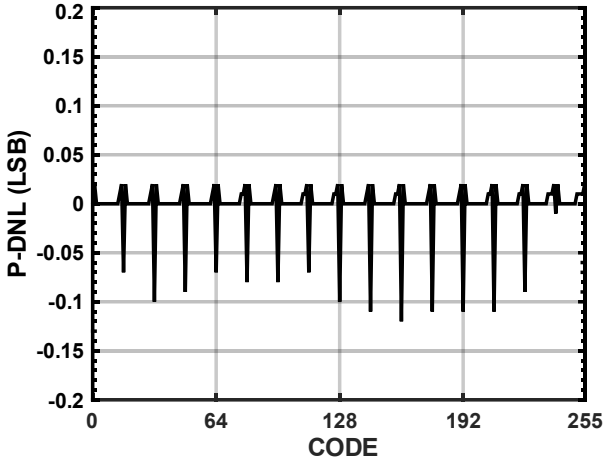

Figure 8. Potentio-DNL vs. Code (10 kΩ)

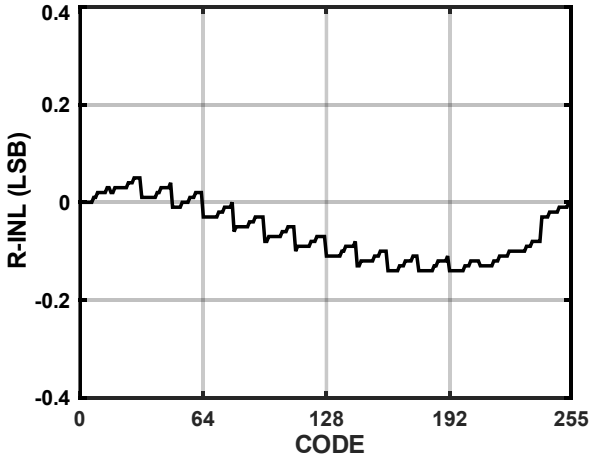

Figure 9. Rheostat-INL vs. Code (100 kΩ)

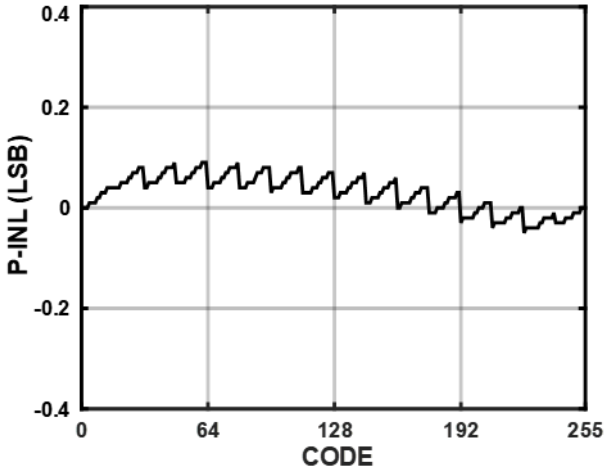

Figure 10. Potentio-INL vs. Code (100 kΩ)

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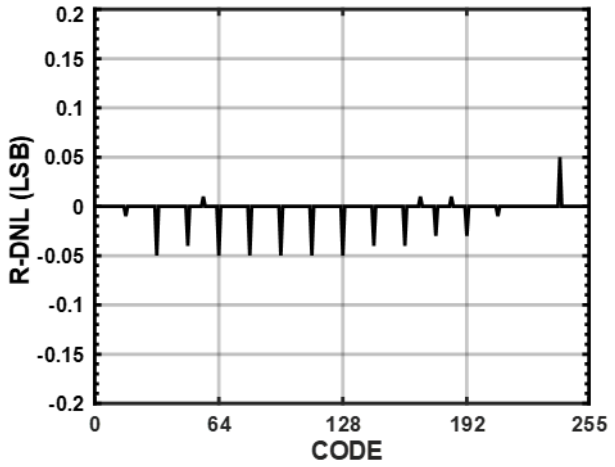

Figure 11. Rheostat-DNL vs. Code (100 kΩ)

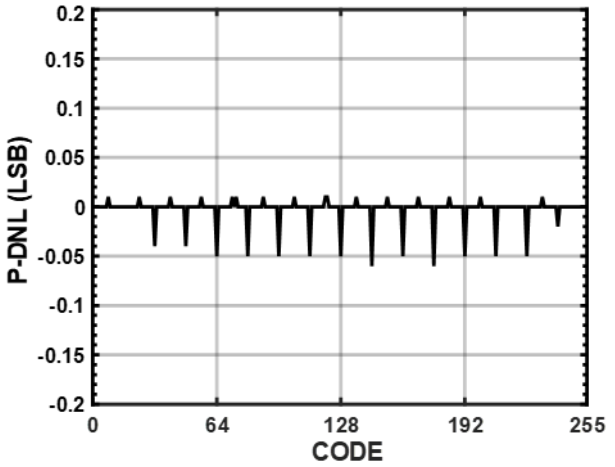

Figure 12. Potentio-DNL vs. Code (100 kΩ)

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Serial Interface

Communications from the controller to the ZJC2741 digital potentiometers is by using the SPI serial interface.

Executing any command is accomplished by setting $\overline{CS}$ low and then clocking-in a code byte into the shift register. The code is executed when $\overline{CS}$ is raised. Data is clocked in on the rising edge of clock. The device will track the number of clocks (rising edges) while $\overline{CS}$ is low and will abort if the number of clocks is less than 8. For one frame ($\overline{CS}$ is low) of serial data write operation, if the number of SCK cycles during the chip select low level is more than 8, the last 8-bit data is valid, and the redundant high bits are ignored.

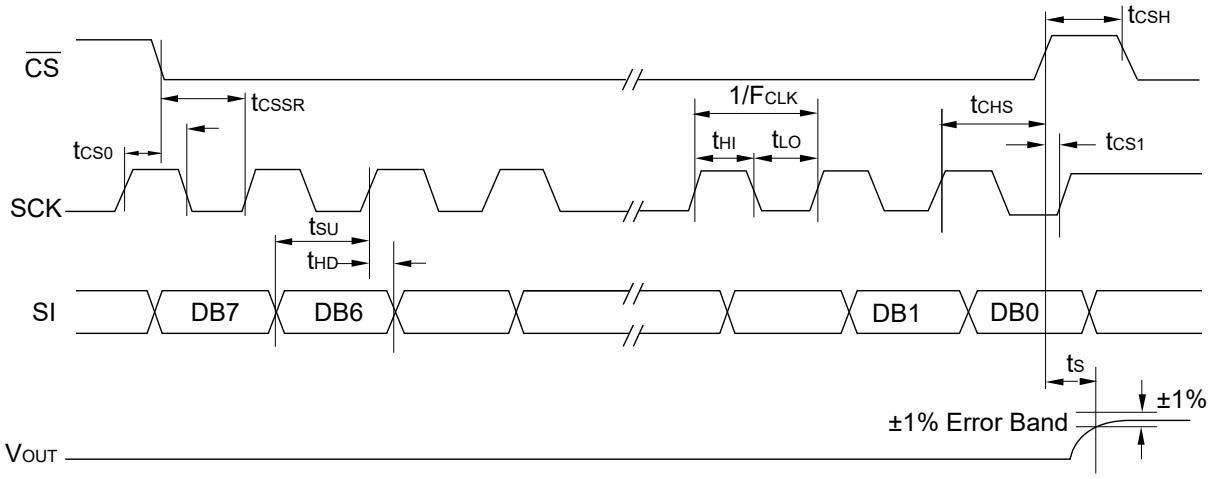

Figure 13. Detailed Serial Interface Timing

Programming the Variable Resistor

Rheostat Operation—±15% Resistor Tolerance

The ZJC2741 operates in rheostat mode when only two terminals are used as a variable resistor. The unused terminal can be floating, or it can be tied to Terminal W.

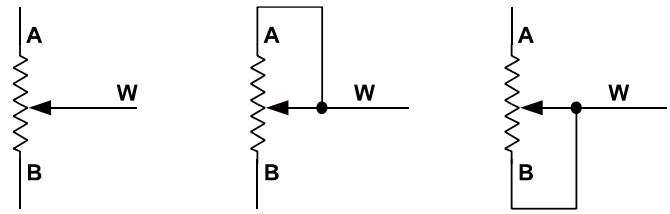

Figure 14. Rheostat Mode Configuration

The nominal resistance between Terminal A and Terminal B, R_{AB}, is 10 kΩ or 100 kΩ, and has 256 tap points accessed by the wiper terminal. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible wiper settings. The general equations for determining the digitally programmed output resistance between Terminal W and Terminal B are

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad From\ 0x00\ to\ 0xFF$$

where:

- D is the decimal equivalent of the binary code in the 8-bit RDAC register.
- R_{AB} is the end to end resistance.
- R_W is the wiper resistance.

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In potentiometer mode, similar to the mechanical potentiometer, the resistance between Terminal W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. R_{WA} also gives a maximum of 15% absolute. R_{WA} starts at the maximum resistance value and decreases as the data loaded into the latch increases. The general equations for this operation are

$$R_{AW}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \quad From\ 0x00\ to\ 0xFF$$

where:

- D is the decimal equivalent of the binary code in the 8-bit RDAC register.
- R_{AB} is the end to end resistance.
- R_W is the wiper resistance.

Programming The Potentiometer Divider

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A that is proportional to the input voltage at A to B.

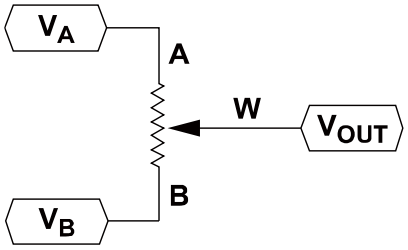

Figure 15. Potentiometer Mode Configuration

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} \times V_A + \frac{R_{AW}(D)}{R_{AB}} \times V_B$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. The output voltage is dependent mainly on the ratio of the internal resistors, R_{AW} and R_{WB}, and not the absolute values.

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Outline Dimensions

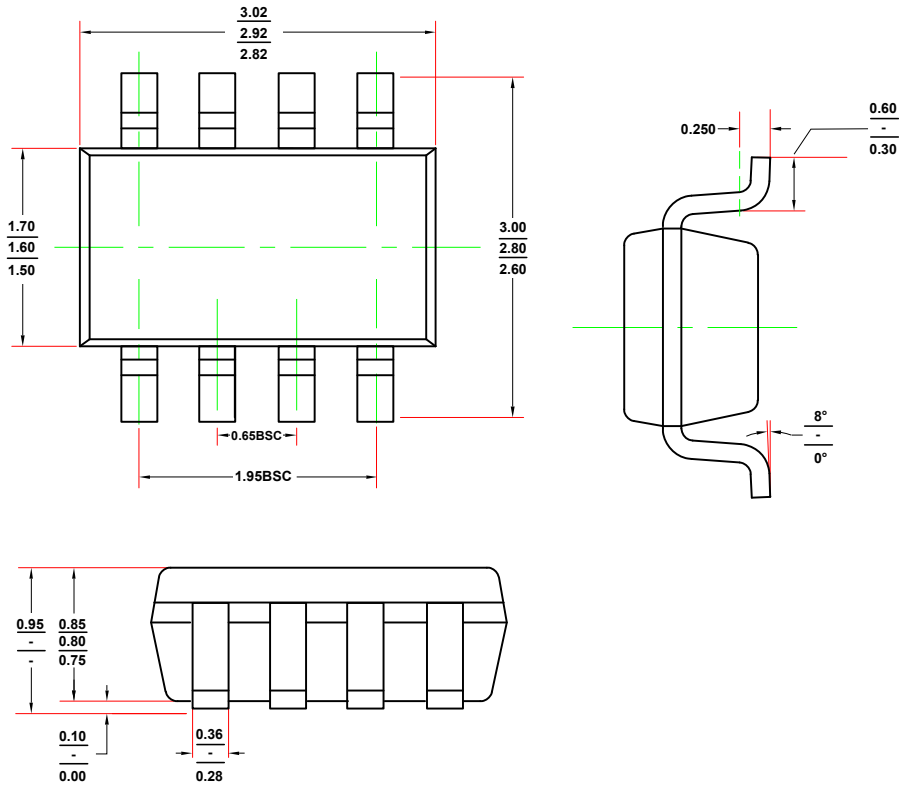

Figure 16. 8-Lead TSOT23 Package Dimensions shown in millimeters

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Ordering Guide

Model	Orderable Device	Package	Marking	Supply Voltage (V)	Temperature Range(°C)	External Package
ZJC2741-10	ZJC2741-10AZABR	TSOT23-8	274113	2.7 to 5.5	-40 to +125	7”reel
ZJC2741-100	ZJC2741-100AZABR	TSOT23-8	274114		-40 to +125	7”reel

Product Order Model

ZJXXXXX X X X X X Q1

- Q1: Automotive Grade
- External Package: T = Tube; R = Reel
- Temperature Range: A = -40 °C to 125 °C Automotive Grade 1, B = -40 °C to 125 °C; E = -40 °C to 85 °C
- Number of Pins: R = 3; K =5; T = 6, A = 8; B = 10; D = 14; E = 16; P = 20
- Package Type: S = SOIC; U = MSOP, TSSOP, SOT; T = DFN, QFN; X = SC70; W = WLCSP; Z = TSOT23
- Grade: B grade is better than A grade
- Base: R = Voltage reference; A = Amplifier; C = Data Converter; G = Switches and Multiplexers; M = Others

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Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
Amplifier		
ZJA3000-1/2/4 ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3018-2 ZJA3008-2	OVP ±75 V, 36 V, Low Power, High Precision Op Amp 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP ±75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/µS, 50 µV max Vos, 1 µV/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3216/06/02-1/2	Precision 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 30 µV max Vos, 1 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 µV max Vosi, ±2.4 V to ±18 V, -40 °C to 125 °C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G ≥ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7 ZJA3678/9	Low power, G=1 Single/Dual 36 V difference amplifier Low power, G=0.5/2 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min (G = 1), Vos 100 µV max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 µA/channel, 2.7 V to 36 V
ZJA3669	High Common-Mode Voltage Difference Amplifier	±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/µS, 50 nS to 16-bit, 50 µV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 20/10/5 MHz CMOS RRIO Op Amps	20/10/5 MHz, RRIO, 2 mV max Vos, 6 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ±2.4 V to ±18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
ZJR1302	5.5 V low power compact precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096 V, 30 ppm/°C max drift -40 °C to 125 °C, 130 µA, SOT23-3
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ±50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV

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