WS2915

Single-line, 65536-level grayscale, five-channel Constant Current LED Driver IC

main features

- The OUTR, G, B, W1, and W2 ports have a withstand voltage of 40 V; the DOUT, DIN, and FDIN ports have a withstand voltage of 24 V.
- The chip incorporates an integrated Zener diode; for power supplies below 24 V, simply connect a series resistor to the VDD pin – no external Zener diode is required.
- The chip features built-in resistors, and the DIN and DOUT ports are equipped with overvoltage protection; instant short-circuiting of the 24 V supply will not cause device burnout.
- Gray-scale adjustment circuit (65,536-level adjustable gray-scale).
- Built-in signal shaping circuit: Upon receiving a signal, each IC performs waveform shaping before outputting it, ensuring that line waveform distortion does not accumulate.
- Built-in power-on reset and power-off reset circuits.
- The PWM control interface supports 65,536-level adjustment with a scanning frequency of 2 kHz.
- A serial interface cascading interface that enables data reception and decoding over a single signal line.
- The transmission distance between any two points does not exceed 3 meters; no additional circuitry is required.
- W1 and W2 connected in parallel can deliver up to 120 mA.
- When the refresh rate is 30 frames per second, the number of cascades shall be no less than 400 points.
- The data transmission speed can reach up to 800 Kbps.

Primary application areas

- Full-color LED decorative lighting, such as LED strings, LED strips, LED modules, etc.
- Indoor/Outdoor LED video display or irregular screen.
- LED consumer electronics.
- Various LED lighting products.

Product Overview

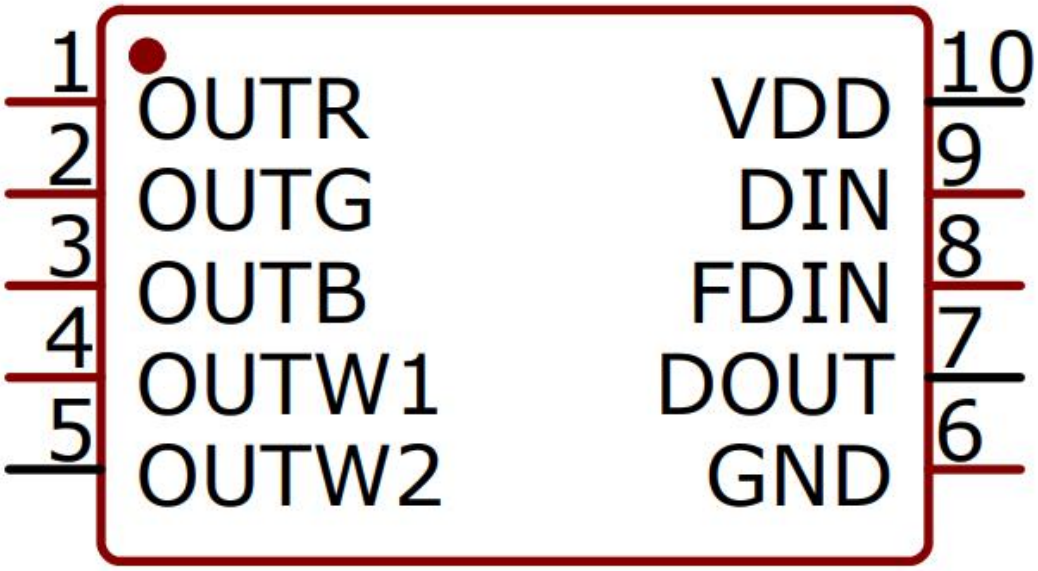
The WS2915 is a dedicated five-channel LED driver control circuit. The chip incorporates an intelligent digital interface data latch, signal shaping, amplification, and driving circuit, as well as a high-precision internal oscillator and a 40 V high-voltage programmable constant-current output driver. Additionally, to reduce power supply ripple, the OTR, G, B, W1, and W2 channels feature a delayed turn-on function, which helps minimize circuit ripple during frame refresh periods.

The chip employs a single-line zero-return encoding communication protocol. Upon power-on reset, the DIN port receives data transmitted from the controller; the first 80 bits of data are extracted by the first chip and sent to its internal data latch, while the remaining data undergoes shaping and amplification via an internal shaping and amplification circuit before being forwarded and output through the DO port to the next cascaded chip. With each chip through which the signal passes, its length decreases by 80 bits. The chip utilizes automatic shaping and forwarding technology, which means the maximum number of cascaded chips is not constrained by signal transmission limitations but is solely determined by the required signal transmission speed.

The chip's internal data latch generates different duty-cycle control signals at the OTR, G, B, W1, and W2 control pins based on the received 80-bit data; when the RESET signal is received at the DIN pin, all chips simultaneously transmit the received data to their respective segments. Upon the expiration of this RESET signal, the chip resumes

receiving data; after successfully receiving the initial 80-bit data, the data is forwarded via the DO port. Until the RESET code is received, the original output levels at the OTR, G, B, W1, and W2 pins remain unchanged; upon reception of a low-level RESET code lasting 280 μs or longer, the chip outputs the just-received 80-bit PWM data pulse width to the OTR, G, B, W1, and W2 pins.

Output terminal arrangement



Output Port Function

order number	symbol	Pin Name	functional description
1	OUTR	LED driver output	RED (Red) PWM Control Output
2	OUTG	LED driver output	GREEN (Green) PWM Control Output
3	OUTB	LED driver output	BLUE (Blue) PWM Control Output
4	OUTW1	LED driver output	WHITE1 (White) PWM control output
5	OUTW2	LED driver output	WHITE2 (White) PWM control output
6	GND	the earth	Signal Grounding and Power Supply Grounding
7	DO	presentation of information	Display cascaded data output
8	FDIN	Data Input 2	Display Data Input 2
9	DIN	Data Input 1	Display Data Input 1
10	VDD	Logical Power Supply	ICsupply electricity

Maximum rated value (TA = 25°C, VSS = 0 V)

parameter	symbol	scope	unit
Logical power supply voltage	VDD	+3.5~+5.9	V
R, G, B, W1, W2 output ports – voltage withstand rating	VOUT	VSS-0.7~40	V
DINwithstand voltage	VI	VSS-0.7 ~ 24	V
DOUTwithstand voltage	Vo	VSS-0.7 ~ 24	V
working temperature	Topt	-40 ~ +85	℃
storage temperature	Tstg	-40~+85	℃

Electrical parameters (TA = 25°C; VDD = 4.5–5.5 V; VSS = 0 V)

parameter	symbol	minimum	typical case	maximum	unit	test condition
quiescent current	Io	——	0.3	——	mA	DC=5V
R、G、B Low-level output current	IOL	28	30	35	mA	DC=5V, DIN（FFH）
W1、W2 Low-level output current	IOL	58	60	70	mA	DC=5V, DIN（FFH）
Single RGBW current differential	Dif	——	——	1.2	mA	DC=5V, DIN
Low-level output current	Idout	10	——	——	mA	Vo=0.4V，DOUT
Input current	II	——	——	±1	μA	VI=VDD/VSS
high-level input	VIH	0.55VDD	——	——	V	DIN
Low-level input	VIL	——	——	0.3 VDD	V	DIN
lagging voltage	VH	——	0.35	——	V	DIN

Switching characteristics (TA = 25°C, VDD = 4.5–5.5 V, VSS = 0 V)

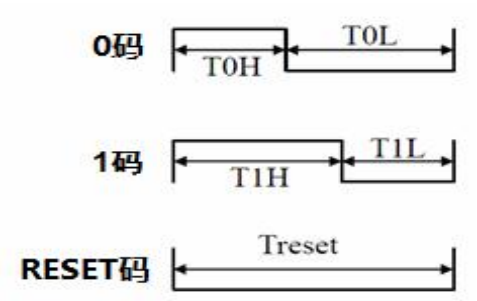
parameter	symbol	minimum	typical case	maximum	unit	test condition
oscillation frequency	*Fosc*	——	800	——	KHz	——
propagation delay time	tPLZ	——	——	300	ns	CL=15pF, DIN→DOUT, RL=10KΩ
drop-out time	tTHZ	——	——	120	μs	CL=300pF, OUTR/OUTG/OUTB
data-signalling rate	*FMAX*	600	——	——	Kbps	Duty cycle: 50%
input capacitance	CI	——	——	15	pF	——

Data transmission time

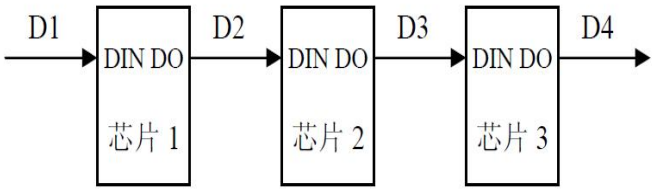
T0H	0 code, high-level duration	220ns~380ns
T1H	1码,高电平持续时间	520ns~1us
T0L	0 code, low-level duration	580ns~1us
T1L	1码,低电平持续时间	580ns~1us
RES	Frame unit, low-level duration	≥280 μs
T0H+T0L、T1H+T1L ≥ 1.25μs		

Time-domain waveform plot

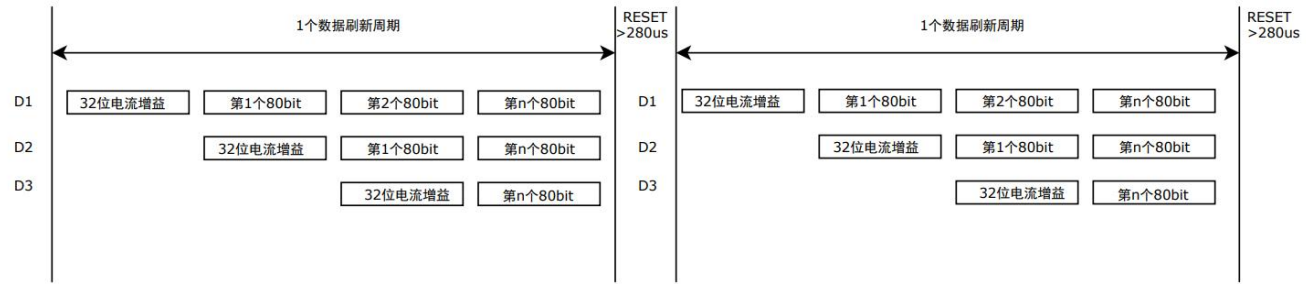
Input coding scheme:



method of attachment:



Data transmission method



Note: D1 represents the data transmitted by the MCU; D2, D3, and D4 represent the data automatically shaped and forwarded by the cascaded circuit.

- **5-channel data structure**

RI4	RI3	RI2	RI1	RI0	GI4	GI3	GI2	GI1	GI0	BI4	BI3	BI2	BI1	BI0	W1I4
W1I3	W1I2	W1I1	W1I0	W2I4	W2I3	W2I2	W2I1	W2I0	check bit 0	check bit 0	check bit 0	check bit 0	check bit 0	check bit 0	check bit 0
R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R2	R0
G15	G14	G13	G12	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
W1_15	W1_14	W1_13	W1_12	W1_11	W1_10	W1_9	W1_8	W1_7	W1_6	W1_5	W1_4	W1_3	W1_2	W1_1	W1_0
W2_15	W2_14	W2_13	W2_12	W2_11	W2_10	W2_9	W2_8	W2_7	W2_6	W2_5	W2_4	W2_3	W2_2	W2_1	W2_0

High-level transmission: data is sent in the order RGBW1W2; the check bit consists of seven '0's.

current gain

电流增益设置	RGB 电流（mA）	W1W2 电流（mA）	W1W2 并联（mA）
0	0	0	0
1	0.92	2.09	4.16
2	2.04	4.23	8.45
3	3.02	6.31	12.58
4	4.15	8.51	16.98
5	5.11	10.55	21.06
6	6.16	12.62	25.20
7	7.10	14.64	29.21
8	8.27	16.67	33.40
9	9.22	18.70	37.38
A	10.24	20.73	41.3
B	11.18	22.72	45.2
C	12.25	24.70	49.2
D	13.17	26.67	53.0
E	14.17	28.62	56.9
F	15.08	30.54	60.7
10	16.42	32.59	62.4
11	17.34	34.59	66.3
12	18.34	36.63	70.2
13	19.25	38.63	74.1
14	20.28	40.5	77.7
15	21.19	42.4	81.6
16	22.17	44.3	85.4
17	23.06	46.3	89.1
18	24.11	47.6	91.1
19	24.98	49.6	94.7
1A	25.94	51.5	98.5
1B	26.82	53.4	102.2
1C	27.82	55.1	105.5
1D	28.67	57.0	109.2
1E	29.61	58.8	112.8
1F	30.46	60.7	116.3

Typical application circuit

1. **Power supply voltage VCC = 5 V (each channel drives one LED):**

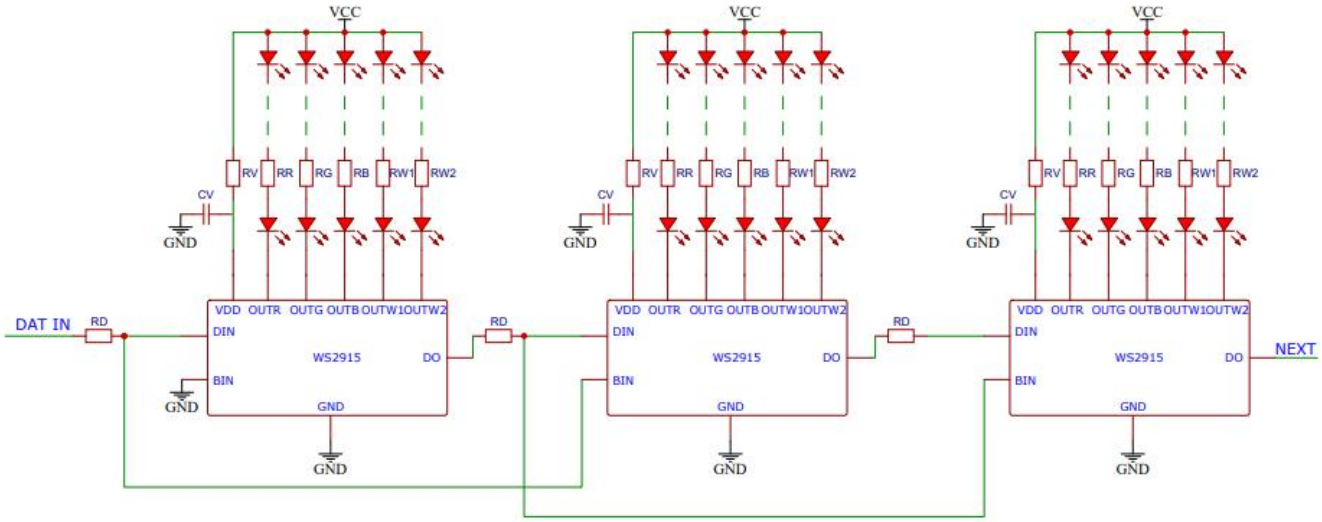
The recommended values for RV and CV are 150 Ω and 0.1 μF, respectively. The WS2915 is compatible with the earlier 5 V WS2805 application circuit and can operate normally at 100 Ω.

2. **Power supply voltage VCC = 12 V (each channel drives 3 LEDs):**

The recommended values for RV and CV are 4.7 kΩ and 0.1 μF, respectively. The WS2915 is compatible with the earlier 12 V WS2805 application circuit and can operate normally at 2.7 kΩ.

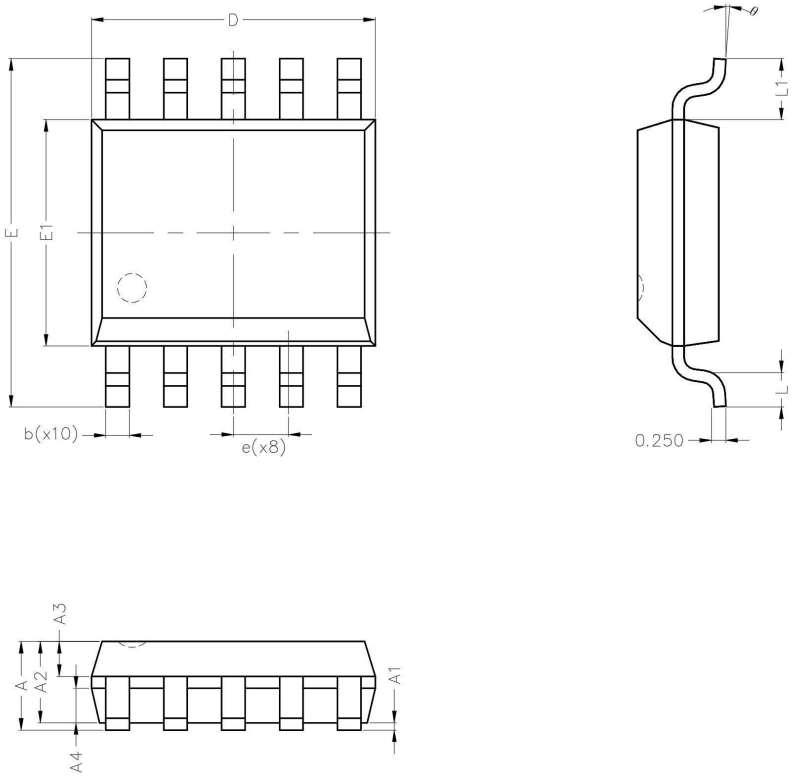
3. **Power supply voltage VCC = 24 V (each channel drives 6 LEDs):**

The recommended values for RV and CV are 10 kΩ and 0.1 μF, respectively. The WS2915 is compatible with the earlier 24 V WS2805 application circuit and can operate normally at 7.5 kΩ.



Package Diagram and Parameters

- **SOP10 Package**



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	–	–	1.75
STAND OFF	A1	0.05	0.125	0.20
MOLD TOTAL THICKNESS	A2	1.30	1.40	1.60
TOP MOLD THICKNESS	A3	0.55	0.60	0.65
BOTTOM MOLD THICKNESS	A4	0.547	0.597	0.647
LEAD WIDTH	b	0.31	–	0.53
MOLD LENGTH	D	4.80	4.90	5.00
MOLD WIDTH	E1	3.80	3.90	4.00
LEAD SPAN	E	5.80	6.00	6.20
LEAD PITCH	e	1.00 BSC		
LEAD LENGTH	L1	0.95	1.05	1.15
LEAD SOLE LENGTH	L	0.40	0.60	0.80
LEAD FORM ANGLE	θ	0°	–	8°

Document Change History

version number	state	Modify Content Summary	Revision Date	Reviser	approver
V1.0	N	new-built	20240801	He Wenbin	Yin Huaping
V1.1	M	parameter adjustment	20241212	Chen Yongzhao	Yin Huaping
V1.2	M	parameter adjustment	20250609	He Wenbin	Yin Huaping
V1.3	M	parameter adjustment	20250612	He Wenbin	Yin Huaping
V1.4	M	Standardize signal transmission distance and logic power supply voltage	20260709	Chen Yongzhao	Yin Huaping
V1.5	M	Format Adjustment	20260731	Chen Yongzhao	Yin Huaping