GENERAL DESCRIPTION

The LW67XX series is a group 70V high accuracy LDO regulator. The 3.0μA power consumption makes it ideal for most HV power-saving systems. The maximum operating voltage can be as high as 70V. The LW67XX can deliver 100mA output current.

The other features include current limiting protection, short circuit protection and thermal shutdown protection.

The LW67XX is available in ESOP-8, DFN2x2-6L, SOT89-3L and TO-252 packages.

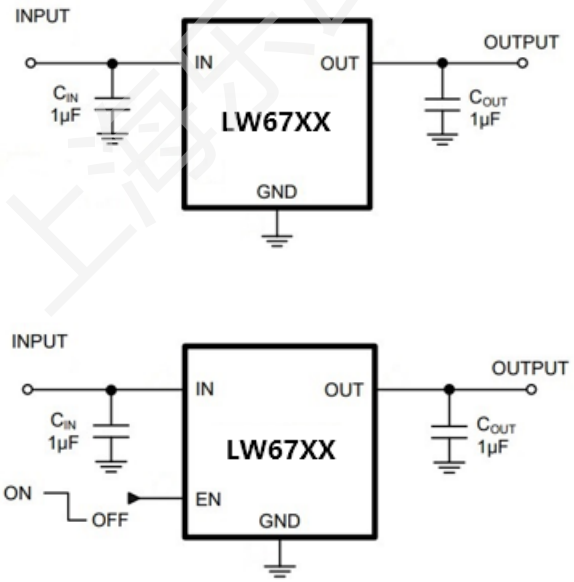
FEATURES

- Low Power Consumption: 3.0μA(Typ.)
- Operating Voltage Range: from 3.5V to 70V
- Output Voltage Range: from 2.5V to 15V
- Maximum Output Current: 100mA
- Output Accuracy: ±1.0% @+25℃
- Low Dropout Voltage:635mV@100mA/3.3V
- High PSRR: 80dB@1kHz, 10mA
- Low Temperature Coefficient
- Current Limiting Protection
- Output Short-Circuit Protection
- Over-Temperature Protection
- Fast Discharge Function
- Stable with 1μF Output Capacitor

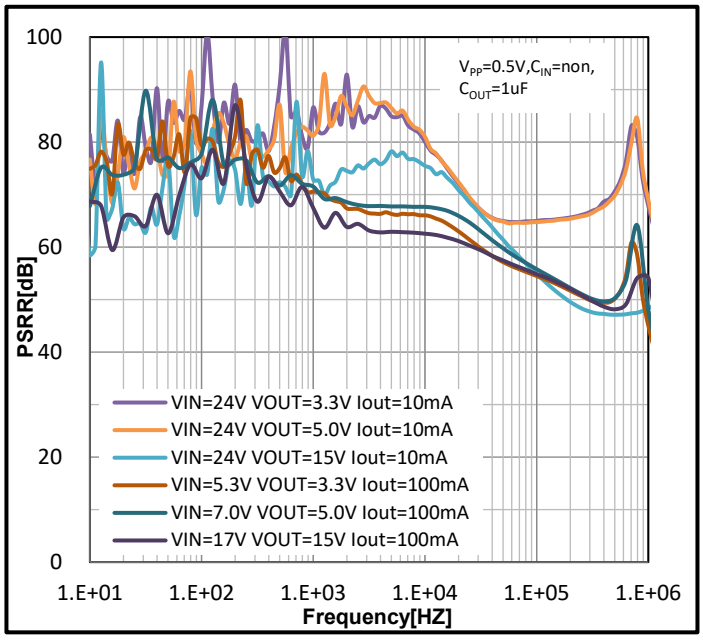
APPLICATIONS

- Battery Supplied Systems
- Telecom Systems
- Portable Audio & Video Equipment
- Ultra-Low Power Microcontroller

TYPICAL APPLICATION CIRCUIT



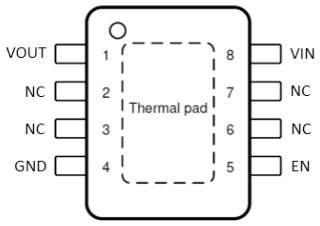
TYPICAL PERFORMANCE CHARACTERISTCS



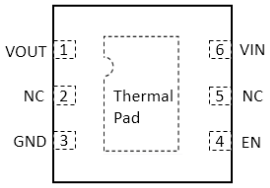
PIN DESCRIPTION:

PIN No				SYMBOL	DESCRIPTTION
ESOP-8	DFN2x2-6L	SOT89-3L (Type-B)	TO-252 /SOT89-3L (Type-C)		
8	6	3	1	VIN	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the Recommended Operating Conditions table and the Input and Output Capacitor Requirements section. Place the input capacitor as close to the output of the device as possible.
4	3	2、TAB	2、TAB	GND	Ground pin.
5	4	--	--	EN	Enable pin. Drive EN greater than $V_{EN(HI)}$ to turn on the regulator. Drive EN less than $V_{EN(LO)}$ to put the low-dropout regulator (LDO) into shutdown mode.
2,3,6,7	2,5	--	--	NC	No internal connection. Ground this pin for better thermal performance.
1	1	1	3	VOUT	Regulated output voltage pin. Connect a low-equivalent series resistance (ESR) capacitor to this pin. For best transient response, use the nominal recommended value or larger capacitor from OUT to GND. An internal pulldown resistor prevents a charge from remaining on OUT when the regulator is in shutdown mode ($V_{EN} < V_{EN\ (LOW)}$).
Thermal pad	Thermal pad	--	--	Pad	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

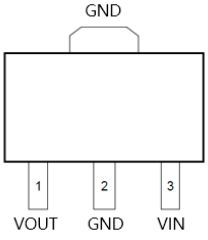
PIN ASSIGNMENT



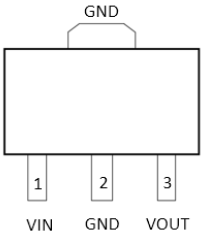
ESOP-8



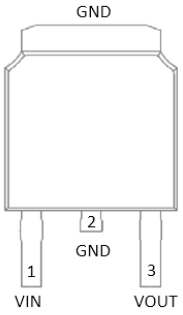
DFN2x2-6L



SOT89-3L(Type-B)



SOT89-3L(Type-C)



TO-252

MARK INFORMATION:

TO-252/SOT89-3L

XX: VOLTAGE

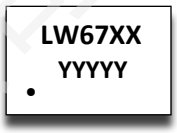
Y: DATE CODE



ESOP-8/ DFN2x2-6L

XX: VOLTAGE

YY: DATE CODE



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ABSOLUTE MAXIMUM RATINGS (1):

(T_A =25℃, unless otherwise specified.)

SYMBOL	ITEM		RATING	UNIT
V_{IN}	Supply Voltage		-0.3~80	V
V_{EN}	EN Pin Voltage		-0.3~80	V
V_{OUT}	V_{OUT} Pin Voltage		-0.3~16	V
$V_{(ESD)}$	ESD Susceptibility, HBM(2)		±2000	V
$R_{\theta JA}$	Junction-to-ambient Thermal Resistance(3)	ESOP-8	45	℃/W
		DFN2x2-6L	60	
		SOT89-3L	90	
		TO-252	35	
T_J	Junction Temperature Range		-40~150	℃
T_{STG}	Storage Temperature Range		-40~150	℃
T_{SOLDER}	Lead Temperature (Soldering)		260℃, 10s	

Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

2. per ANSI/ESDA/JEDEC JS-001

3. Device mounted on FR-4 PCB, Refer to JESD51-3 for detailed information on the board construction

RECOMMENDED OPERATING RANGE:

SYMBOL	ITEM	VALUE	UNIT
V_{IN}	V_{IN} Supply Voltage	3.5~70	V
V_{EN}	EN Pin Voltage	0~70	V
V_{OUT}	V_{OUT} Pin Voltage	2.5~15	V
I_{OUT}	Output Current	0~100	mA
T_J	Junction Temperature Range	-40~125	℃

ELECTRICAL CHARACTERISTICS:

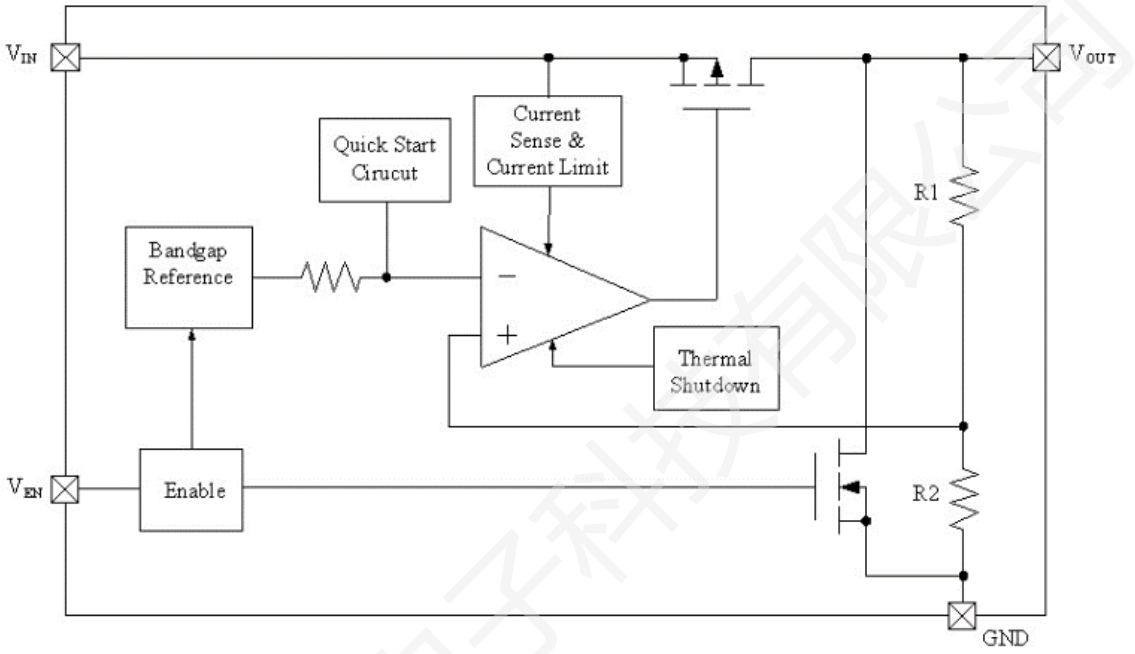
(V_{IN}=$V_{OUT(NOM)}$+1V or 2V, whichever is greater, C_{IN}= C_{OUT}=1μF, unless otherwise specified, typical values are at T_A = 25℃.)

Symbol	Parameter	Test Conditions		MIN	TYP	MAX	Units
V_{IN}	Input Voltage			3.5		70	V
V_{OUT}	Output Accuracy	I_{OUT}= 1mA		-1.0		+1.0	%
I_{LIM}	Current Limit(1)			100	150		mA
I_Q	Quiescent Current	V_{IN}=V_{EN}=V_{OUT}+1V, No Load	V_{OUT}≤6.0V		3.0	5.0	μA
			V_{OUT}＞6.0V		4.0	6.0	
I_{SHD}	Shutdown Current	V_{EN}=0V			0.35	1.0	μA
V_{DROP}	Dropout Voltage(1) (2)	I_{OUT}=100mA, V_{OUT}=3.3V			635		mV
		I_{OUT}=100mA, V_{OUT}=5.0V			580		
		I_{OUT}=100mA, V_{OUT}=15V			545		
ΔV_{OUT}/ (ΔV_{IN}*$V_{OUT(NOM)}$)	Line Regulation	V_{IN}= V_{OUT} +1V to 70V, I_{OUT}=1mA			0.01	0.02	%/V
ΔV_{OUT}	Load Regulation	1mA≤I_{OUT}≤100mA			30	60	mV
I_{SHORT}	Short Current(1)	V_{OUT}=0V			15		mA
V_{ENH}	EN High Voltage	V_{IN}=3.5V to 70V, I_{OUT}=1mA		1.5			V
V_{ENL}	EN Low Voltage					0.5	V
PSRR	Power Supply Rejection Ratio	V_{IN}= 4.3V, V_{OUT}=3.3V, V_{PP}=0.5V, C_{IN} =None, I_{OUT}=10mA	f=217Hz		83		dB
			f=1KHz		80		
			f=10KHz		71		
			f=100KHz		58		
T_{SD}	Thermal Shutdown	Temperature rising			160		℃
△T_{SD}	TSD Hysteresis	Temperature falling			30		℃
R_{DSCHG}	Output Discharge Resistance	V_{IN}=12V, V_{EN}=0V			80		Ω

NOTES:

1. Guaranteed by design
2. The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} =95%*$V_{OUT(NOM)}$

SIMPLIFIED BLOCK DIAGRAM:



DETAIL OPERATION DESCRIPTION:

The LW67XX Series is a low power consumption low drop-out voltage regulator. It consists of a current limiter circuit, a driver transistor, a precision reference voltage and an error correction circuit, and is compatible with low ESR ceramic capacitors. The current limiter's fold-back circuit operates as a short circuit protection as well as the output current limiter.

Current Limiting and Short-Circuit Protection

The current limit circuitry prevents damage to the MOSFET switch and the hub downstream port but can deliver load current up to the current limit threshold of typically 100mA through the switch. When a heavy load or short circuit is applied to an enabled switch, a large transient current may flow until the current limit circuitry responds. Once this current limit threshold is exceeded the device enters constant current mode until the thermal shutdown occurs or the fault is removed.

TYPICAL OPERATING CHARACTERISTICS:

（*Tested under* T_A *=25*°C, C_{IN}=C_{OUT}=1μF, unless otherwise specified）

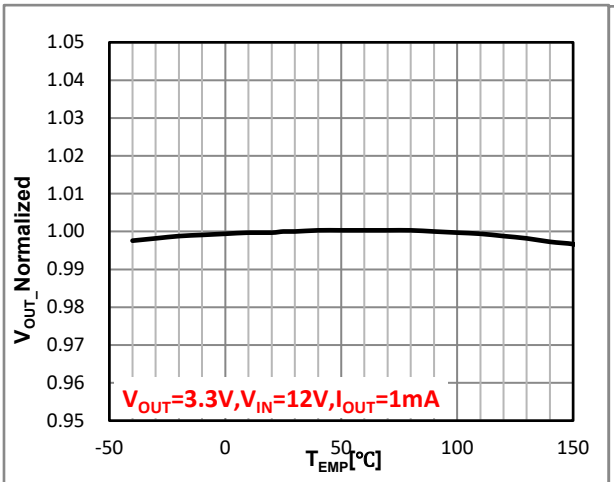


Figure 1. V_{OUT} vs Temperature

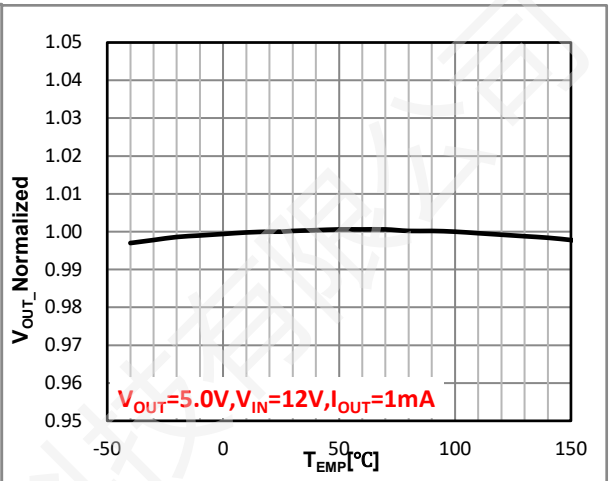


Figure 2. V_{OUT} vs Temperature

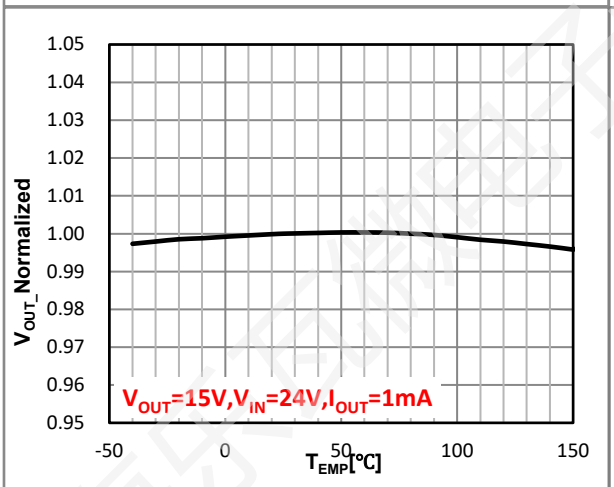


Figure 3. V_{OUT} vs Temperature

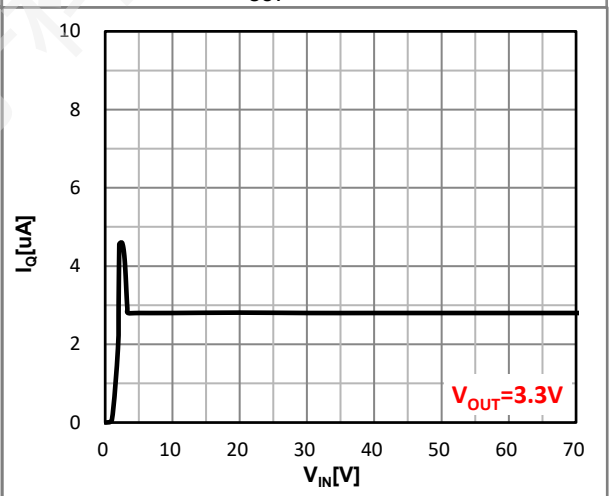


Figure 4. I_Q vs V_{IN}

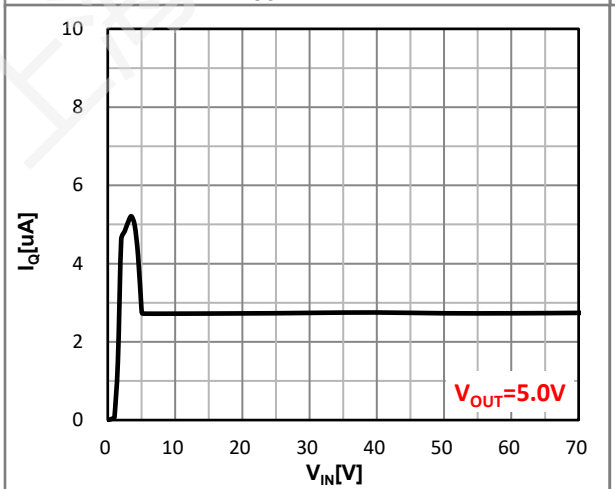


Figure 5. I_Q vs V_{IN}

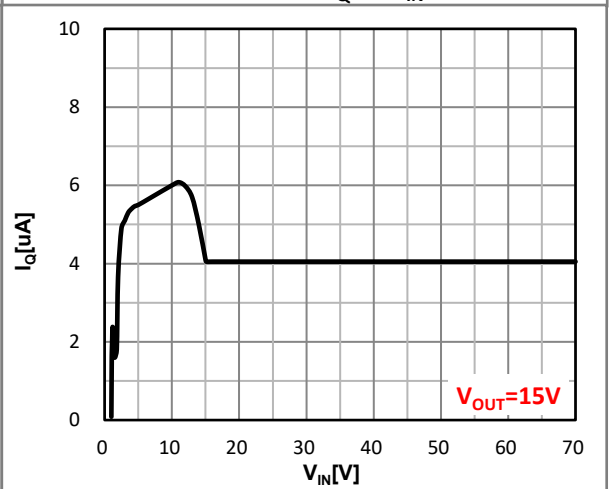


Figure 6. I_Q vs V_{IN}

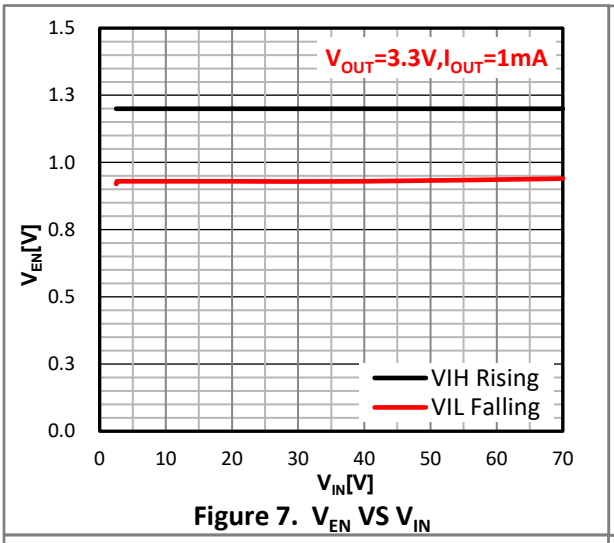


Figure 7. V_{EN} VS V_{IN}

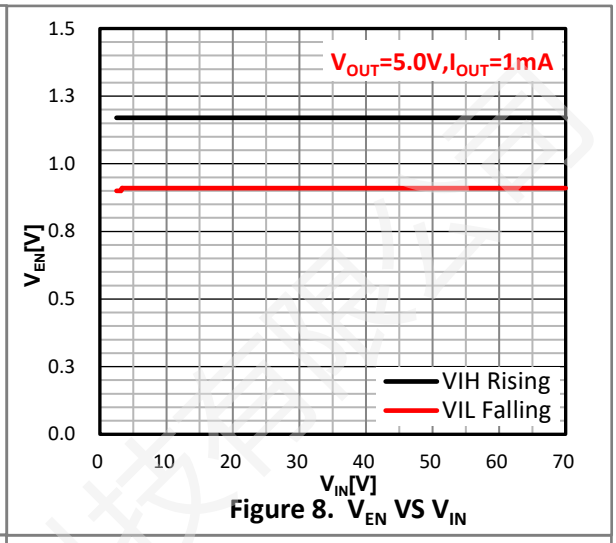


Figure 8. V_{EN} VS V_{IN}

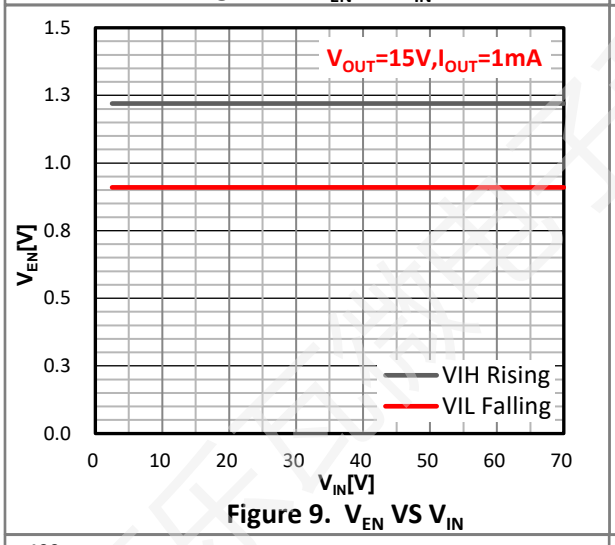


Figure 9. V_{EN} VS V_{IN}

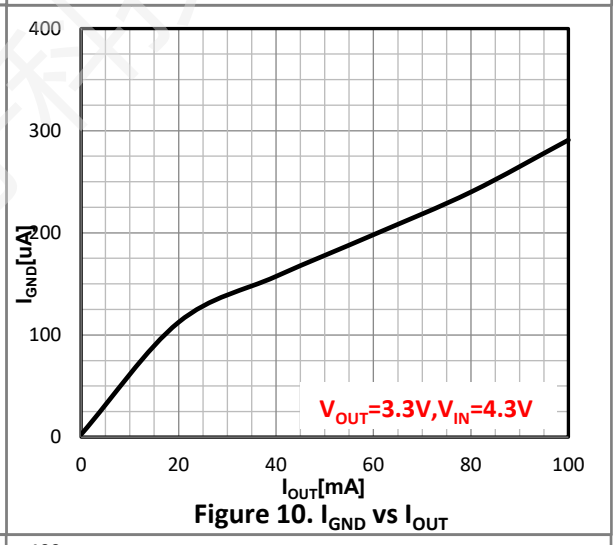


Figure 10. I_{GND} vs I_{OUT}

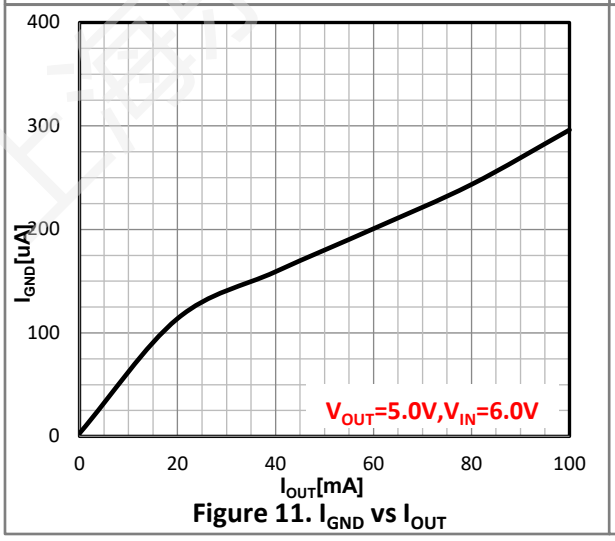


Figure 11. I_{GND} vs I_{OUT}

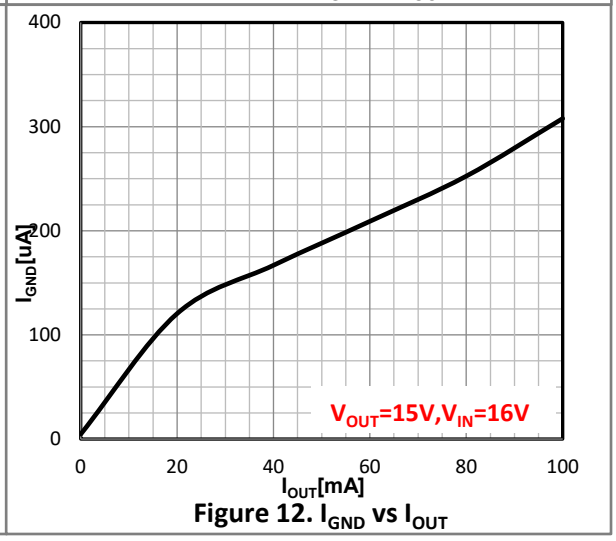


Figure 12. I_{GND} vs I_{OUT}

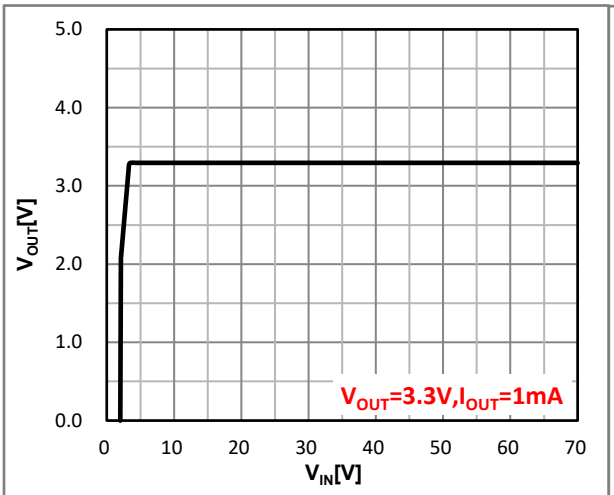


Figure 13. V_{OUT} vs V_{IN}

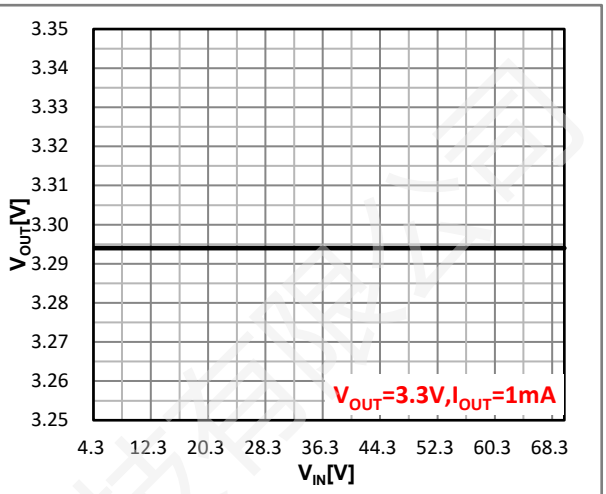


Figure 14. Line Regulation

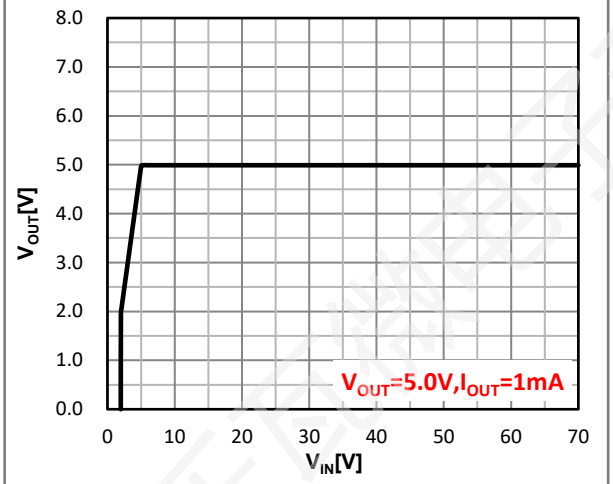


Figure 15. V_{OUT} vs V_{IN}

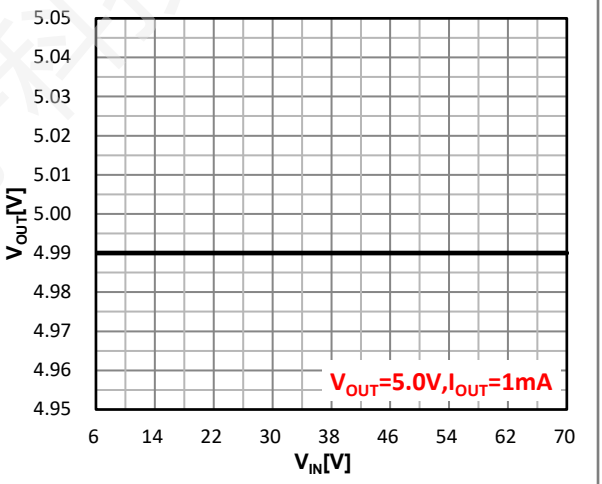


Figure 16. Line Regulation

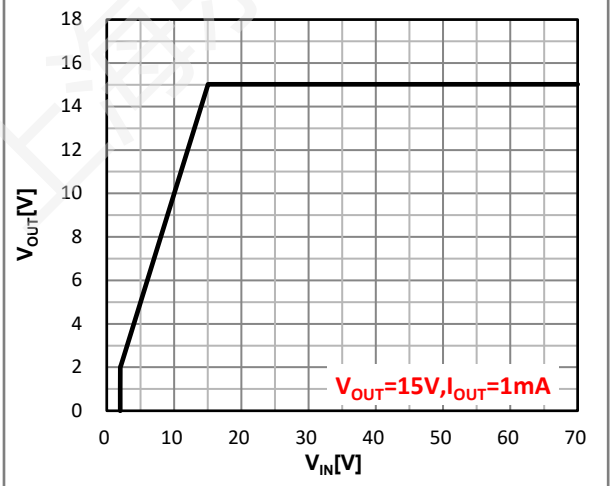


Figure 17. V_{OUT} vs V_{IN}

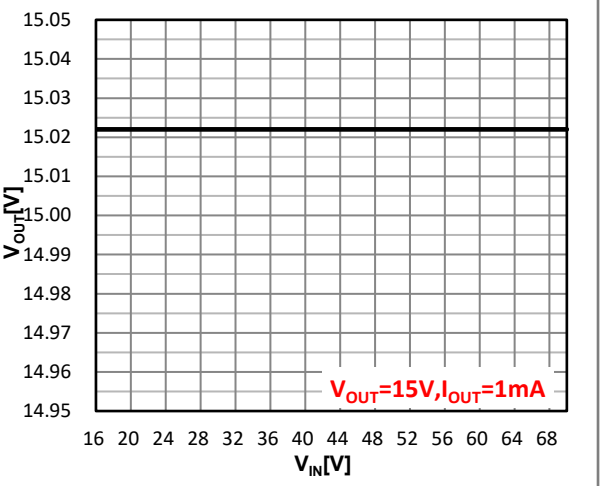


Figure 18. Line Regulation

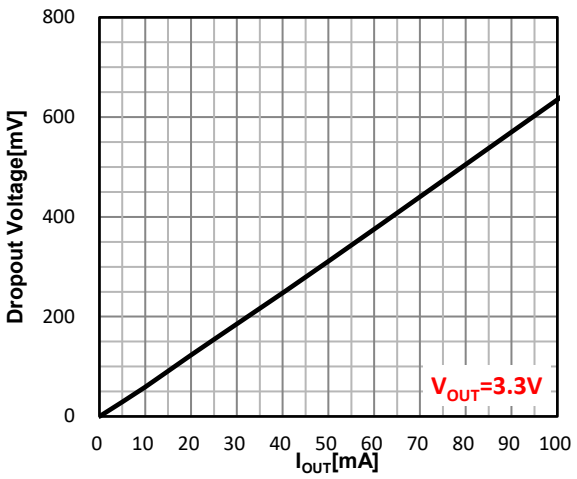


Figure 19. Dropout Voltage VS I_{OUT}

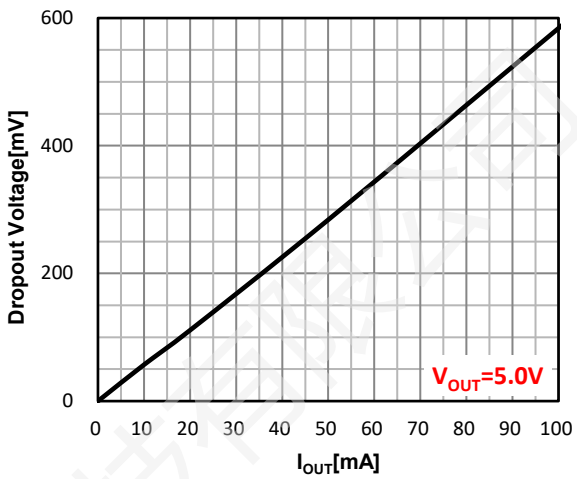


Figure 20. Dropout Voltage VS I_{OUT}

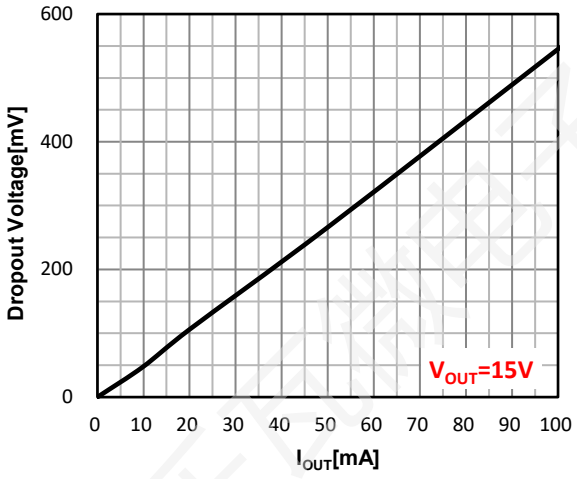


Figure 21. Dropout Voltage VS I_{OUT}

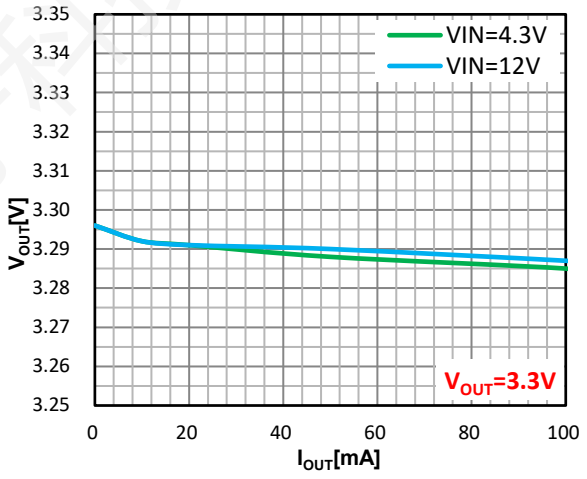


Figure 22. Load Regulation

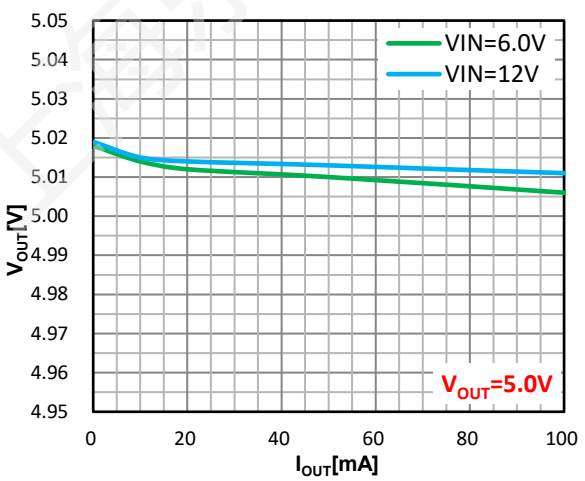


Figure 23. Load Regulation

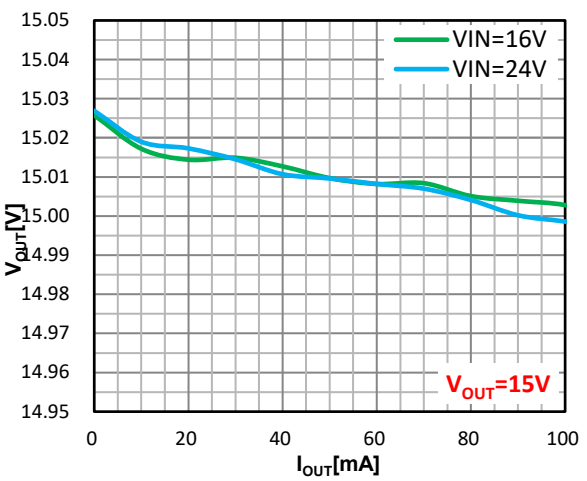
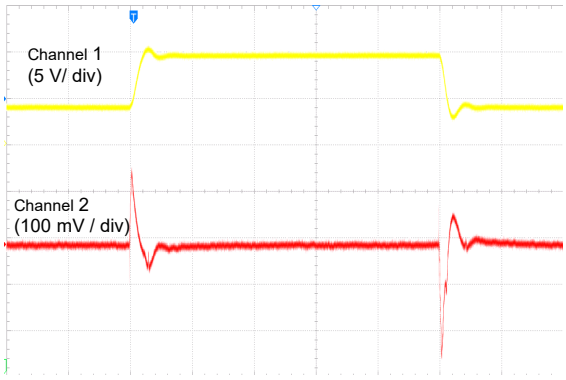


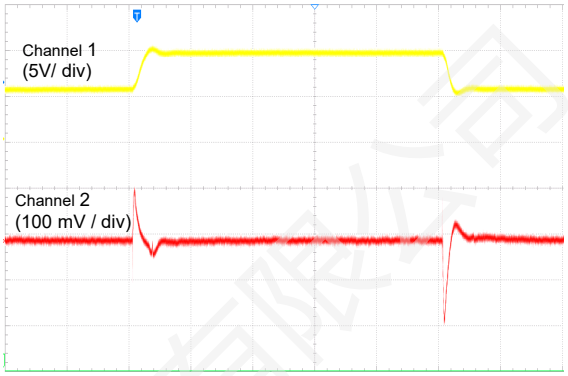
Figure 24. Load Regulation



Time (20 us / div)

Channel 1 = V_{IN}, Channel 2 =V_{OUT}, V_{IN}=4.3V→10V,
Tr=Tf=5us, V_{OUT}=3.3V, I_{OUT}=10mA

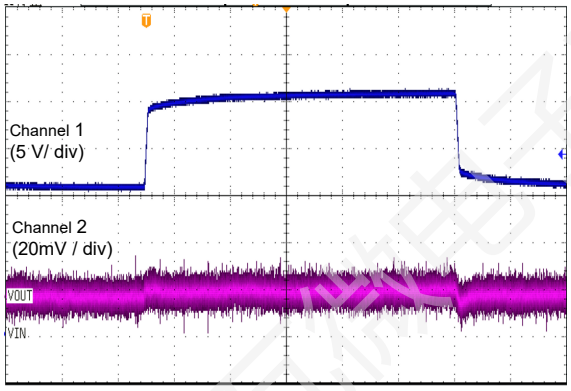
Figure 25. Line Transient



Time (20 us / div)

Channel 1 = V_{IN}, Channel 2 =V_{OUT}, V_{IN}=6.0V→10V,
Tr=Tf=5us, V_{OUT}=5.0V, I_{OUT}=10mA

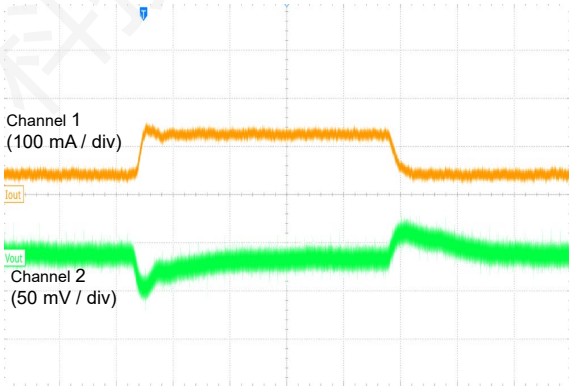
Figure 26. Line Transient



Time (20 us / div)

Channel 1 = V_{IN}, Channel 2 =V_{OUT}, V_{IN}=16V→24V,
Tr=Tf=5us, V_{OUT}=15V, I_{OUT}=10mA

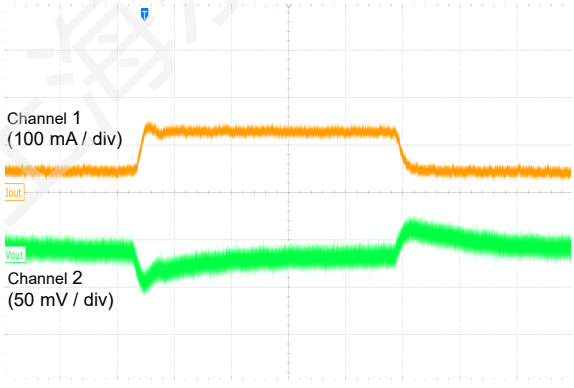
Figure 27. Line Transient



Time (100 us / div)

Channel 1 = I_{OUT}, Channel 2 =V_{OUT}, V_{IN}=4.3V, V_{OUT}=3.3V,
C_{IN}=C_{OUT}=1uF

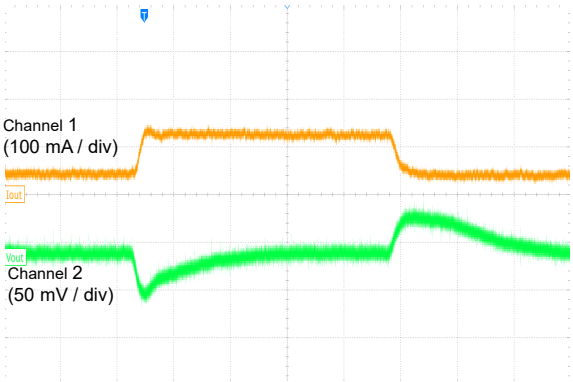
Figure 28. Load Transient (1 mA → 100 mA)



Time (100 us / div)

Channel 1 = I_{OUT}, Channel 2 =V_{OUT}, V_{IN}=6.0V, V_{OUT}=5.0V,
C_{IN}=C_{OUT}=1uF

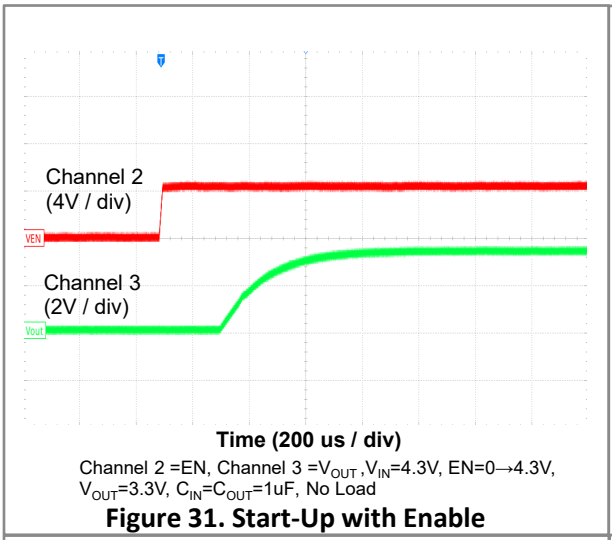
Figure 29. Load Transient (1 mA → 100 mA)



Time (100 us / div)

Channel 1 = I_{OUT}, Channel 2 =V_{OUT}, V_{IN}=16V, V_{OUT}=15V,
C_{IN}=C_{OUT}=1uF

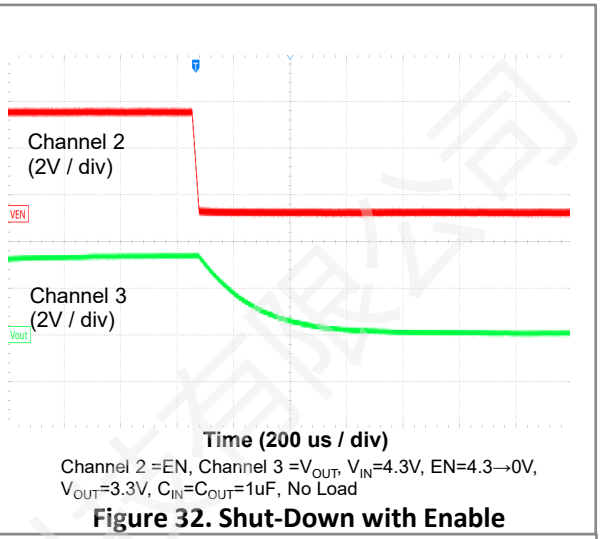
Figure 30. Load Transient (1 mA → 100 mA)



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT} ,V_{IN}=4.3V, EN=0→4.3V, V_{OUT}=3.3V, C_{IN}=C_{OUT}=1uF, No Load

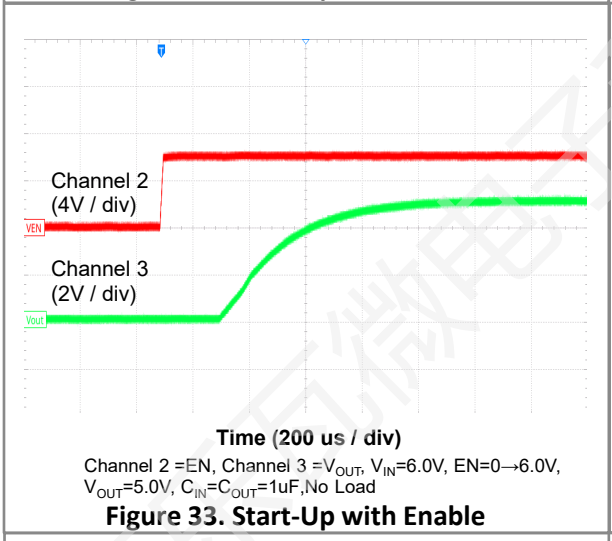
Figure 31. Start-Up with Enable



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=4.3V, EN=4.3→0V, V_{OUT}=3.3V, C_{IN}=C_{OUT}=1uF, No Load

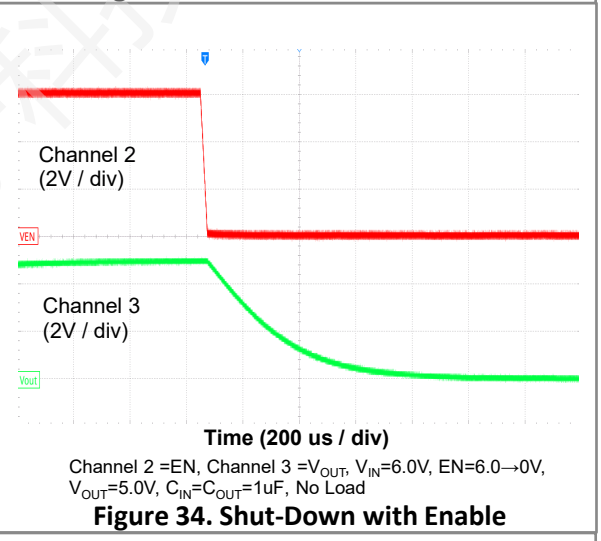
Figure 32. Shut-Down with Enable



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=6.0V, EN=0→6.0V, V_{OUT}=5.0V, C_{IN}=C_{OUT}=1uF,No Load

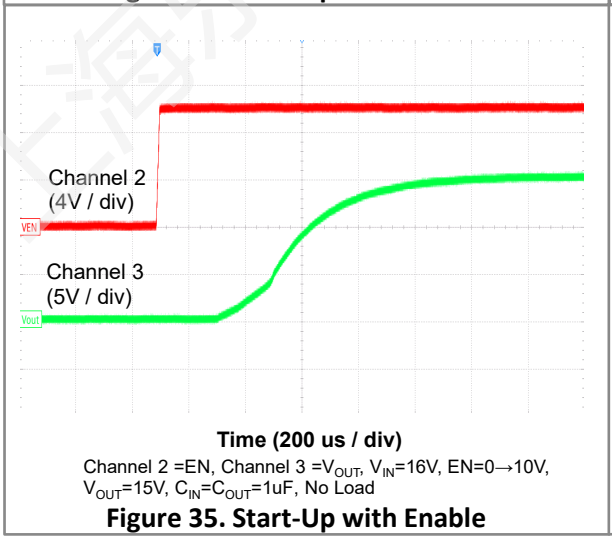
Figure 33. Start-Up with Enable



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=6.0V, EN=6.0→0V, V_{OUT}=5.0V, C_{IN}=C_{OUT}=1uF, No Load

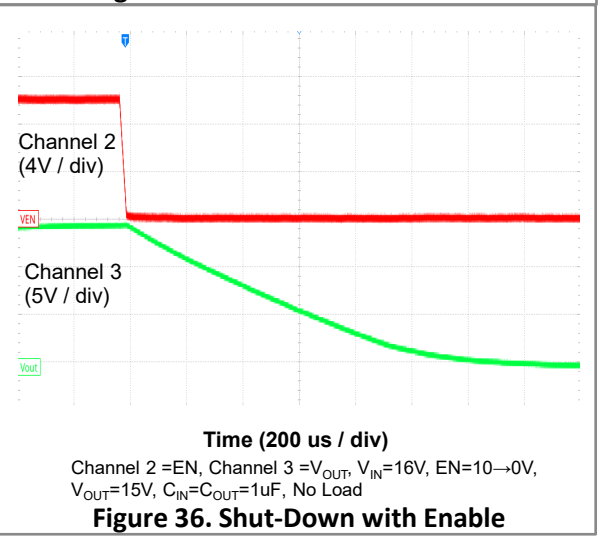
Figure 34. Shut-Down with Enable



Time (200 us / div)

Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=16V, EN=0→10V, V_{OUT}=15V, C_{IN}=C_{OUT}=1uF, No Load

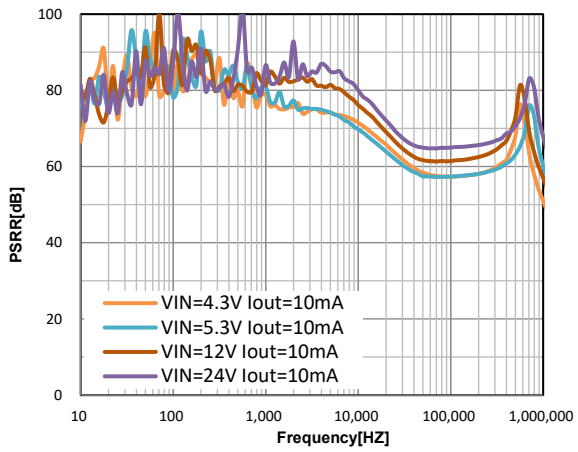
Figure 35. Start-Up with Enable



Time (200 us / div)

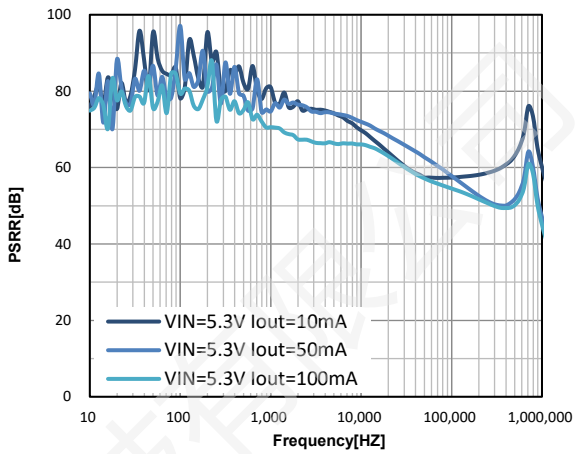
Channel 2 =EN, Channel 3 =V_{OUT}, V_{IN}=16V, EN=10→0V, V_{OUT}=15V, C_{IN}=C_{OUT}=1uF, No Load

Figure 36. Shut-Down with Enable



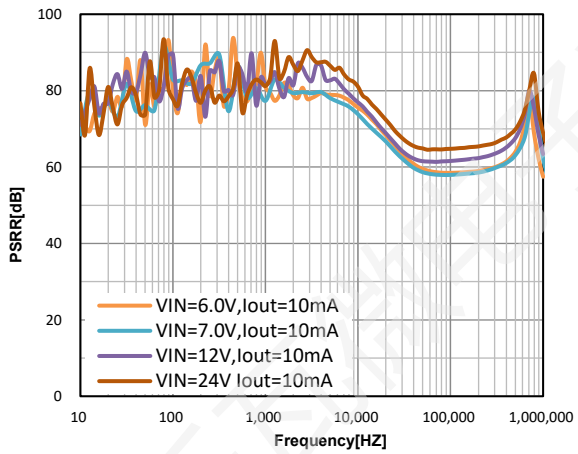
V_{OUT}=3.3V,V_{PP}=0.5V,C_{IN}=non,C_{OUT}=1uF,I_{OUT}=10mA

Figure 37. PSRR vs Frequency



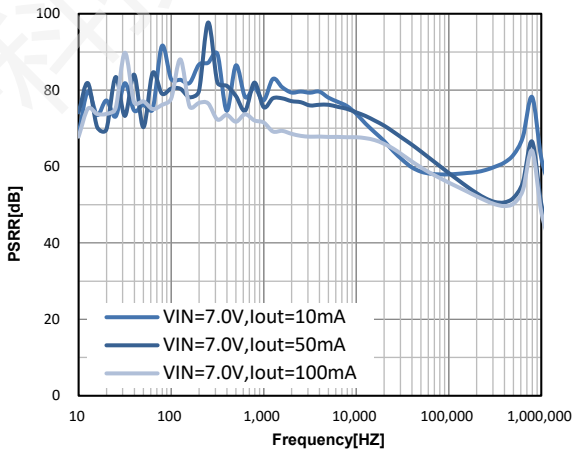
V_{OUT}=3.3V, V_{PP}=0.5V,C_{IN}=non,C_{OUT}=1uF,V_{IN}=V_{OUT}+2V

Figure 38. PSRR vs Frequency



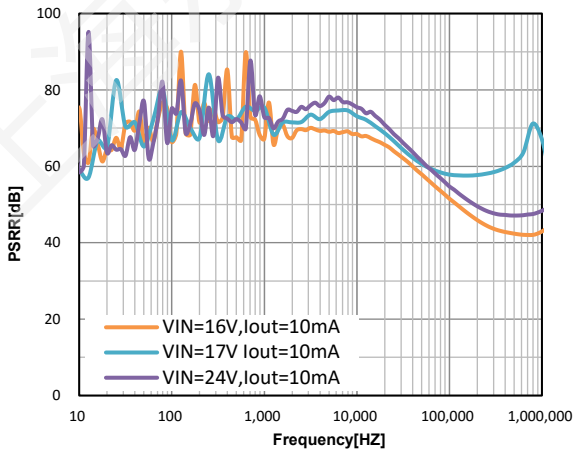
V_{OUT}=5.0V, V_{PP}=0.5V,C_{IN}=non, C_{OUT}=1uF,I_{OUT}=10mA

Figure 39. PSRR vs Frequency



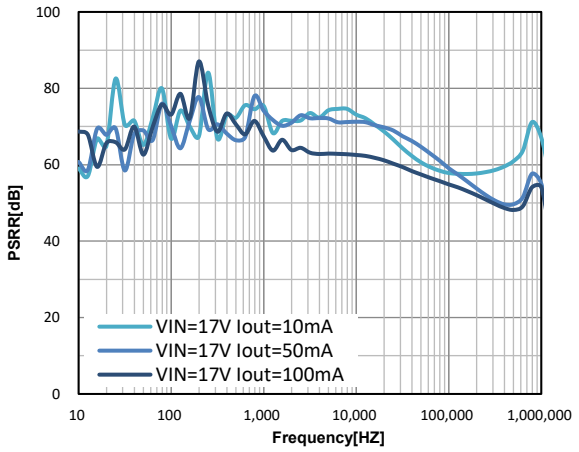
V_{OUT}=5.0V, V_{PP}=0.5V,C_{IN}=non, C_{OUT}=1uF,V_{IN}=V_{OUT}+2V

Figure 40. PSRR vs Frequency



V_{OUT}=15V, V_{PP}=0.5V,C_{IN}=non, C_{OUT}=1uF,I_{OUT}=10mA

Figure 41. PSRR vs Frequency



V_{OUT}=15V, V_{PP}=0.5V,C_{IN}=non, C_{OUT}=1uF,V_{IN}=V_{OUT}+2V

Figure 42. PSRR vs Frequency

APPLICATION INFORMATION:

- **Input Capacitor Selection**

Like any low-dropout regulator, the external capacitors used with the LW67XX Series must be carefully selected for regulator stability and performance. Using a capacitor whose value is >=1μF on the LW67XX Series input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

- **Output Capacitor Selection**

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LW67XX Series is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF on the LW67XX Series output ensures stability. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the LW67XX Series and returned to a clean analog ground.

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- **Layout considerations**

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for VIN and VOUT, with each ground plane connected only at the GND pin of the device.

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ORDER INFORMATION:

LW67①②③④⑤⑥

Designator	Item	Symbol	Description
①②	Output Voltage	25~A5	e.g.2.8V→①=2,②=8
③④⑤⑥	Packages	ES8H	ESOP-8
		N22G	DFN2x2-6L
		B89C	SOT89-3L(Type-B)
		C89C	SOT89-3L(Type-C)
		A52B	TO-252

Part #	Output Voltage	Package	Shipping
LW6725ES8H	2.5V	ESOP-8	4000 Pcs / Tape & Reel
LW6730ES8H	3.0V		
LW6733ES8H	3.3V		
LW6740ES8H	4.0V		
LW6750ES8H	5.0V		
LW6790ES8H	9.0V		
LW67A2ES8H	12V		
LW67A5ES8H	15V		
LW6725N22G	2.5V	DFN2x2-6L	3000 Pcs/ Tape & Reel
LW6730N22G	3.0V		
LW6733N22G	3.3V		
LW6740N22G	4.0V		
LW6750N22G	5.0V		
LW6790N22G	9.0V		
LW67A2N22G	12V		
LW67A5N22G	15V		

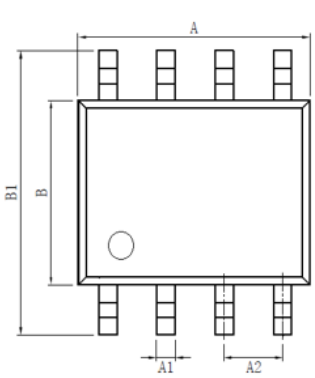
Part #	Output Voltage	Package	Shipping
LW6725B89C	2.5V	SOT89-3L(Type-B)	1000 Pcs / Tape & Reel
LW6730B89C	3.0V		
LW6733B89C	3.3V		
LW6740B89C	4.0V		
LW6750B89C	5.0V		
LW6790B89C	9.0V		
LW67A2B89C	12V		
LW67A5B89C	15V		
LW6725C89C	2.5V	SOT89-3L(Type-C)	1000 Pcs / Tape & Reel
LW6730C89C	3.0V		
LW6733C89C	3.3V		
LW6740C89C	4.0V		
LW6750C89C	5.0V		
LW6790C89C	9.0V		
LW67A2C89C	12V		
LW67A5C89C	15V		
LW6725A52B	2.5V	TO-252	2500 Pcs / Tape & Reel
LW6730A52B	3.0V		
LW6733A52B	3.3V		
LW6740A52B	4.0V		
LW6750A52B	5.0V		
LW6790A52B	9.0V		
LW67A2A52B	12V		
LW67A5A52B	15V		

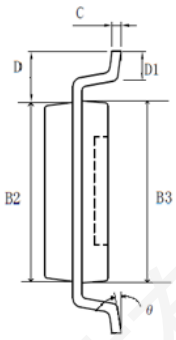
If customers have special output voltage requirements, please contact us.

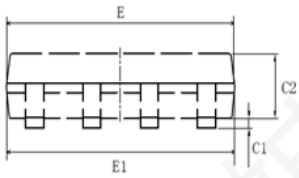
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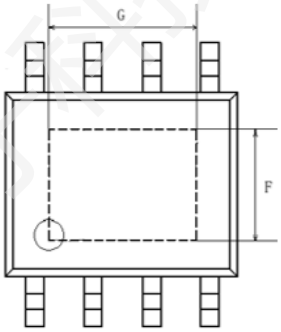
PACKAGE OUTLINE:

ESOP-8 Package





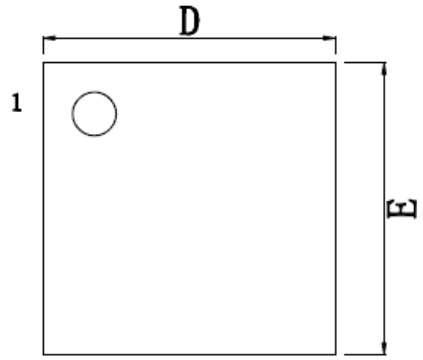




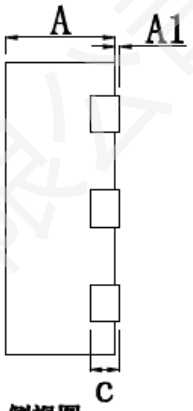
Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	4.70	4.90	5.10
A1	0.37	0.42	0.47
A2	1.22	1.27	1.32
B	3.70	3.90	4.10
B1	5.80	6.00	6.20
B2	3.75	3.85	3.95
B3	3.80	3.90	4.00
C	0.16	0.21	0.26
C1	0.04	0.11	0.18
C2	1.30	1.40	1.50
D	0.95	1.05	1.15
D1	0.40	0.50	0.60
E	4.65	4.85	5.05
E1	4.70	4.90	5.10
θ	REF 8°		
G	3.20	3.35	3.50
F	2.20	2.35	2.50

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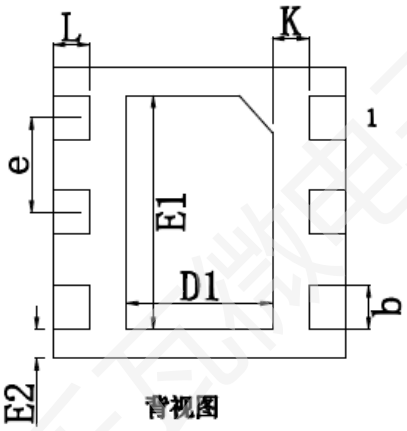
DFN2x2-6L Package



俯视图



侧视图

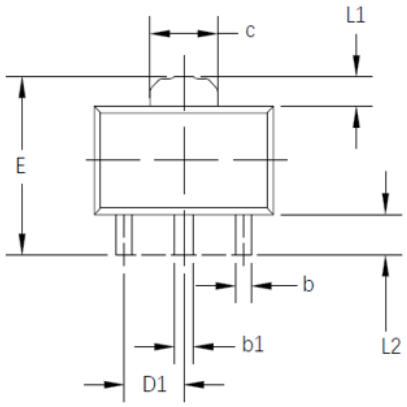


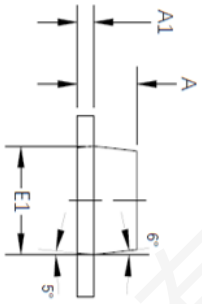
背视图

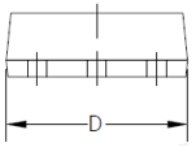
SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.25	0.30	0.35
c	0.203 TYP		
D	1.95	2.00	2.05
D1	0.90	1.00	1.10
E	1.95	2.00	2.05
E1	1.55	1.60	1.65
E2	0.20 REF		
e	0.65 BSC		
K	0.25 REF		
L	0.20	0.25	0.30

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SOT89-3L Package



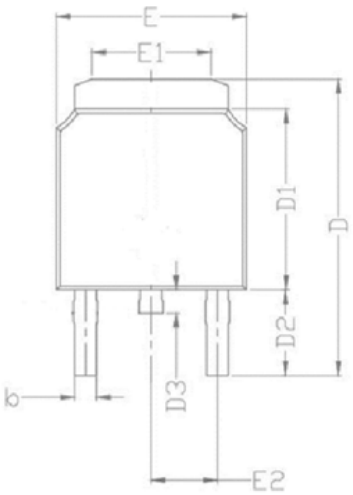


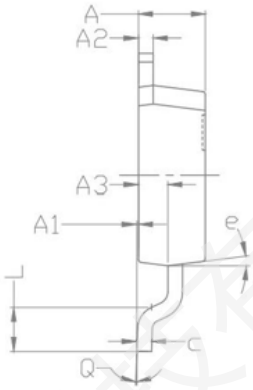


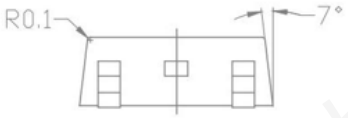
COMMON DIMENSION (MM)			
PKG	SOT89-3L		
Symbol	MIN	NOM	MAX
A	1.450	1.500	1.550
A1	0.350	0.400	0.450
b	0.350	0.430	0.500
b1	0.430	0.500	0.570
C	1.650	1.700	1.750
D	4.450	4.550	4.700
D1	1.470	1.500	1.550
E	4.100	4.200	4.300
E1	2.450	2.550	2.650
L1	0.630	0.700	0.770
L2	0.900	0.950	1.000

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TO-252 Package







COMMON			
PKG	TO-252		
Symbol	Min	Nom	Max
A	2.200	2.300	2.400
A1	0.000	0.075	0.150
A2	0.460	0.525	0.590
A3	0.960	1.010	1.060
b	0.640	0.720	0.800
C	0.450	0.515	0.580
D	9.800	10.025	10.350
D1	6.000	6.100	6.200
D2	2.850	2.900	3.100
D3	0.490	0.800	1.000
E	6.400	6.550	6.700
E1	4.050	4.130	4.600
E2	2.250	2.286	2.300
L	1.400	1.550	1.700
e	7°	8°	9°
Q	0°	5°	10°

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Revision History:

Revision	Date	Descriptions
Rev 0.1	Nov.2022	Initial Version
Rev 0.2	Sep.2023	Adjust product definition
Rev 1.0	Jan.2024	Formal Version
Rev 1.1	Oct.2024	Add Package DFN2x2-6L
Rev 1.2	Aug.2025	Distinguish I_Q under different conditions in Ectable
Rev 1.3	Apr.2026	Update Eletrical Characteristcs & Package Outline
Rev 1.4	Sep.2026	Update Absolute Maximum Ratings & Typical Operating Characteristics

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