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Features

- RTC Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year with Leap-Year Compensation Valid Up to 2100
- Support 1.8V/3.0V/3.3V operation
- 56-Byte Battery-Backed NV RAM for Data Storage
- I²C Serial Interface
- Programmable Square-Wave Output Signal
- Automatic Power-Fail Detect and Switch Circuitry
- Operating Temperature: -40 ~ 85℃

Applications

- Handhelds (GPS, POS Terminal)
- Consumer Electronics (Set-Top Box, Digital Recording, Network Appliance)
- Office Equipment (Fax/Printer, Copier)
- Medical (Glucometer, Medicine Dispenser)
- Telecommunications (Router, Switcher, Server)
- Other (Utility Meter, Vending Machine, Thermostat, Modem)

Typical application circuit

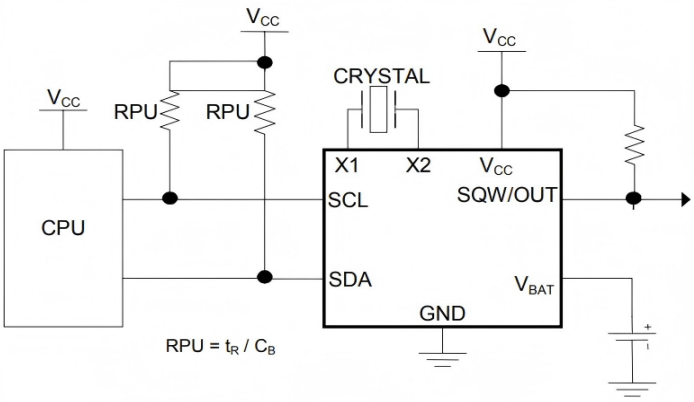

Figure 1 Typical application circuit

Description

The DS1338Z-NF serial real-time clock (RTC) is a low-power, full binary-coded decimal (BCD) clock/calendar plus 56 bytes of NV SRAM. Address and data are transferred serially through an I2C interface. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The DS1338Z-NF has a built-in power-sense circuit that detects power failures and automatically switches to the battery supply.

Ordering Information:

Ordering Code	Package	Package Description
DS1338Z-NF		SOP-8

Pb-free and Green

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Pin Configurations

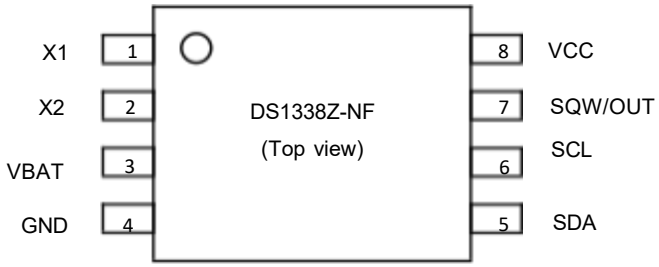

Figure 2 SOP-8 pin configuration (Top view)

Pin Name	Pin No. SOP-8 / MSOP-8	Description
X1	1	Pin X1 can optionally be connected to an external 32 .768kHz oscillator. Pin X2 , is floated if an external oscillator is connected to pin X1 .
X2	2	
VBAT	3	+ 3V Battery Input.
GND	4	Ground. DC power is provided to the device on these pins.
SDA	5	Serial Data. Input/ output pin for the I2C serial interface. It is open drain and requires an external pull up resistor.
SCL	6	Serial Clock. Used to synchronize data movement on the serial interface
SQW/OUT	7	Square-Wave/Output Driver .
VCC	8	Primary Power Supply.

Part Number Information

Part Number	
PN1	PN2
FRTC1338S	DS1338Z-NF

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Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
T_{store}	Storage Temperature	-55	-	+150	℃
T_{op}	Operating Temperature Range	-40	-	+85	℃
V_{IN}	Voltage Range on Any Pin Relative to Ground	-0.3	-	6	V

Note:
Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Symbol	Parameter	CONDITIONS	MIN	TYP	MAX	Unit
VCC	Positive DC Supply Voltage	DS1338Z-NF	2.97	3.3	3.63	V
VIH	SCL/SDA input		0.7 x VCC	-	VCC + 0.3	V
VIL	SCL/SDA input		-0.3	-	+0.3 x VCC	V
VPF	Power-Fail Voltage	DS1338Z-NF	2.7	2.82	2.97	V
VBAT	Battery Voltage*2		1.3	3.0	3.7	V

Note:
1. Limits at -40°C are guaranteed by design and not production tested.
2. All voltages are referenced to ground

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DC Electrical Characteristics

Unless otherwise specified, -40 ° C≤T_A≤ 85 ° C , ($V_{CC(MIN)}$ ≤V_{CC}≤ $V_{CC(MAX)}$)* 1

Symbol	Parameter	Test Conditions*1		MIN	TYP	MAX	Unit
V_{BAT}	Battery Voltage*2			1.3		3.7	V
I_{LI}	Input Leakage	SCL only		-	-	1	µA
I_{LO}	I/O Leakage	SDA and SQW/OUT			-	1	µA
I_{OLSDA}	SDA Logic 0 Output	V_{CC} > 2V; V_{OL} = 0.4V		-	-	3	mA
		V_{CC} < 2V; V_{OL} = 0.2 V_{CC}		-	-	3	mA
I_{OLSQW}	SQW/OUT Logic 0 Output	V_{CC} > 2V; V_{OL} = 0.4V		-	-	3	mA
		1.71V < V_{CC} < 2V; V_{OL} = 0.2 V_{CC}		-	-	3	
		1.3V < V_{CC} < 1.71V; V_{OL} = 0.2 V_{CC}		-	-	250	mA
I_{CCA}	Active Supply Current Supply Current	SCL clocking at max frequency = 400kHz	DS1338Z-NF	-	120	200	µA
I_{CCS}	Standby Current	Specified with the I2C bus inactive	DS1338Z-NF	-	85	125	µA
I_{BATLKG}	V_{BAT} Leakage Current (V_{CC} Active)				25	100	nA
$I_{BATOSC1}$	V_{BAT} Current (O_{SC} ON)	V_{BAT} = 3.7V , SQW/OUT OFF*3			400	1200	nA
$I_{BATOSC2}$	V_{BAT} Current (O_{SC} ON)	V_{BAT} = 3.7V , SQW/OUT ON (32kHz) *3			570	1400	nA
I_{BATDAT}	V_{BAT} Data-Retention Current (O_{SC} Off)	V_{BAT} = 3.7V*2			10	100	nA

Note:
1. Limits at -40°C are guaranteed by design and not production tested.
2. All voltages are referenced to ground
3. A fast-mode device can be used in a standard-mode system, but the requirement tSU:DAT ⩾ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tR MAX + tSU:DAT = 1000 + 250 = 1250ns before the SCL line is released.

Crystal Specifications

Symbol	Parameter	MIN	TYP	MAX	Units
f_O	Nominal Frequency		32.768		kHZ
ESR	Series Resistance			45	kΩ
C_L	Load Capacitance		12.5		pF

Note:
1. The crystal, traces, and crystal input pins should be isolated from RF generating signals.

AC Electrical characteristics

(TA = -40°C to +85°C) *1

Symbol	Parameter	Test Conditions*1	MIN	TYP	MAX	Unit
f_{SCL}	SCL Clock Frequency	Fast mode	100		400	kHz
		Standard mode			100	kHz
t_{BUF}	Bus Free Time Between STOP and START Condition	Fast mode	1.3			μs
		Standard mode	4.7			
$t_{HD:STA}$	Hold Time (Repeated) START Condition*2	Fast mode	0.6			μs
		Standard mode	4.0			
t_{LOW}	LOW Period of SCL Clock	Fast mode	1.3			μs
		Standard mode	4.7			
t_{HIGH}	HIGH Period of SCL Clock	Fast mode	0.6			μs
		Standard mode	4.0			
$t_{SU:STA}$	Setup Time for Repeated START Condition	Fast mode	0.6			μs
		Standard mode	4.7			
$t_{HD:DAT}$	Data Hold Time*3/4	Fast mode	0		0.9	μs
		Standard mode	0			
$t_{SU:DAT}$	Data Setup Time*5	Fast mode	100			ns
		Standard mode	250			
t_R	Rise Time of Both SDA and SCL Signals *6	Fast mode	20 + 0.1CB		300	ns
		Standard mode	20 + 0.1CB		1000	
t_F	Fall Time of Both SDA and SCL Signals *6	Fast mode	20 + 0.1CB		300	ns
		Standard mode	20 + 0.1CB		300	
$t_{SU:STO}$	Setup Time for STOP Condition	Fast mode	0.6			μs
		Standard mode	4.0			
C_B	Capacitive Load for Each Bus Line*6				400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL) *7				10	pF
t_{OSF}	Oscillator Stop Flag (OSF) Delay*8			100		ms

FRTC

Note:

1. Limits at -40°C are guaranteed by design and not production tested.
2. After this period, the first clock pulse is generated
3. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL
4. The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
5. A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geqslant$ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ MAX} + t_{SU:DAT} = 1000 + 250 = 1250$ns before the SCL line is released.
6. C_B—total capacitance of one bus line in pF
7. Guaranteed by design. Not production tested
8. The parameter t_{OSF} is the time period the oscillator must be stopped for the OSF flag to be set over the voltage range of $0.0V \leqslant V_{CC} \leqslant V_{CC\ MAX}$ and $1.3V \leqslant V_{BAT} \leqslant 3.7V$

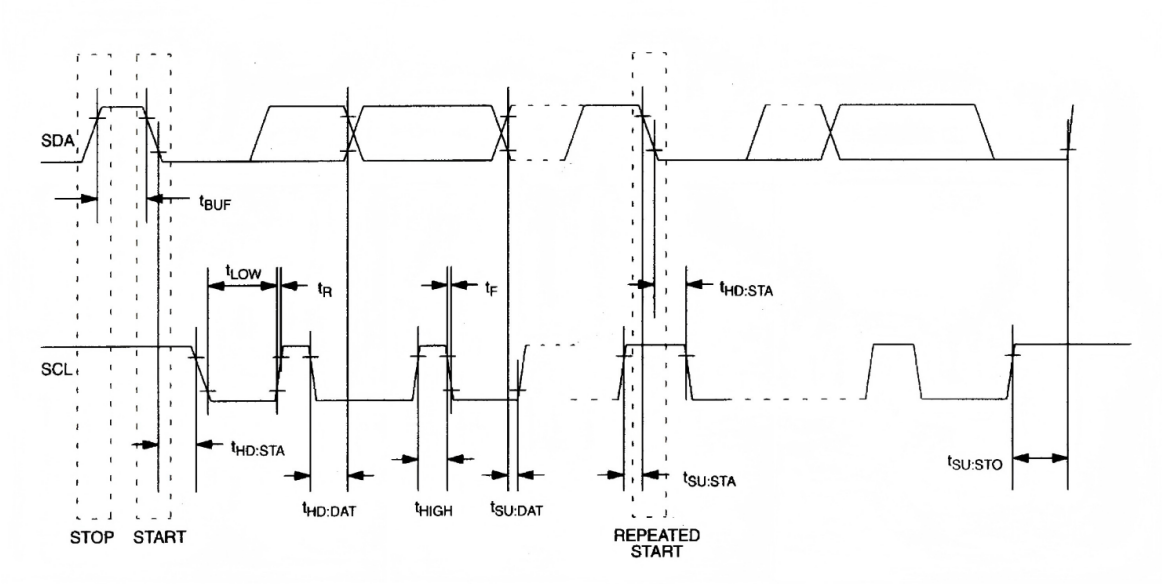


Figure 3 Timing Diagram

Power-Up/Power-Down Characteristics

(TA = -40°C to +85°C) *1

Symbol	Parameter	Test Conditions*1	MIN	TYP	MAX	Unit
t_{REC}	Recovery at Power-Up*2				2	ms
t_{VCCF}	V_{CC} Fall Time	V_{PF}(MAX) to V_{PF}(MIN)	300			μs
t_{VCCR}	V_{CC} Rise Tim	V_{PF}(MIN) to V_{PF}(MAX)	0			μs

Note:
1. Limits at -40°C are guaranteed by design and not production tested.
2. This delay applies only if the oscillator is enabled and running. If the oscillator is disabled or stopped, no power-up delay occurs.

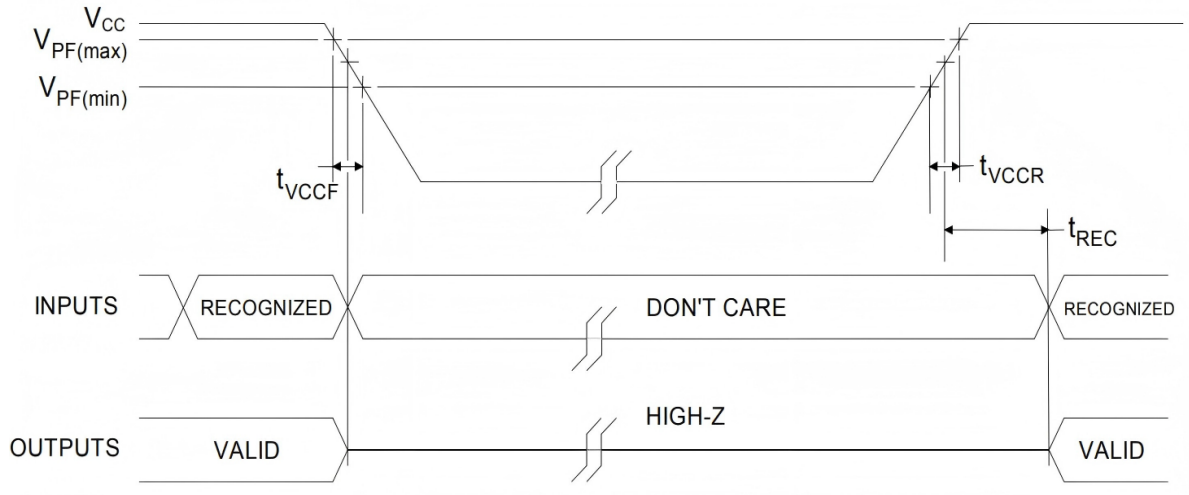


Figure 4 Power-Up/Power-Down Timing

Functional Description

The DS1338Z-NF serial RTC is a low-power, full BCD clock/ calendar plus 56 bytes of NV SRAM. Address and data are transferred serially through an I2C interface. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The DS1338Z-NF has a built-in power-sense circuit that detects power failures and automatically switches to the battery supply . The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 12 .5 pF. Pin X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, pin X2, is floated if an external oscillator is connected to pin X1 . An external 32. 768 kHz oscillator can also drive the DS1338Z-NF. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

DS1338Z-NF has a Backup supply input for any standard 3V lithium cell or other energy source. V_{BAT} voltage must be held between the minimum and maximum limits for proper operation. If a backup supply is not required, V_{BAT} must be grounded. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected to the device and V_{CC} is below V_{PF} , reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage.

When enabled and the SQWE bit set to 1, the SQW/OUT pin outputs one of four square-wave frequencies (1Hz, 4kHz, 8kHz, 32kHz). It is open drain and requires an external pullup resistor. Operates with either V_{CC} or V_{BAT} applied.

Application Information

The DS1338Z-NF operates as a slave device on the serial bus.

Access is obtained by implementing a START condition and providing a device identification code, followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF} . However, when V_{CC} falls below V_{PF} , the internal clock registers are blocked from any access. If V_{PF} is less than V_{BAT} , the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{PF} . If V_{PF} is greater than V_{BAT} , the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{BAT} . The registers are maintained from the V_{BAT} source until V_{CC} is returned to nominal levels. The block diagram shows the main elements of the DS1338Z-NF.

An enable bit in the seconds register controls the oscillator. Oscillator startup times are highly dependent upon crystal characteristics, PC board leakage , and layout. High ESR and excessive capacitive loads are the major contributors to long start-up times. A circuit using a crystal with the recommended characteristics and proper layout usually starts within 1 second.

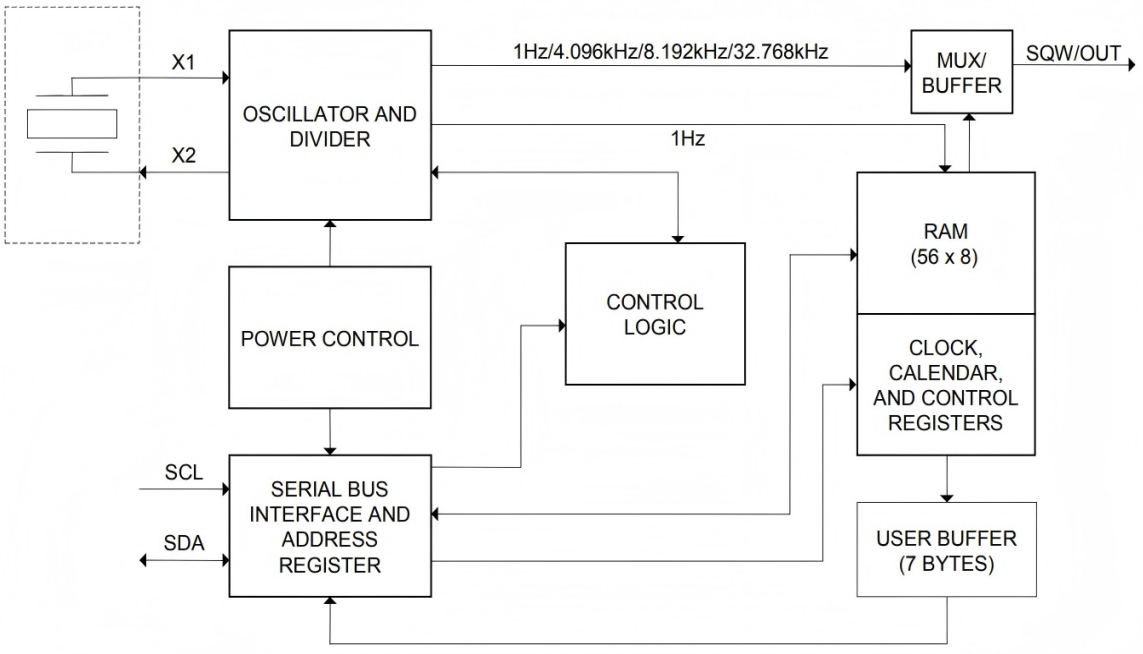


Figure 5 Block Diagram

Oscillator Circuit

DS1338Z-NF uses an external 32 .768kHz crystal.
The oscillator circuit does not require any external resistors or capacitors to operate . Figure:
Oscillator Circuit Showing Internal Bias Network shows a functional schematic of the oscillator circuit.
The startup time is usually less than 1 second when using a crystal with the specified characteristics .

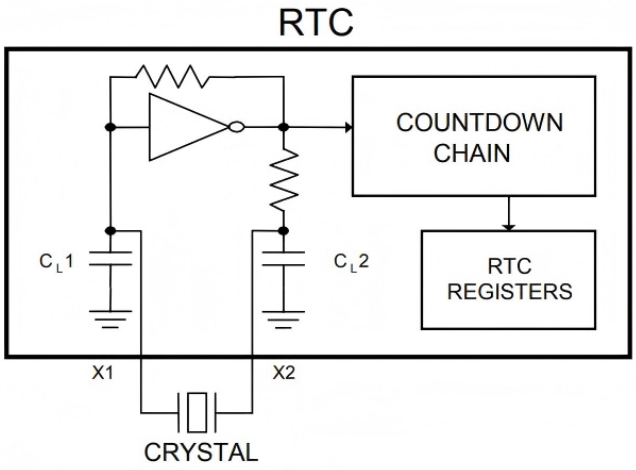


Figure 6 Oscillator Circuit Showing Internal Bias Network

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Crystal frequency drift caused by temperature shifts creates additional error. External circuit noise coupled into the oscillator circuit can result in the clock running fast.

RTCAnd RAM Address Map

The RTC registers and control register are located in address locations 00h to 07h. The RAM registers are located in address locations 08h to 3Fh. During a multibyte access, when the register pointer reaches 3Fh (the end of RAM space) it wraps around to location 00h (the beginning of the clock space). On an I2C START, STOP, or register pointer incrementing to location 00h , the current time and date is transferred to a second set of registers. The time and date in the secondary registers are read in a multibyte data transfer, while the clock continues to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Clock And Calendar

The time and calendar information is obtained by reading the appropriate register bytes. See Figure RTC and RAM Address Map for the RTC registers. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the BCD format. Bit 7 of Register 0 is the clock halt (CH) bit. When this bit is set to 1, the oscillator is disabled. When cleared to 0, the oscillator is enabled. The clock can be halted whenever the timekeeping functions are not required, which decreases V_{BAT} current.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i . e . , if 1 equals Sunday, then 2 equals Monday, and so on) . Illogical time and date entries result in undefined operation .

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any start or stop and when the register pointer rolls over to zero . The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge from the DS1338Z-NF.
Once the countdown chain is reset, to avoid rollover issues the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enabled, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

Note that the initial power-on state of all registers, unless otherwise specified, is not defined. Therefore, it is important to enable the oscillator (CH = 0) during initial configuration.

The DS1338Z-NF runs in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12-hour or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit, with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). If the 12/24-hour mode select is changed, the hours register must be re-initialized to the new format.

On an I2C START, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

RTC and RAM Address Map

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function	Range
00H	CH	10 Seconds			Seconds				Seconds	00-59
01H	0	10 Minutes			Minutes				Minutes	00-59
02H	0	12/24	AM/PM 10 Hour	10 Hour	Hour				Hour	1-12 +AM/PM 00-23
03H	0	0	0	0	0	Day			Day	1-7
04H	0	0	10 Date		Date				Date	01-31
05H	0	0	0	10 Month	Month				Month	01-12
06H	10 Year				Year				Year	00-99
07H	OUT	0	OSF	SQWE	0	0	RS1	RS0	Control	
08H-3FH									RAM 56 x 8	00H-FFH

Note: Bits listed as "0" always read as a 0

FRTC

Control Register (07h)

The control register controls the operation of the SQW/OUT pin and provides oscillator status.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OUT	0	OSF	SQWE	0	0	RS1	RS0

Bit 7: Output Control (OUT). Controls the output level of the SQW/OUT pin when the square-wave output is disabled. If SQWE = 0, the logic level on the SQW/OUT pin is 1 if OUT = 1; it is 0 if OUT = 0.

Bit 5: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator has stopped or was stopped for some time period and can be used to judge the validity of the clock and calendar data. This bit is edge triggered, and is set to logic 1 when the internal circuitry senses the oscillator has transitioned from a normal run state to a STOP condition. The following are examples of conditions that may cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on V_{CC} and V_{BAT} are insufficient to support oscillation.
3) The CH bit is set to 1, disabling the oscillator.
4) External influences on the crystal (i.e., noise, leakage, etc).

This bit remains at logic 1 until written to logic 0. This bit can only be written to logic 0. Attempting to write OSF to logic 1 leaves the value unchanged.

Bit 4: Square-Wave Enable (SQWE). When set to logic 1, this bit enables the oscillator output to operate with either V_{CC} or V_{BAT} applied. The frequency of the square-wave output depends upon the value of the RS0 and RS1 bits.

Bits 1 and 0: Rate Select (RS1 and RS0). These bits control the frequency of the square-wave output when the square-wave output has been enabled. The table below lists the square-wave frequencies that can be selected with the RS bits.

Square-Wave Output Frequency

RS1	RS0	SQW Output Frequency
0	0	1HZ
0	1	4.096kHz
1	0	8. 192kHz
1	1	32 .768kHz

RTC

I²C Serial Data Bus

The DS1338Z-NF supports the I2 C protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data is a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device, which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1338Z-NF operates as a slave on the I2C bus. Within the bus specifications, a standard mode (100kHz cycle rate) and a fast mode (400kHz cycle rate) are defined. The DS1338Z-NF works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure: Data Transfer on I2C Serial Bus).

1) Data transfer can be initiated only when the bus is not busy.
2) During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly , the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition .

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition , the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition . The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device , when addressed, is obliged to generate an acknowledge after the reception of each byte . The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave . In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition .

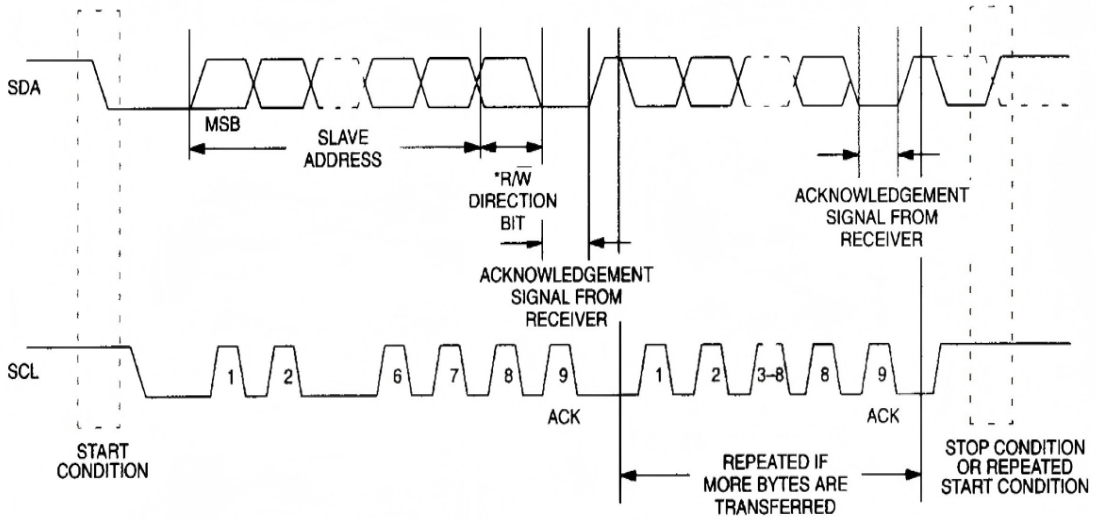


Figure 7 Data Transfer on I2C Serial Bus

Depending upon the state of the R/W bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The master transmits the first byte (the slave address). Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2) **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, which is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a "not acknowledge" is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The DS1338Z-NF can operate in the following two modes:

1) **Slave receiver mode (write mode):** Serial data and clock are received through SDA and SCL. An acknowledge bit is transmitted after each byte is received. START and STOP conditions are recognized as the beginning and end of a serial transfer. Hardware performs address recognition after reception of the slave address and direction bit (Figure: Data Write). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit DS1338Z-NF address—1101000—followed by the direction bit (R/W), which, for a write, is 0. After receiving and decoding the slave address byte, the slave outputs an acknowledge on the SDA line. After the DS1338Z-NF acknowledges the slave address and write bit, the master transmits a register address to the DS1338Z-NF. This sets the register pointer on the DS1338Z-NF, with DS1338Z-NF acknowledging the transfer. The master may then transmit zero or more bytes of data, with the DS1338Z-NF acknowledging each byte received. The register pointer increments after each data byte is transferred.
   The master generates a STOP condition to terminate the data write.
2) **Slave transmitter mode (read mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. The DS1338Z-NF transmits serial data on SDA while the serial clock is input on SCL.
   START and STOP conditions are recognized as the beginning and end of a serial transfer (Figure Data Read). The slave address byte is the first byte received after the master generates the START condition.
   The slave address byte contains the 7-bit DS1338Z-NF address—1 10 1000—followed by the direction bit (R/W), which, for a read, is 1. After receiving and decoding the slave address byte, the slave outputs an acknowledge on the SDA line. The DS1338Z-NF then starts transmitting data using the register address pointed to by the register pointer. If the register pointer is not set before the initiation of a read mode, the first address that is read is the last one stored in the register pointer. The register pointer is incremented after each byte is transferred. The DS1338Z-NF must receive a "not acknowledge" to end a read.

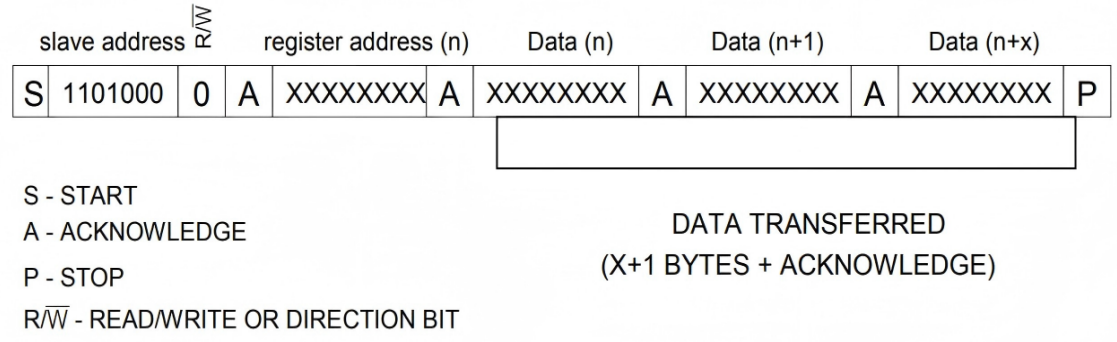


Figure: Data Write—Slave Receiver Mode

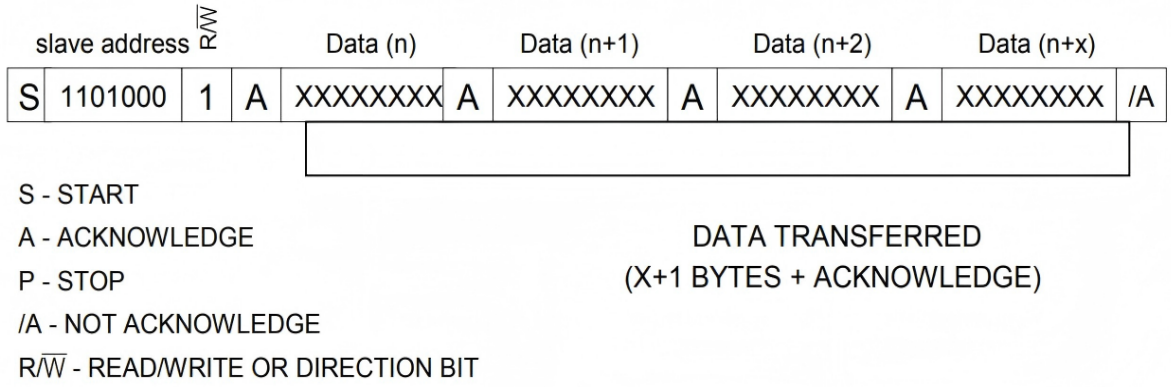


Figure: Data Read— Slave Transmitter Mode

Handling, PC Board Layout, And Assembly

The DS1338Z-NF package contains a quartz tuning-fork crystal. Pick-and-place equipment may be used, but precautions should betaken to ensure that excessive shocks are avoided.
Ultrasonic cleaning should be avoided to prevent damage to the crystal.
Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. All N.C. (no connect) pins must be connected to ground.

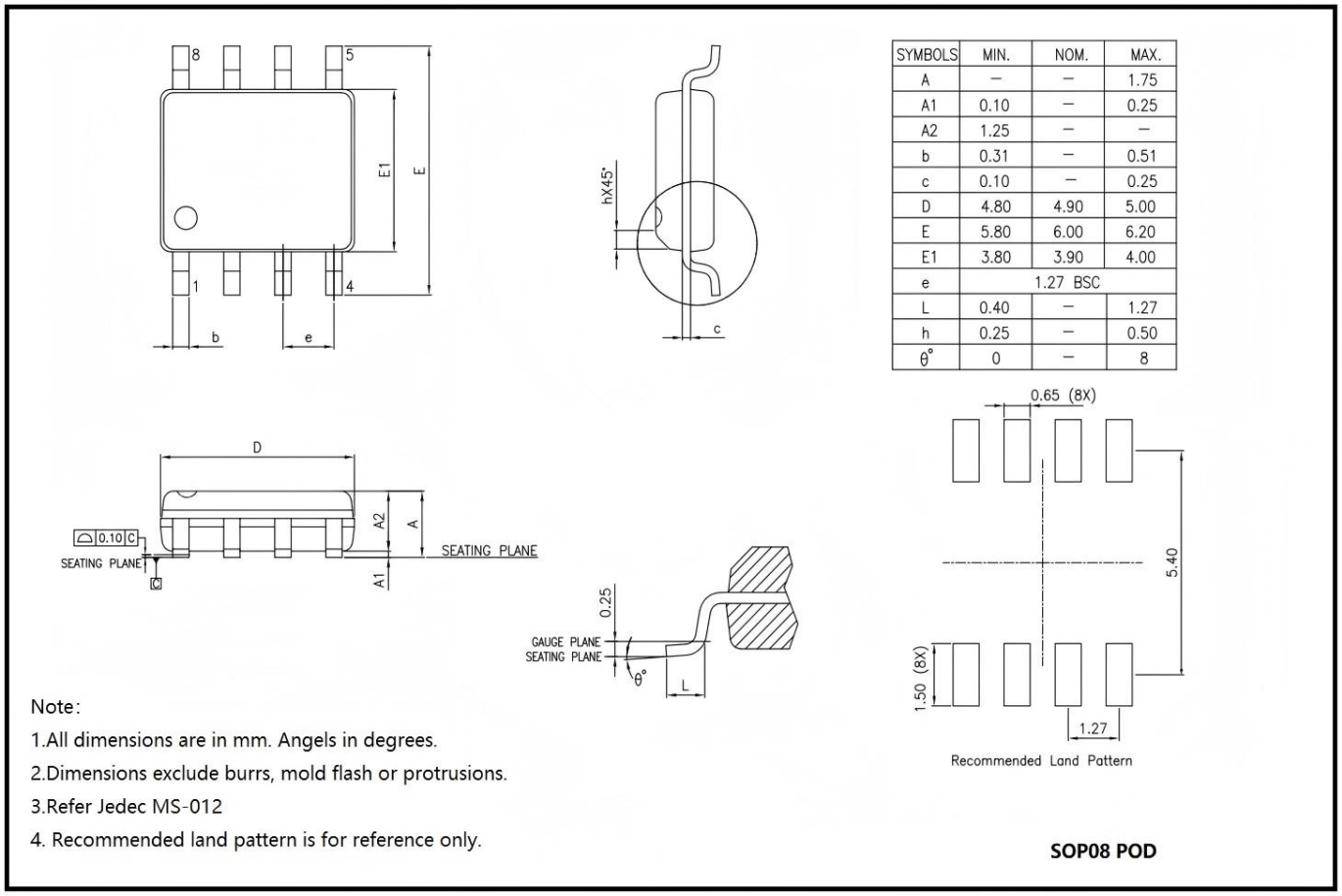
The SO package may be reflowed as long as the peak temperature does not exceed 240°C. Peak reflow temperature (≥ 230°C) duration should not exceed 10 seconds, and the total time above 200°C should not exceed 40 seconds (30 seconds nominal). Exposure to reflow is limited to 2 times maximum.

Moisture-sensitive packages are shipped from the factory dry-packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020B standard for moisture-sensitive device (MSD) classifications.

NYFEA

Package Information

DS1338Z-NF SOP-8 Package



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.75
A1	0.10	—	0.25
A2	1.25	—	—
b	0.31	—	0.51
c	0.10	—	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
L	0.40	—	1.27
h	0.25	—	0.50
θ°	0	—	8

Note:

1.All dimensions are in mm. Angels in degrees.

2.Dimensions exclude burrs, mold flash or protrusions.

3.Refer Jedec MS-012

4. Recommended land pattern is for reference only.

SOP08 POD

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Revision History

Revision	Description	Date
V1.3		2025/01/03

FRTC