3-V to 36-V Input, 6-A, Low Quiescent Current Synchronous Step-Down Regulator

Features

- AEC-Q100 Grade 1 Qualified for Automotive Applications
- Wide Input Voltage Range: 3 V to 36 V
- Supports up to 42-V Abs Max Input Voltage
- Integrated 40-mΩ High-Side, 20-mΩ Low-Side Power MOSFETs
- Low Shutdown and Quiescent Current
- 85% PFM Efficiency at 1-mA, 13.5-V VIN, 5-V Output
- 1-V ±1% Reference Voltage Accuracy
- 200-kHz to 2.2-MHz Configurable Switching Frequency
- Optional Frequency Spread Spectrum to Reduce EMI
- Symmetrical Input Path to Optimize Switch Node Ringing
- Adjustable Switch Node Slew Rate
- Output Voltage Adjustable from 1-V to 95% of Input
- Optional External Clock Synchronization
- Power-Save Mode or Forced-PWM Mode Available
- Cycle by Cycle Current Limit, Recovery from Dropout, Over Voltage, Short Circuit Protection, Thermal Shutdown
- Available in the QFN4X3.5-14 Package

Applications

- Automotive Infotainment, Cluster, USB Charge
- Advanced Driver Assistance Systems
- Battery-Powered Systems

Description

The TPP36609Q is a high-efficiency synchronous step-down regulator with integrated high-side and low-side MOSFETs. It provides up to 6-A output current with constant frequency, peak current mode control for fast loop response. The switching frequency is resistor programmable from 200 kHz to 2.2 MHz.

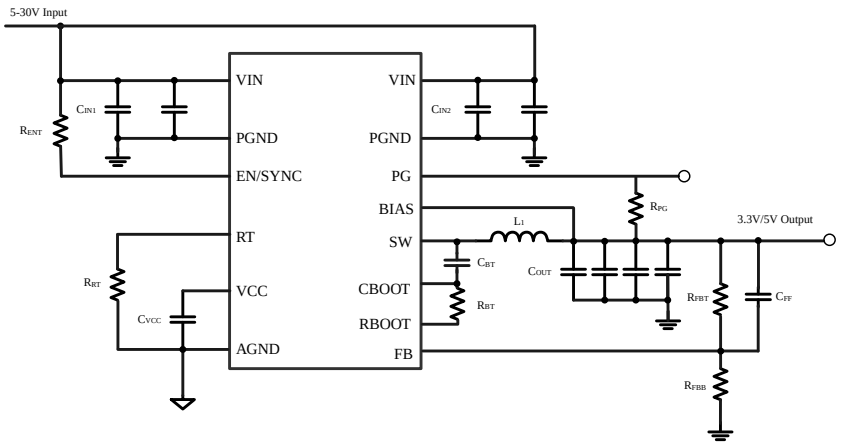
The TPP36609Q operates over a wide input voltage range from 3 V to 36 V with ultra-low quiescent current. It is ideal for automotive environments and battery-powered systems due to its extremely low quiescent current. The switching frequency automatically foldbacks to improve efficiency in the light load or standby operation. With external bias option and low integrated MOSFET resistance, the device can also ensure high efficiency in the full load range.

The TPP36609Q features 55-ns minimum on time and low drop-out mode, which can maintain stable operation for high-frequency automotive conditions. EMI performance is specially optimized in TPP36609Q. The device features a frequency spread spectrum method, adjustable switch node slew rate, optimized symmetrical pinout, and EMI friendly package to optimize the EMI emissions.

The TPP36609Q integrates soft recovery from low-dropout mode to reduce the output overshoot. The TPP36609Q has built-in robust protections such as thermal shutdown, UVLO, OVP, enable (EN) control, and power good (PG) indicator. Additionally, during the overload or short circuit condition, the accurate cycle by cycle current limit and hiccup protection are provided. Thermal shutdown provides reliable and fault-tolerant operation.

The TPP36609Q is available in the QFN4x3.5-14 package.

Typical Application Circuit



3-V to 36-V Input, 6-A, Low Quiescent Current Synchronous Step-Down Regulator

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Product Family Table

Order Number	Light Load Mode	Spread Spectrum	Output Voltage
TPP366090Q-FC3R-S	PSM Mode	Yes	Adjustable
TPP366091Q-FC3R-S	FPWM Mode	Yes	Adjustable
TPP366092Q-FC3R-S	PSM Mode	No	Adjustable

Revision History

Date	Revision	Notes
2025-06-10	Rev A.0	Initial released.
2025-09-05	Rev A.1	Added description to POD information required by packaging reference standards, and the actual product remains unchanged.
2025-10-05	Rev A.2	The following updates are about typo corrections. The actual product remains unchanged. Updated the b4 value in the POD of the QFN4X3.5-14.

Pin Configuration and Functions

TPP36609Q
QFN4X3.5-14
Top View

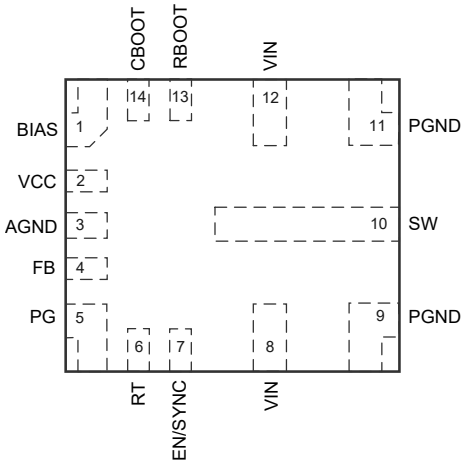


Table 1. Pin Functions: TPP36609Q

Pin No.	Name	I/O	Description
1	BIAS	P	Internal LDO input pin. Connect to the output voltage or an external supply to improve efficiency. Connect an optional ceramic capacitor from this pin to AGND to increase noise immunity. Connect to AGND if it is not used.
2	VCC	O	Internal LDO output pin. The power supply for the driver and control circuits. Connect a ceramic bypass capacitor from this pin to AGND.
3	AGND	G	Analog ground pin. The reference ground for control circuits. Connect to the power ground plane at the point of the ground of the VCC capacitor.
4	FB	I	Voltage feedback pin. Connect to the middle point of a feedback resistor divider to set the output value.
5	PG	O	Power-good indicator pin with open-drain output. Connect a pull-up resistor to the system voltage rail.
6	RT	I/O	Frequency adjustable input. Connect an external resistor from this pin to AGND to set the switching frequency. Do not float or connect to ground.
7	EN/SYNC	I	Enable and external clock input pin. The input signal to turn the regulator on or off, High = on, Low = off. This pin can also be used as clock synchronization input. This function is triggered on the rising edge of the external clock.
8, 12	VIN	P	Input voltage supply pin. Input capacitors should be placed as close to this pin and PGND pin as possible. Low impedance plane must be provided between two VIN pins.

Pin No.	Name	I/O	Description
9, 11	PGND	G	Power ground pin. The reference ground of the internal power stage. Low impedance plane must be provided between two PGND pins.
10	SW	O	Switching output pin. Connect this pin to the external inductor.
13	RBOOT	I/O	Slew rate adjustable pin. Connect this pin to CBOOT pin through a resistor range from 0 Ω to open to adjust the switch node rising time. Short to the CBOOT pin if requiring the highest slew rate.
14	CBOOT	I/O	High-side MOSFET gate supply pin. Recommend connecting a 0.1-μF ceramic capacitor between CBOOT and SW pins.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
Input	VIN to PGND	−0.3	42	V
	EN/SYNC to AGND	−0.3	42	
	FB, RT to AGND	−0.3	5.5	
	BIAS to AGND	−0.3	20	
	PG to AGND	−0.3	20	
	RBOOT, CBOOT to SW	−0.3	5.5	
	AGND to PGND	−0.3	0.3	
	AGND to PGND (less than 100 ns)	−2	2	
Output	SW to PGND	−0.3	VIN+0.3	V
	SW to PGND (less than 100 ns)	−3.5	42	
	VCC to AGND	−0.3	5.5	
T_J	Junction Temperature	−40	150	°C
T_S	Storage Temperature	−55	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	AEC-Q100-002 (1)	±2000	V
CDM	Charged Device Model ESD	AEC-Q100-011	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Recommended Operating Conditions (1)

Parameter		Min	Max	Unit
Buck Regulator	VIN	3	36	V
	VOUT (2)	1	95%*VIN	
	FB (2)	0	5	
Control	EN/SYNC	0	VIN	V
	BIAS (2)	0	15	
	PG	0	15	
Current	IOUT	0	6	A
T_A	Ambient Temperature	−40	125	°C

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, refer to the Electrical Characteristics table.
(2) Under no conditions should the output, FB, and BIAS voltage be allowed to fall below zero volts.

Thermal Information

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
QFN4X3.5-14	52.3	13.3	24.8	°C/W

Electrical Characteristics

Unless otherwise noted, the min and max limits apply over the recommended operating ambient temperature range (T_A) of −40°C to 125°C. Typical values are measured under T_A = 25°C and represent the most likely parameters normally for reference. The default test conditions: V_{IN} = 13.5 V, V_{OUT} is the output voltage.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power Supply						
V_{IN}	Operation Input Voltage		3		36	V
I_{SD}	Shutdown Supply Current, Measured at VIN Pin	V_{EN} = 0 V		0.5		μA
I_{Q_PSM}	Operating Regulation Current (Non-Switching) (1)	V_{FB} = 1.2 V, V_{BIAS} = 5 V, PSM Mode		8.3		μA
I_{Q_VIN}	Operating Quiescent Current at VIN Pin (Non-Switching)	V_{FB} = 1.2 V, V_{BIAS} = 5 V		0.9		μA
I_{Q_BIAS}	Operating Quiescent Current at BIAS Pin (Non-Switching)	V_{FB} = 1.2 V, V_{BIAS} = 5 V, PSM Mode		20		μA
Enable						
V_{EN_H}	Enable Rising Threshold		1.21	1.26	1.31	V
V_{EN_HYS}	Enable Hysteresis Threshold as Percentage of Typical EN Voltage			25		%
V_{EN_SYNC}	Edge Necessary for SYNC Function	Rise/Fall Time < 30 ns			2.5	V
t_{SYNC_MIN}	Min SYNC Edge on and off Time		100			ns
I_{EN}	Enable Pin Input Current	V_{EN} = V_{IN}		2		nA
Soft Start						
T_{SS}	Time from First SW Pulse to V_{REF} Reach 90%			5	7.5	ms
T_{SS2}	Time from First SW Pulse to Release FPWM Lockout if Output is not in Regulation			13.5	20	ms
Voltage Reference						
V_{FB}	Feedback Voltage	FPWM Mode	0.99	1	1.01	V
I_{FB}	Current into FB Pin	V_{FB} = 1 V		10		nA
VCC Regulator						
VCC	Internal LDO Output	V_{BIAS} > 3.4 V, CCM Mode		3.3		V
		V_{BIAS} = 3.2 V, Non-Switching		3.2		V
VCC_{UVLO_R}	Internal LDO Output UVLO Rising Threshold			3		V
VCC_{UVLO_HYST}	Internal LDO Output UVLO Hysteresis Threshold			0.4		V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BIAS_ON_R}$	Internal BIAS Operating Rising Threshold			3.1		V
MOSFETs						
R_{DSON_H}	High Side MOSFET on Resistance			40		mΩ
R_{DSON_L}	Low Side MOSFET on Resistance			20		mΩ
Current Limits						
I_{LIMIT_H}	High Side MOSFET Current Limit (2)	Duty Cycle Approaches 0%	8.5	10	12.1	A
I_{LIMIT_L}	Low Side MOSFET Current Limit		6.1	7.5	9.1	A
I_{LIMIT_NEG}	Negative Current Limit in FPWM Mode			-3		A
I_{PK_MIN}	Minimum Peak Inductor Current in PSM Mode			0.9		A
Power Good						
V_{PG_HR}	Power Good High Threshold	Rising Threshold, % of V_{FB}	104	107	110	%
V_{PG_LF}	Power Good Low Threshold	Falling Threshold, % of V_{FB}	91	94	97	%
V_{PG_HYST}	Power Good Threshold Hysteresis	% of V_{FB}		1		%
R_{PG}	PG Pull-Down Resistance	V_{EN} = 3.3 V, 1 mA Pull up to PG Pin		25	50	Ω
t_{PG_R}	Power Good High Delay			2		ms
t_{PG_F}	PG Glitch Filter Delay			120		μs
V_{IN_PG}	Minimum Input Voltage for PG Function				2.7	V
V_{PG}	PG Logic Low Output	V_{EN} = 0 V, 1 mA Pullup to PG Pin			0.05	V
BOOT Supply						
$V_{BOOT\text{-}UV}$	Bootstrap Voltage Undervoltage Threshold			2.1		V
Hiccup Mode						
V_{HC}	FB Voltage to Trip Hiccup Mode			0.4		V
t_{HC}	Interval Time between Hiccup Burst			80		ms
Oscillator						
f_{SW_200k}	Switching Frequency	RT = 66.5 kΩ	175	200	225	kHz
f_{SW_400k}	Switching Frequency	RT = 33.2 kΩ	355	400	445	kHz
$f_{SW_2.2M}$	Switching Frequency	RT = 5.76 kΩ	1.98	2.2	2.42	MHz
f_{SS}	Spread Spectrum Frequency Deviation from Center Frequency			8		%
T_{ON_MIN}	Minimum On Time			55		ns
T_{OFF_MIN}	Minimum Off Time			120		ns
T_{ON_MAX}	Maximum On Time			8		μs
Thermal						
T_{SD}	Thermal Shutdown			170		°C

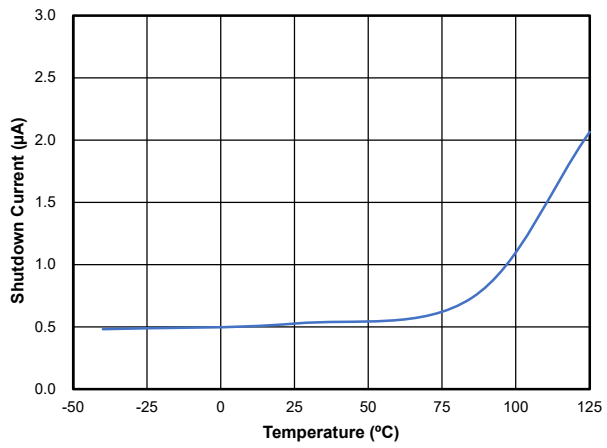
Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{SD_HYS}	Thermal Shutdown Hysteresis			20		°C

(1) Guaranteed by design. $I_{Q_PSM} = I_{Q_VIN} + I_{Q_BIAS} * (V_{OUT} / V_{IN})$

(2) High-side MOSFET current limit is affected by the duty cycle. The high-side current limit is higher at a small duty cycle.

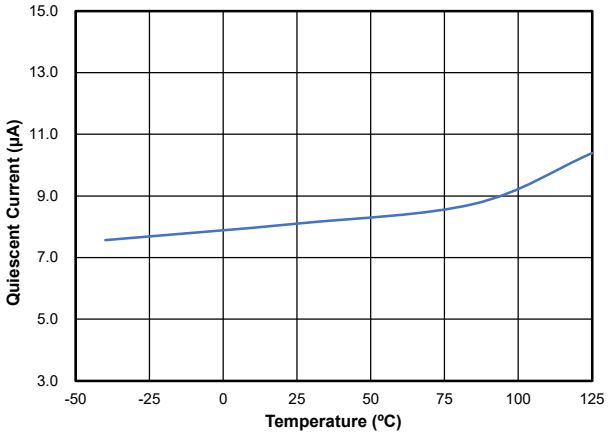
Typical Performance Characteristics

All test conditions: V_{IN} = 13.5 V, F_{SW} = 400 kHz, T_A = 25 °C, unless otherwise noted.



V_{EN} = 0 V

Figure 1. Shutdown Supply Current



V_{FB} = 1.2 V

Figure 2. Quiescent Current

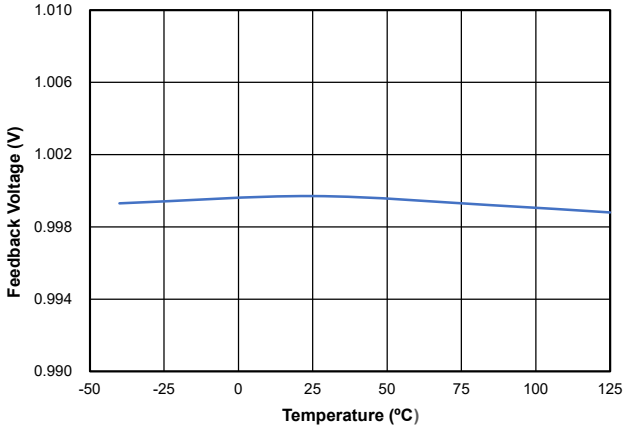


Figure 3. Feedback Voltage

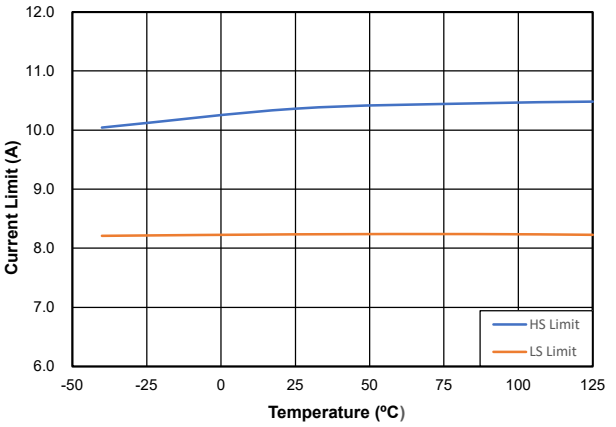


Figure 4. High-Side and Low-Side Current Limits

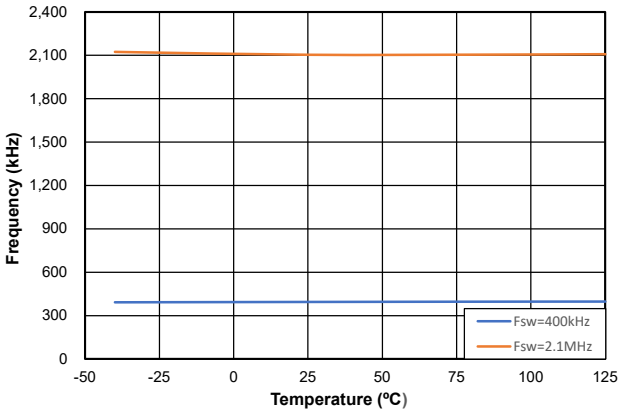


Figure 5. Switching Frequency

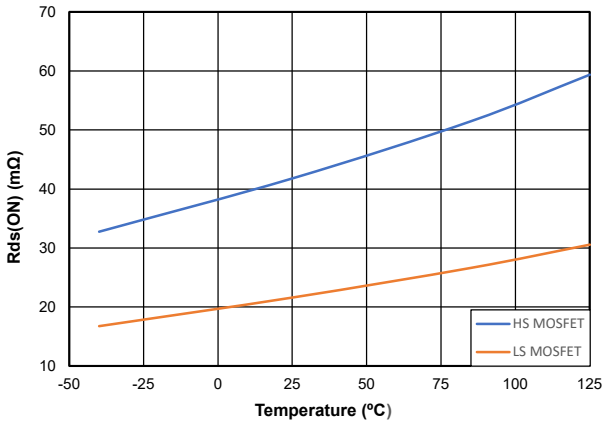


Figure 6. High-side and Low-side MOSFET

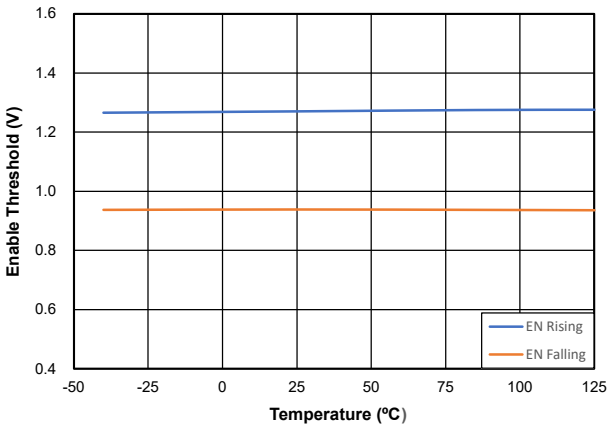


Figure 7. Enable Thresholds

Detailed Description

Overview

The TPP36609Q is a high-efficiency synchronous step-down regulator with integrated high-side and low-side MOSFETs. It provides up to 6-A output current with high efficiency from light-load to full-load operating range. The TPP36609Q operates with constant frequency, peak current mode control for fast loop response. The switching frequency is resistor programmable from 200 kHz to 2.2 MHz.

The TPP36609Q operates over a wide input voltage range from 3 V to 36 V with ultra-low quiescent current. It is ideal for automotive environments and battery-powered systems due to its ultra-low quiescent current. The switching frequency automatically foldbacks to improve efficiency in the light load or standby operation. With the external bias option and low integrated MOSFET resistance, the device can also ensure high efficiency in the full load range. The internal-soft start limits inrush current during power on. The TPP36609Q also integrates a compensation circuit inside the chip to simplify the loop design.

The TPP36609Q features 55 ns minimum on time and low drop-out mode, which can maintain stable operation for high-frequency automotive conditions. EMI performance is specially optimized in the TPP36609Q. The device features frequency a spread spectrum method, adjustable switch node slew rate, optimized symmetrical pinout, and EMI friendly package to optimize the EMI emissions.

The TPP36609Q integrates soft recovery from low dropout-mode to reduce the output overshoot. The TPP36609Q has built-in robust protections such as thermal shutdown, UVLO, OVP, enable (EN) control, and power good (PG) indicator. Additionally, during the overload or short circuit condition, the accurate cycle-by-cycle current limit and hiccup protection are provided. Thermal shutdown provides reliable and fault-tolerant operation.

Functional Block Diagram

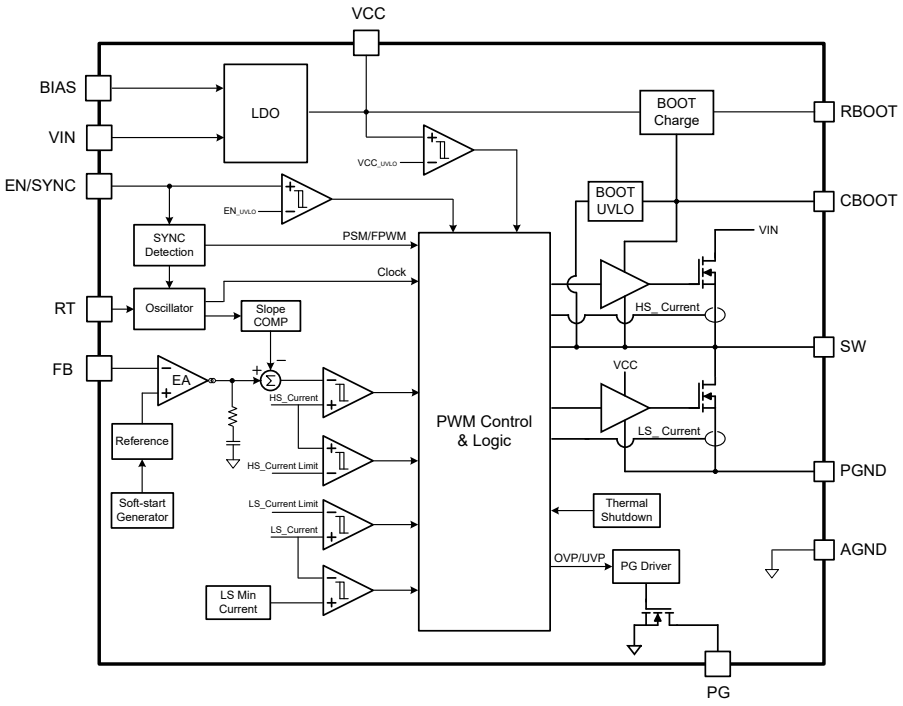


Figure 8. Functional Block Diagram

Feature Description

Fixed Frequency Peak Current Mode Control

The TPP36609Q adopts fixed frequency peak current mode control. The feedback voltage is sensed from the resistor divider through the FB pin to compare with the internal voltage reference by an error amplifier. By adjusting the value of the peak current with different output voltage deviations, this voltage control loop is designed to obtain accurate DC voltage regulation. The output of the error amplifier is compared with the sensed peak current by the PWM comparator and controls the on time of the high-side power switch. The device also integrates the compensation of the voltage feedback loop to save external components and ensure the stability of the control loop in various working conditions.

An internal oscillator controls the switching frequency and initiates the turn-on of the integrated high-side power switch in each duty cycle. During this high side on period, SW voltage rises to approximately input voltage, and the inductor current increases linearly. Once the sensed current through the high-side switch reaches the threshold level set by COMP voltage of the error amplifier, the PWM comparator turns off the high-side switch. The low-side power switch is turned on after a short dead time and the inductor current is discharged linearly by the low-side power switch. The device also utilizes an internal ramp compensation control to avoid sub-harmonic oscillations when duty cycle is larger than 50%. The COMP voltage is also clamped for current limit conditions and light load operation.

EN/SYNC Function for Synchronization

The TPP36609Q integrates an accurate enable threshold. When the EN/SYNC voltage rises above the threshold, the device is turned on. The EN/SYNC pin cannot be left floating. The simplest way to enable the device is to connect this pin to the input voltage. However, the accurate threshold can provide an accurate input undervoltage lockout (UVLO) operation. This can be used for sequencing, preventing the re-triggering of the device. In this application, the UVLO threshold is adjusted by using the EN/SYNC pin with an external resistor divider.

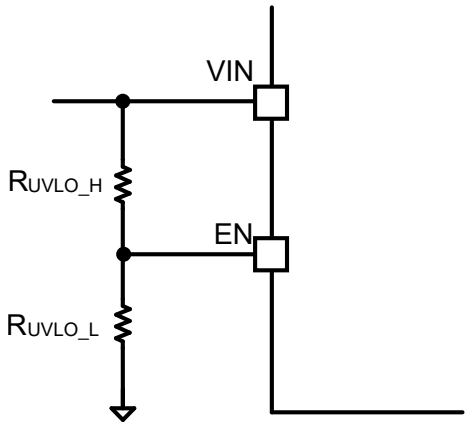


Figure 9. UVLO Adjustment

The resistor values can be calculated below.

$$R_{UVLO_L} = R_{UVLO_H} * \frac{V_{EN}}{V_{ON} - V_{EN}} \quad (1)$$

where V_{ON} is the desired start-up UVLO voltage.

The EN/SYNC pin can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by AC coupling a positive clock into the EN/SYNC pin. The AC-coupled clock edge into the EN/SYNC pin must exceed the SYNC amplitude threshold, while the minimum SYNC rising and falling pulse period must be longer than the minimum edge required.

Adjustable Switching Frequency

The frequency of the device is programmable through a resistor connected between the RT pin and AGND. The switching frequency affects solution size, efficiency, and duty cycle. It is suggested that all factors be taken care of when selecting the switching frequency. The resistor can be calculated through the following equation.

$$F_{SW}(kHz) = \frac{12073}{\left(\frac{R_{RT}(k\Omega)}{1000}\right)^{0.948}} \quad (2)$$

Internal LDO, BIAS Input

VCC is the power supply for the integrated driver and control circuits. It is the output of the internal LDO which typical value is 3.3V. The input of the internal LDO is the BIAS pin, which can be supplied from the output voltage or another external power supply to further improve the operating efficiency and reduce the quiescent current of the system. If the BIAS voltage is below 3.1V, the input voltage takes over and supply the internal LDO.

Soft-Start with Pre-Biased Capability

The TPP36609Q implements a soft-start circuit to prevent the inrush current during start up. The soft-start time is fixed internally. When the start-up period begins, the internal reference voltage slowly ramps up.

The TPP36609Q also supports a monotonic start-up with pre-biased loads. If the output voltage is pre-biased to a certain value during start-up, the device disables switching for both high-side and low-side power switches until the soft-start reference voltage exceeds the feedback voltage.

Frequency Spread Spectrum (Dual Triangle Spread Spectrum)

The TPP36609Q provides a digital spread spectrum that reduces the EMI of the power supply over a wide frequency range. The internal modulator dithers the internal clock. When an external synchronization clock is applied to the EN/SYNC pin, the internal spread spectrum is disabled. The dual triangle spread spectrum combines a low-frequency triangular modulation profile with a high-frequency triangular modulation profile. The low-frequency triangular modulation improves performance in lower radio frequency bands (for example, AM band), while the high-frequency triangular modulation improves performance in higher radio frequency bands (for example, FM band). In addition, the frequency of the triangular modulation is further modulated to reduce the likelihood of any audible tones. To minimize output voltage ripple caused by the spread spectrum, the duty cycle is modified on a cycle-by-cycle basis to maintain a nearly constant duty cycle when dithering is enabled.

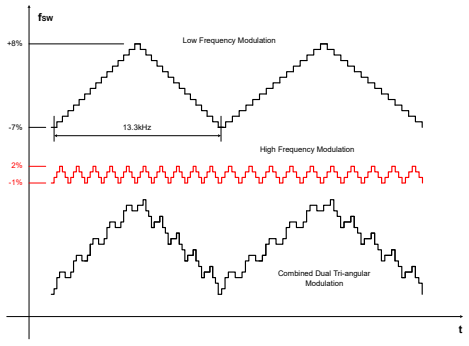


Figure 10. Dual Triangle Spread Spectrum

Bootstrap and Adjustable Slew Rate

The internal driver for the high-side switch utilizes a bootstrap supply to boost the voltage higher than the input. An external capacitor should be connected between CBOOT and SW pins while the bootstrap diode is integrated in TPP36609Q to minimize the external component. The voltage on the CBOOT pin is charged from VCC through this internal switch when the low- side switch is turned on. It is recommended that a 100-nF capacitor rated for 10 V or higher is used.

To allow optimization of EMI with respect to efficiency, one resistor can be connected between RBOOT and CBOOT pins by adjusting the rising time of the device. When the RBOOT pin is shorted to the CBOOT pin, the rising time is very fast. Note that switching with a slower slew rate also decreases efficiency.

Low Drop-out Mode and Recovery from Dropout

As the duty cycle increases, where the input voltage approaches the output voltage level, the required off time of high-side power switch approaches its minimum off time. When the minimum off time is reached, the TPP36609Q automatically extends the high side on time and reduces the switching frequency. The device can realize 95% max duty cycle in drop-out condition. In this condition, the dropout voltage difference between input and output is influenced by the on-resistance of the power switch, the DCR of the power inductor, and the maximum duty cycle achieved. For different load currents, the 5-V output drop-out voltage is shown below

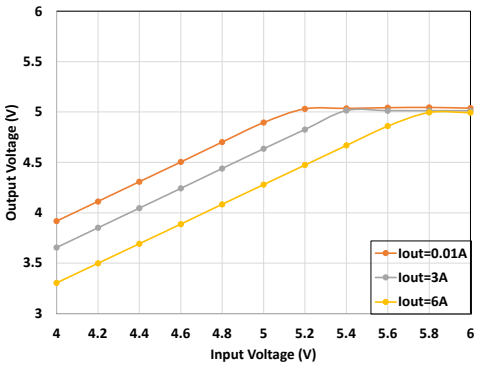


Figure 11. Low Drop-out Voltage

In low drop-out mode, the output voltage falls according to the input voltage decrease. When the output voltage falls more than a certain percentage, the output voltage ramps up slowly. This condition is important because when the device recovers from the dropout mode, the output voltage clamps at the same speed as during the start-up period. This function can help reduce the overshot on the output.

Minimum on Time

As the duty cycle is decreasing, where the conversion ratio is very low, the required on-time of the high-side power switch approaches its minimum on time. The TPP36609Q features a typical 55-ns ultra-low minimum on time and can support smaller duty cycles for high-frequency power systems. Also, the device can automatically reduce the switching frequency, when the minimum on time is reached.

Power Good

The device employs an open-drain output PG signal to check whether the output voltage is operating within the normal range. The external pull-up voltage resource is recommended to be less than 5.5V (such as VCC) with a 1-kΩ resistor. Once the feedback voltage is within 95% and 107% of the internal reference voltage, the PG pull-down is disabled and pulled up by the external resistor. Once the feedback voltage is lower than 94% or greater than 106% of the internal reference voltage, the PG is pulled low.

Light Load Operation

The TPP36609Q integrates two behaviors in light-load operation. One behavior is power-saved mode (PSM) to improve efficiency in light-load working conditions. When the loading current decreases, the device approaches discontinuous conduction mode first, and the COMP voltage decreases accordingly. The low-side power switch is turned off when the zero current detection is triggered to improve system efficiency. When the COMP voltage drops to the low clamped threshold voltage, the device skips pulses and decreases the switching frequency by extending the non-switching period. During this period, the output voltage decreases due to load current or capacitor discharge. The high-side power switch resumes to

turn on once the COMP voltage is higher than the threshold. The device tries to obtain a few switching pulses with a minimum peak inductor current to reduce the output ripple, and the COMP voltage drops to the clamped value again and triggers another non-switching period. During the non-switching period, most internal circuits are shut down, except for some protection blocks, to reduce the power consumption.

The other behavior is forced-PWM mode (FPWM) to optimize the output ripple. In FPWM mode, the device operates in continuous conduction mode during light load operation, and the switching frequency is almost constant over the entire load range. To maintain the switching frequency, a limited negative current is allowed to flow through the inductor and low-side power switch. Note that all the devices operate in FPWM mode when synchronizing frequency to an external signal.

Protection

Current Limits

The TPP36609Q employs both cycle-by-cycle peak and valley current limits to protect the high-side and low-side power switch from overload. Once the inductor current reaches the high-side peak current limit, the high-side switch is turned off immediately to avoid the inductor current from further increasing. When the low-side valley current limit is triggered, the next duty cycle is held until the inductor current recovers within the valley current limit. Both peak and valley current limits determine the maximum output current of the device, and the valley current limit can prevent the inductor current from running away during unexpected overload or short circuit conditions. Also, the device integrates a zero-current detector to turn off the low-side power switch at light loads. Delay needs to be taken into account which may cause the sensed current slightly different from open-loop current limits.

Short Circuit Protection

To further ensure the protection of the converter during prolonged overload or short circuits, the device features a hiccup overload protection. When the inductor peak current is clamped at the peak current limit, the output voltage falls out of normal regulation. Furthermore, if the feedback-sensed voltage drops below 0.4V, the device enters the hiccup mode. Entering this mode, the device stops switching and waits for about 80ms to restart a normal soft start operation. If the overload condition still exists, the device keeps switching with the peak current limit and turns off the switches again. The device can automatically recover to normal operation when the overload condition is removed. The hiccup function is disabled at the normal soft start period to avoid being mistakenly triggered.

Over Voltage Protection

The TPP36609Q integrates the over-voltage protection to optimize the output voltage overshoot during load transients and help recover from the output fault conditions. The internal detection circuit compares the feedback voltage to the internal reference. When the feedback voltage exceeds the threshold voltage, the internal power switch and switching clock are turned off to avoid the output voltage from further increase.

Thermal Shutdown

Once the junction temperature rises above the internal over-temperature shutdown threshold, the internal temperature sensor shuts down the device. The device recovers operating when the junction temperature falls below the threshold with hysteresis.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPP36609Q is typically used to convert a wide range of input voltage to the desired output voltage, which can be set by the feedback resistor divider. Because of the ultra-low minimum on time and high efficiency, the TPP36609Q is also suitable for 2.1-MHz high-frequency applications to increase system power density. The device is integrated with the internal compensation and can operate over a wide range of external components and working conditions. However, some typical parameters and external component values are recommended to help speed up the develop process. In most power systems, lower voltage rails such as 5 V/3.3 V is typically used for microcontrollers, I/Os, and other low-voltage components.

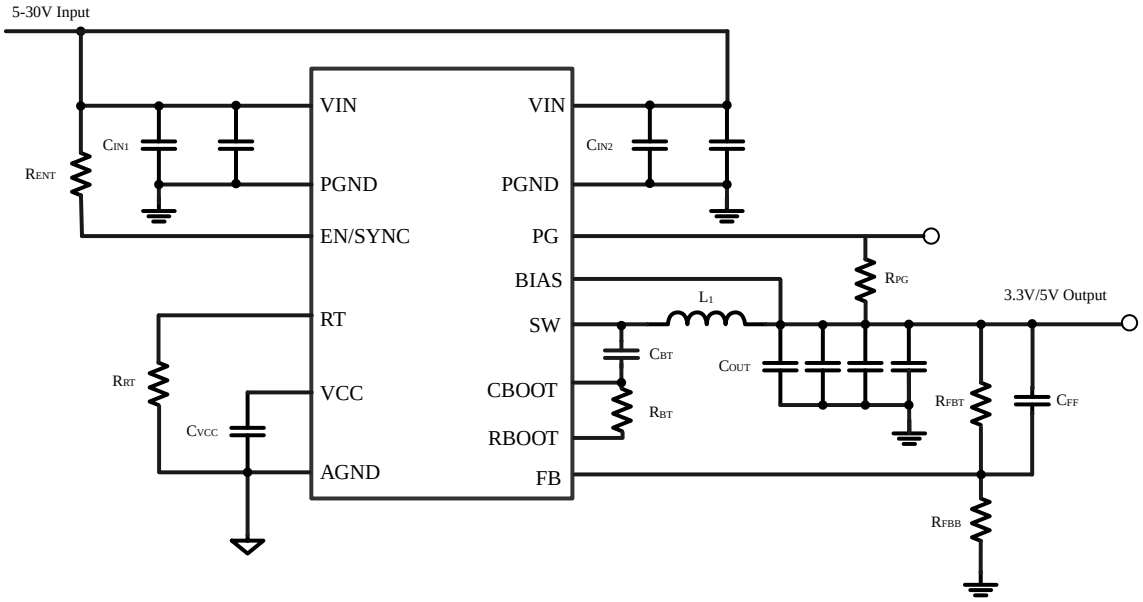


Figure 12. Typical Application Circuit

Choosing Switching Frequency

Switching frequency of the DCDC regulator is a compromise between system efficiency and total solution size. The lower switching frequency can help reduce power losses and usually results in higher system efficiency, while the higher switching frequency allows the selection of smaller external components, such as inductors and output capacitors, and increases the system power density. The TPP36609Q is suitable for high-frequency applications because it is designed with high efficiency and a small minimum on time.

Setting Output Voltage

The external resistor divider network connected to the FB pin sets the output voltage. The resistance of the divider is a compromise between noise suppression and output current consumption. The smaller value resistor reduces noise sensitivity but also increases the quiescent current of the system and reduces light load efficiency. It is typically recommended to select 100 kΩ resistor for the top feedback resistor. If low quiescent current and high light load efficiency are required, a 1-MΩ

top feedback resistor can be selected and one feedback capacitor can be used to improve the phase margin. Once the top feedback resistor is selected, the value of the bottom feedback resistor can be calculated with the equation below.

$$R_{FBB} = \frac{V_{FB} * R_{FBT}}{V_{OUT} - V_{FB}} \quad (3)$$

where V_{FB} is the internal reference voltage, which is typically 1 V for TPP36609Q. For a 5 V output, if R_{FBT} = 100 kΩ, R_{FBB} = 24.9 kΩ is chosen. If R_{FBT} = 1 MΩ, R_{FBB} = 249 kΩ is chosen.

Inductor Selection

The selection of the inductor affects steady-state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications: inductor value, DC resistance, and saturation current. The inductor value is designed based on the desired peak-to-peak ripple current and is typically chosen to be in the range of 20% to 40% of the maximum output current. Once the desired inductor ripple current is selected, the inductor value can be calculated with the equation below.

$$L = \frac{V_{OUT}}{f_{SW} * \Delta I_L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

where f_{SW} is the switching frequency and ΔI_L is the inductor ripple current.

When the inductor current approaches its saturation level, the effective inductance can fall to a fraction of the zero current value. Although one high-side valley current limit is integrated to avoid the current runaway, the inductor current can rise to a high value very rapidly if the inductor is saturated. The inductor saturation current must leave a safe margin from the high-side peak current limit in the worst-case conditions. The RMS current and peak current of the inductor can be calculated with the equation below.

$$I_{L_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (5)$$

$$I_{L_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L}{12}} \quad (6)$$

Input Capacitor Selection

The input capacitor of the step-down regulator is used to supply the AC input current and maintain a stable DC input voltage. At least a 10-μF capacitance of ceramic input capacitor is recommended. Additional input capacitance may be required to meet ripple and transient requirements. High-quality ceramic capacitor, X5R or X7R, is recommended because of low equivalent series resistance (ESR) characteristics and small capacitance variations over a temperature range. In addition, one small value and small case size, ceramic capacitor (such as 100-nF, 0603 package) is recommended to be used at the input and be placed as close as possible to the VIN and GND pins. This can provide a high-frequency bypass for the internal control circuits. The input capacitor can be calculated with the equation below when the input voltage ripple is determined.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

where C_{IN} is the input capacitance value.

The input capacitor ripple current rating should be greater than the maximum input current ripple. The RMS current of the input capacitor can be calculated with the equation below.

$$I_{CIN_RMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (8)$$

The worst case for the input voltage ripple and RMS current occurs when the duty cycle is 50%.

Output Capacitor Selection

The output capacitance is mainly selected to meet the requirement of the output ripple and voltage change during a load transient. Then the control loop is compensated for the output capacitor selected. The output voltage ripple is related to the capacitance and ESR of the output capacitor. Assuming the capacitor has small ESR, the minimum output capacitance needed for a given output ripple voltage can be calculated with the equation below.

$$C_{OUT} > \frac{\Delta I_L}{8 * f_{SW} * \Delta V_{OUT}} \quad (9)$$

where ΔI_L is the inductor ripple current and ΔV_{OUT} is the output voltage ripple.

If a large ESR capacitor is used, it contributes additional output ripple. ESR ripples can be neglected for ceramic capacitors, but must be considered if electrolytic capacitors are used. The maximum ESR for a given ripple can be calculated with the equation below.

$$R_{ESR} < \frac{\Delta V_{OUT}}{\Delta I_L} - \frac{1}{8 * f_{SW} * C_{OUT}} \quad (10)$$

The effective value of the ceramic capacitor decrease should be considered when the output DC bias voltage is added across the capacitors. The RMS current of the output capacitor can be calculated with the equation below.

$$I_{COUT_RMS} = \frac{V_{OUT} * (V_{IN_MAX} - V_{OUT})}{\sqrt{12} * V_{IN_MAX} * L * f_{SW}} \quad (11)$$

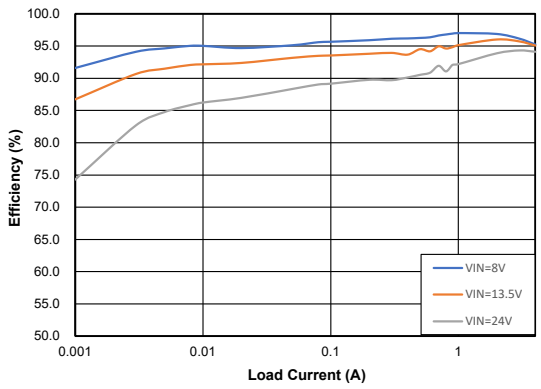
where V_{IN_MAX} is the maximum input voltage, and L is the selected inductor value.

Bootstrap Capacitor Selection

A typical 0.1-μF bootstrap capacitor is connected between the BOOT pin and the SW pin. It is recommended to use a ceramic capacitor with X5R or superior grade dielectric and a voltage rating of 10 V or higher.

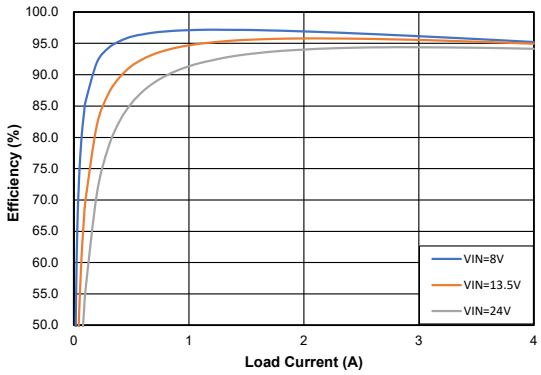
Application Waveforms

All test conditions: V_{IN} = 13.5 V, F_{SW} = 400 kHz, V_{OUT} = 5 V, T_A = 25 °C, unless otherwise noted.



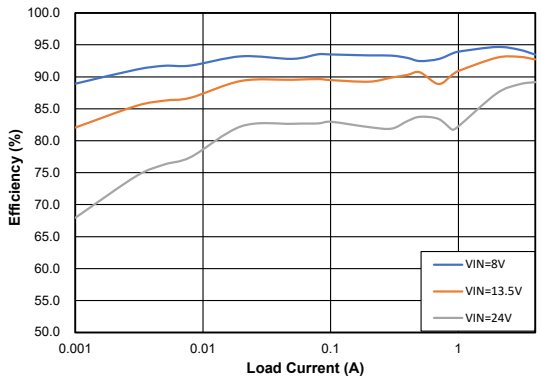
F_{SW} = 400 kHz, PFM Mode

Figure 13. Efficiency



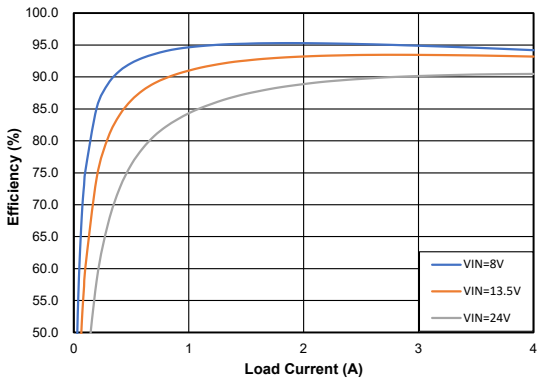
F_{SW} = 400 kHz, FPWM Mode

Figure 14. Efficiency



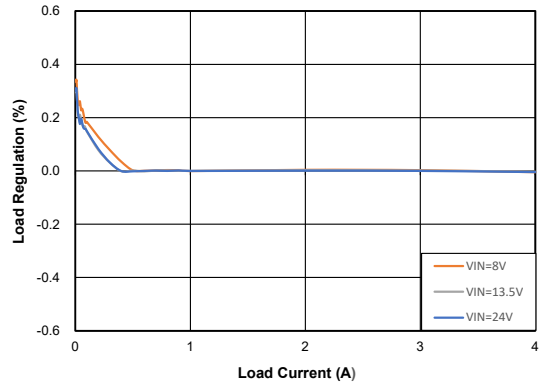
F_{SW} = 2.1 MHz, PFM Mode

Figure 15. Efficiency



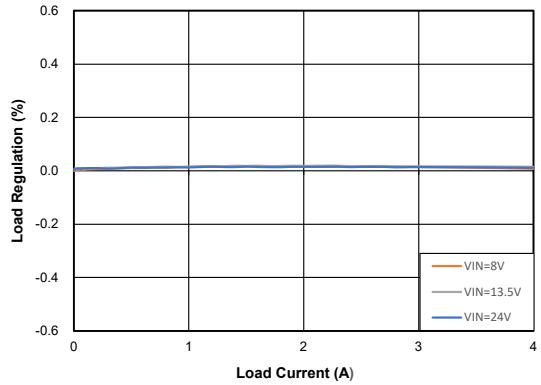
F_{SW} = 2.1 MHz, FPWM Mode

Figure 16. Efficiency



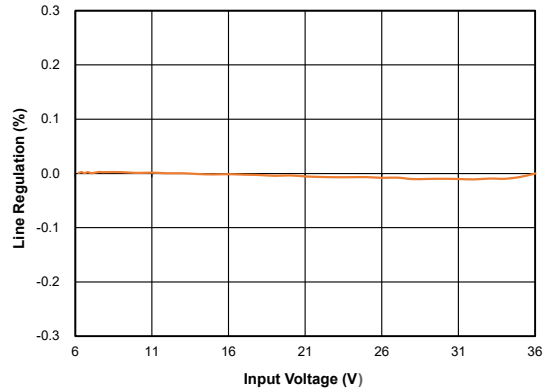
PFM Mode, I_{OUT} = 3 A

Figure 17. Load Regulation



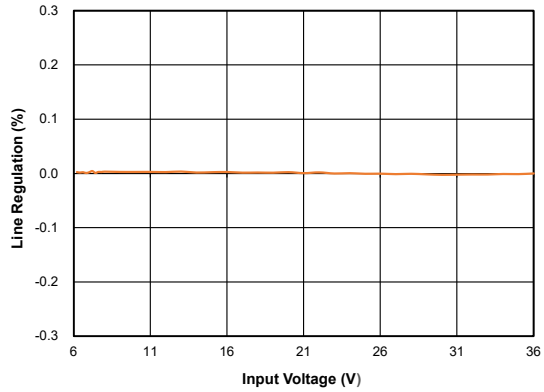
FPWM Mode, I_{OUT} = 3 A

Figure 18. Load Regulation



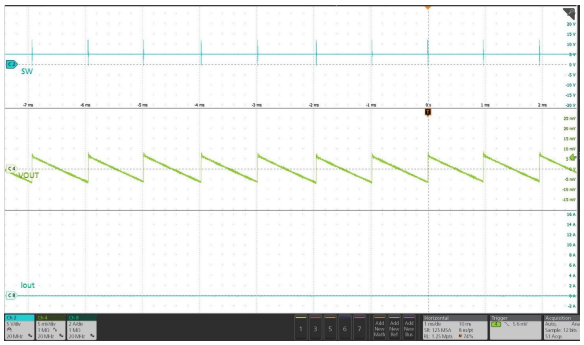
PFM Mode

Figure 19. Line Regulation



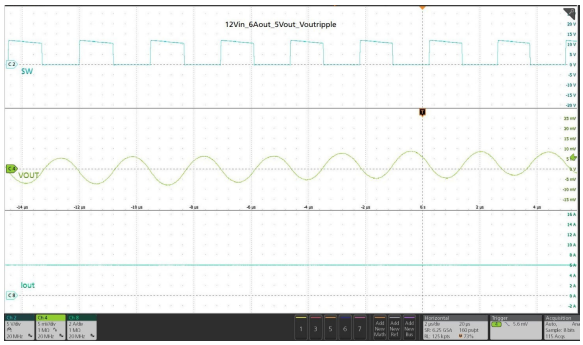
FPWM Mode

Figure 20. Line Regulation



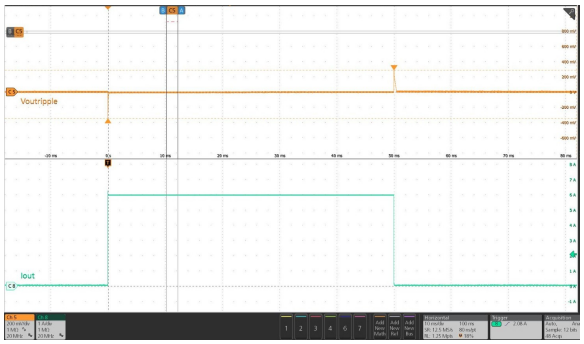
I_{OUT} = 10 mA, PFM Mode

Figure 21. Switching Waveform and Output Ripple



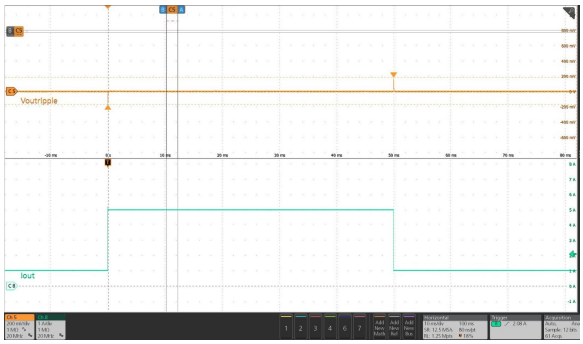
I_{OUT} = 6 A, PFM Mode

Figure 22. Switching Waveform and Output Ripple



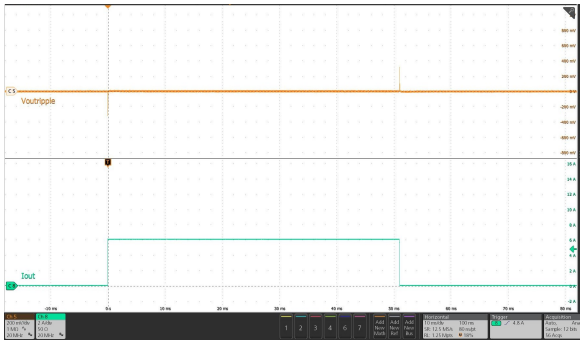
I_{OUT} = 0 A to 6 A to 0 A, PFM Mode

Figure 23. Load Transient



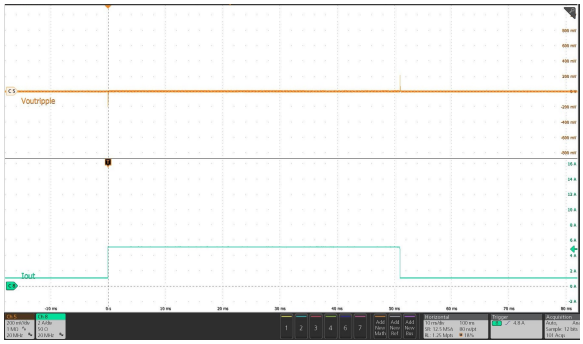
I_{OUT} = 1 A to 5 A to 1 A, PFM Mode

Figure 24. Load Transient



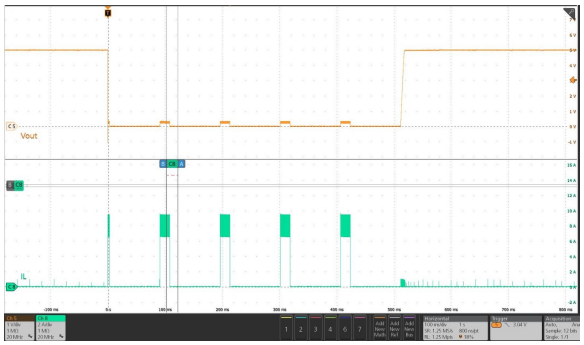
I_{OUT} = 0 A to 6 A to 0 A, FPWM Mode

Figure 25. Load Transient



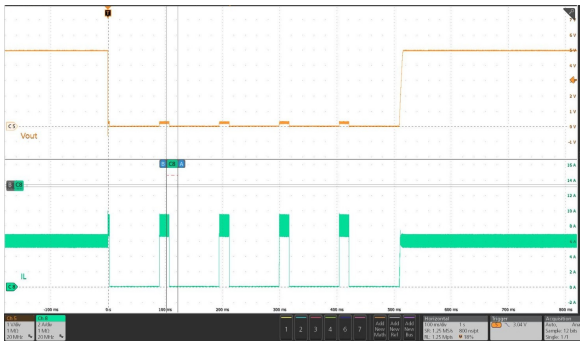
I_{OUT} = 1 A to 5 A to 1 A, FPWM Mode

Figure 26. Load Transient



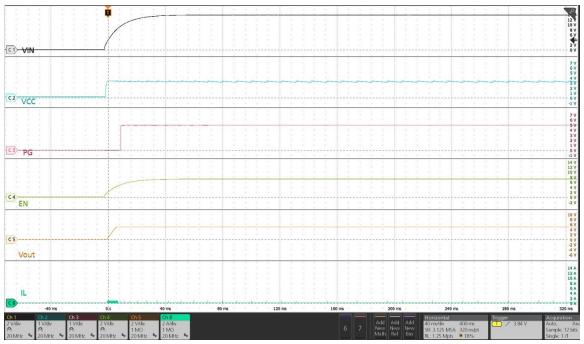
I_{OUT} = 0 A, PFM Mode

Figure 27. Short Circuit Protection



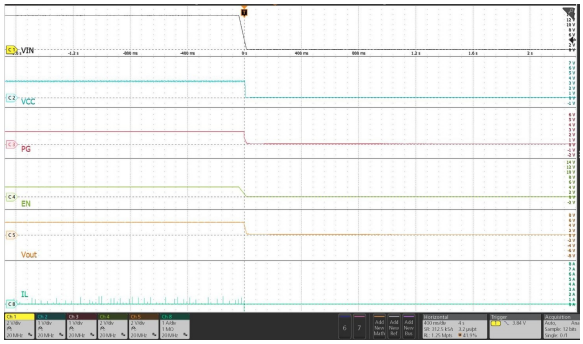
I_{OUT} = 6 A, PFM Mode

Figure 28. Short Circuit Protection



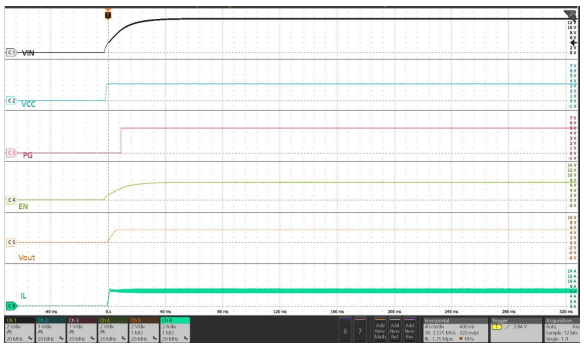
I_{OUT} = 0 A, PFM Mode

Figure 29. Power up by Inputs



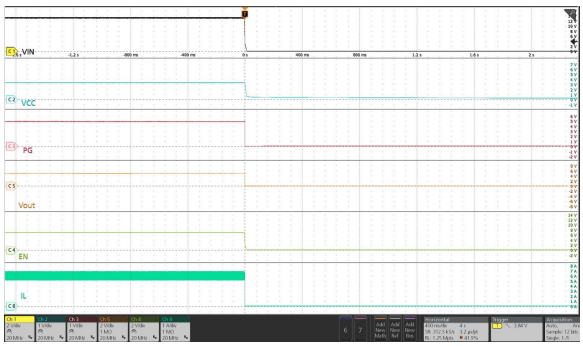
I_{OUT} = 0 A, PFM Mode

Figure 30. Power down by Inputs



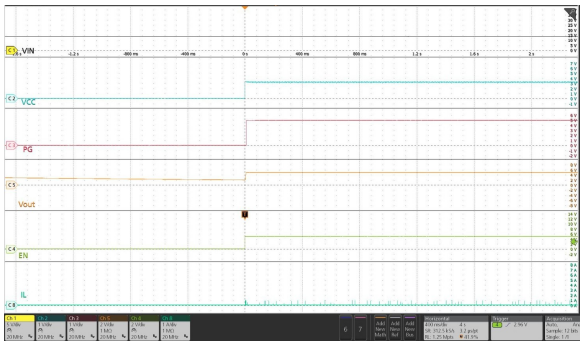
I_{OUT} = 6 A, PFM Mode

Figure 31. Power up by Inputs



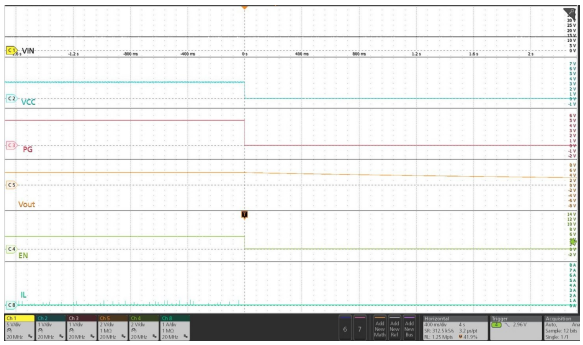
I_{OUT} = 6 A, PFM Mode

Figure 32. Power down by Inputs



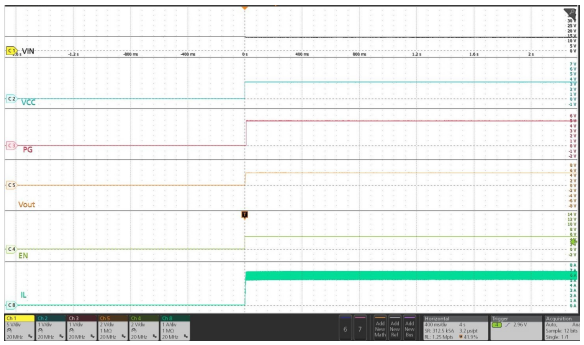
I_{OUT} = 0 A, PFM Mode

Figure 33. Power up by Enable



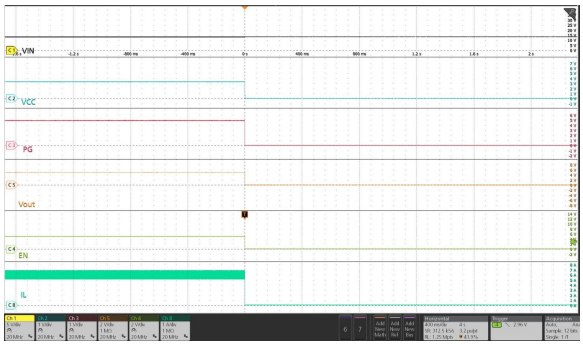
I_{OUT} = 0 A, PFM Mode

Figure 34. Power down by Enable



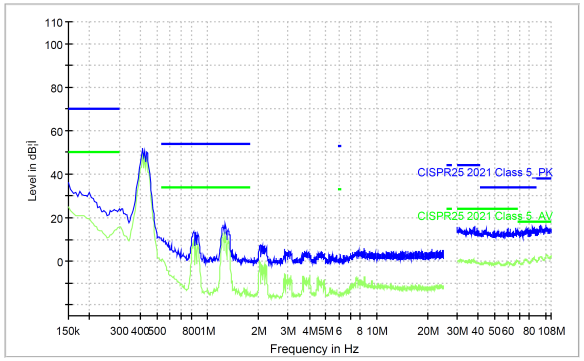
I_{OUT} = 6 A, PFM Mode

Figure 35. Power up by Enable



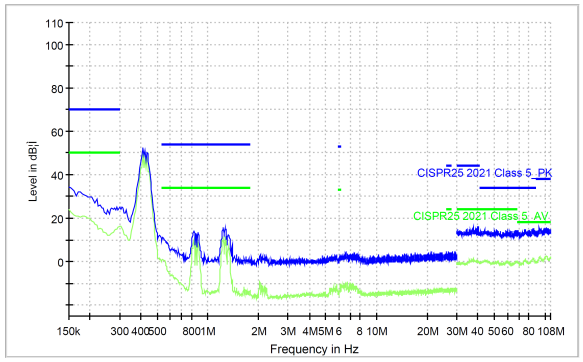
I_{OUT} = 6 A, PFM Mode

Figure 36. Power down by Enable



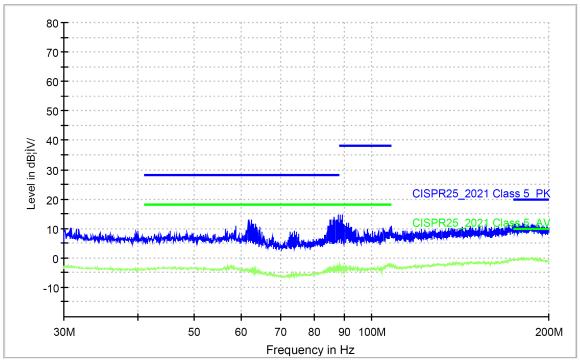
Frequency Tested: 150 kHz to 108 MHz, Positive

Figure 37. Conducted EMI versus CISPR25 Limits



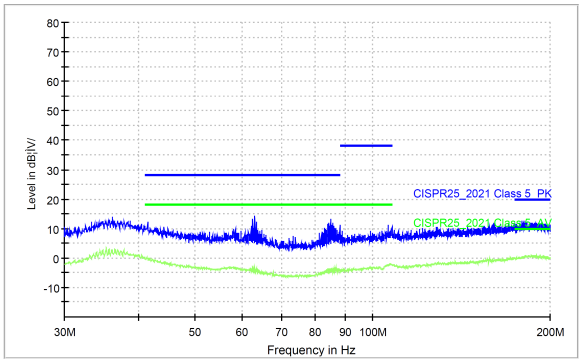
Frequency Tested: 150 kHz to 108 MHz, Negative

Figure 38. Conducted EMI versus CISPR25 Limits



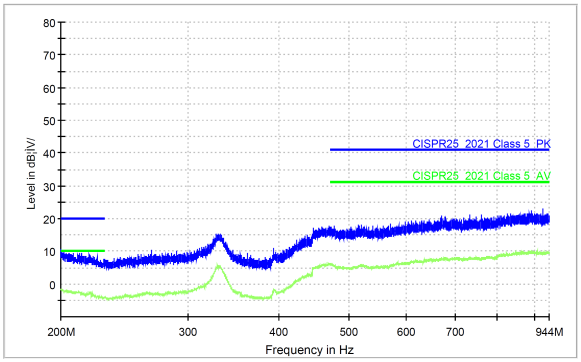
Analogue Broadcast, Frequency Tested: 30 MHz to 200 MHz, Horizon

Figure 39. Radiated EMI versus CISPR25 Limits



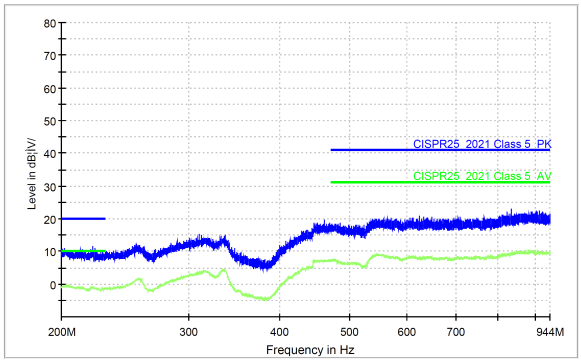
Analogue Broadcast, Frequency Tested: 30 MHz to 200 MHz, Vertical

Figure 40. Radiated EMI versus CISPR25 Limits



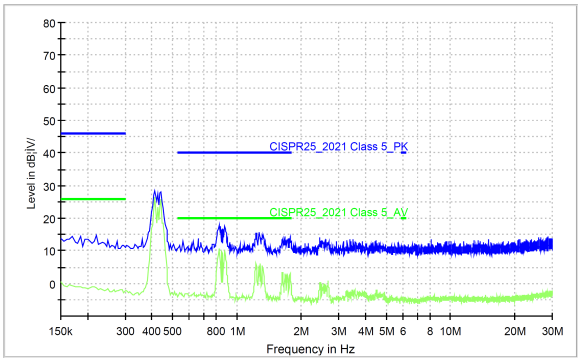
Analogue Broadcast, Frequency Tested: 200 MHz to 944 MHz, Horizon

Figure 41. Radiated EMI versus CISPR25 Limits



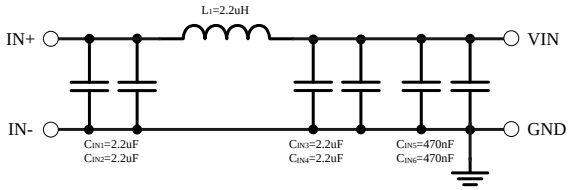
Analogue Broadcast, Frequency Tested: 200 MHz to 944 MHz, Vertical

Figure 42. Radiated EMI versus CISPR25 Limits



Analogue, Frequency Tested: 150 kHz to 30 MHz, Vertical

Figure 43. Radiated EMI versus CISPR25 Limits



F_{SW} = 2.1 MHz

Figure 44. Recommended Input EMI Filter

Layout

Layout Guideline

The performance of switching regulators heavily depends on the quality of the PCB layout, especially for thermal design and EMI design. Even if the schematic design is good, a bad PCB layout can disrupt the operation of the regulator.

1. Place a low ESR ceramic capacitor as close to the VIN pin and the ground as possible.
2. Make sure the top switching loop with power has the lowest impendence of grounding.
3. Use a large ground plane to connect to PGND directly. And add vias near PGND.
4. The output inductor should be placed close to the SW pin to minimize the SW area.
5. The FB terminal is sensitive to noise so the feedback resistor should be located as close as possible to the IC.
6. Keep the connection of the input capacitor and VIN as short and wide as possible.

Layout Recommendations

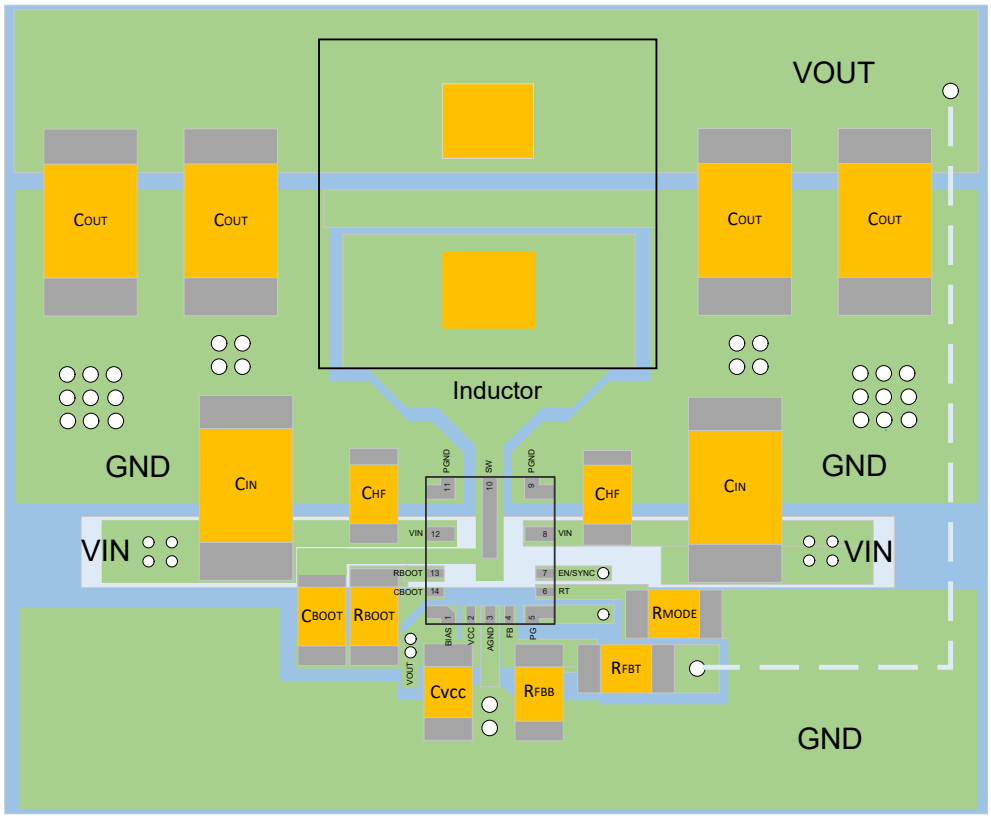
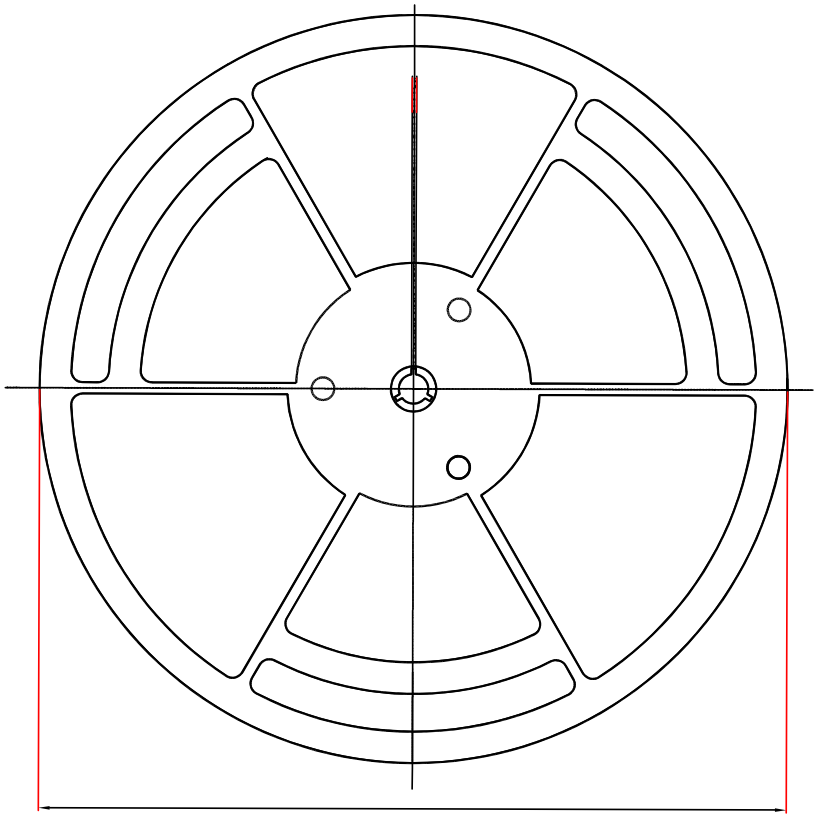
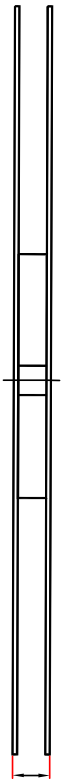
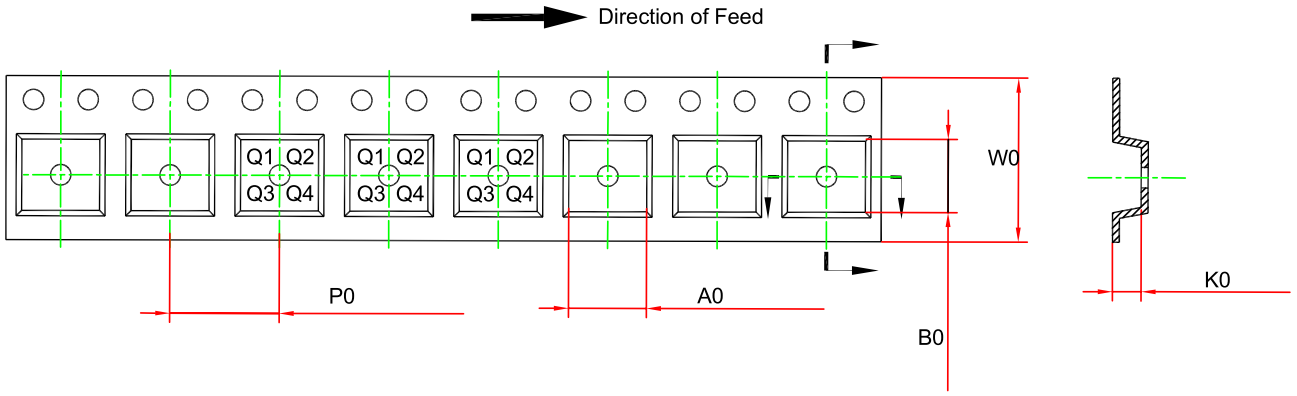


Figure 45. Layout Example

Tape and Reel Information





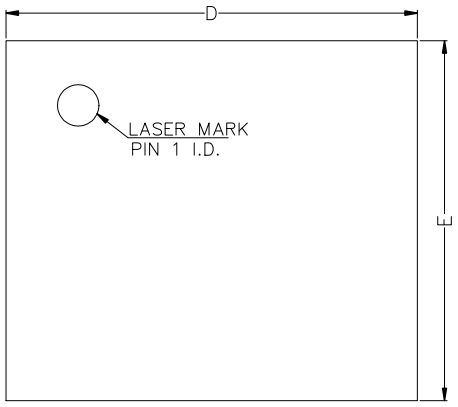


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPP366090Q-FC3R-S	QFN4X3.5-14	330	17.6	3.75	4.25	1.05	4.0	12.0	Q2
TPP366091Q-FC3R-S	QFN4X3.5-14	330	17.6	3.75	4.25	1.05	4.0	12.0	Q2
TPP366092Q-FC3R-S	QFN4X3.5-14	330	17.6	3.75	4.25	1.05	4.0	12.0	Q2

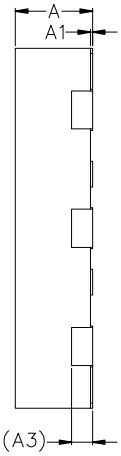
Package Outline Dimensions

QFN4X3.5-14

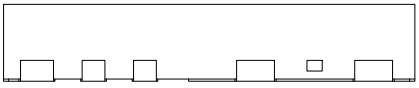
Package Outline Dimensions FC3(QFN4X3.5-14-A)



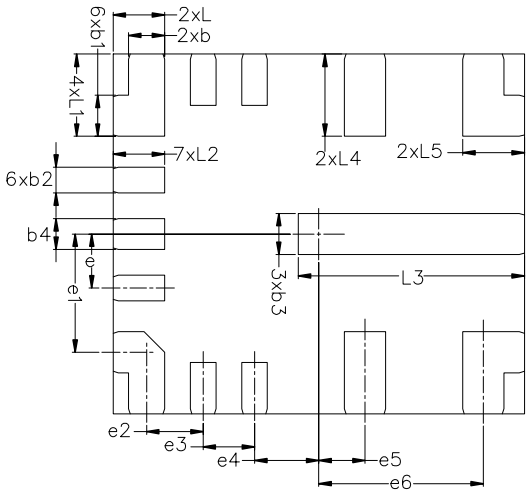
TOP VIEW



SIDE VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203 REF		0.008 REF	
b	0.300	0.400	0.012	0.016
b1	0.350	0.450	0.014	0.018
b2	0.200	0.300	0.008	0.012
b3	0.350	0.450	0.014	0.018
b4	0.250	0.350	0.010	0.014
D	3.900	4.100	0.154	0.161
E	3.400	3.600	0.134	0.142
e	0.425	0.625	0.017	0.025
e1	1.050	1.250	0.041	0.049
e2	0.450	0.600	0.018	0.024
e3	0.400	0.600	0.016	0.024
e4	0.525	0.725	0.021	0.029
e5	0.400	0.500	0.016	0.020
e6	1.500	1.700	0.060	0.067
L	0.400	0.600	0.016	0.024
L1	0.700	0.900	0.028	0.035
L2	0.400	0.600	0.016	0.024
L3	2.100	2.300	0.083	0.091
L4	0.700	0.900	0.028	0.035
L5	0.500	0.700	0.020	0.028

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. Dimensioning and tolerancing per ASME Y14.5M.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPP366090Q-FC3R-S	−40 to 125°C	QFN4X3.5-14	690QS	MSL2	Tape and Reel, 3000	Green
TPP366091Q-FC3R-S	−40 to 125°C	QFN4X3.5-14	691QS	MSL2	Tape and Reel, 3000	Green
TPP366092Q-FC3R-S	−40 to 125°C	QFN4X3.5-14	692QS	MSL2	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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