LPDDR4X Datasheet

BWMEDX32H2A-32Gb-X

BWMEDX32H2A-64Gb-X

Released

Ver.1.0

July. 2023

DAT-CES-0109-A

深圳佰维存储科技股份有限公司
BIWIN STORAGE TECHNOLOGY CO.,LTD.

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Revision History

Version	Date	Description
1.0	July. 2023	First Release

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1. Features

•Ultra-low-voltage core and I/O power supplies

– VDD1 = 1.70– 1.95V; 1.80V nominal

– VDD2 = 1.06– 1.17V; 1.10V nominal

– VDDQ = 0.57–0.65V; 0.60Vnominal

– or VDDQ = 1.06– 1.17V; 1.10V nominal

• Frequency range

– 2133– 10 MHz (data rate range: 4266–20 Mb/s/ pin)

•16n prefetch DDR architecture

•8 internal banks per channel for concurrent operation

•Single-data-rate CMD/ADR entry

•Bidirectional/ differential data strobe per byte lane

•Programmable READ and WRITE latencies (RL/WL)

•Programmable and on-the-fly burst lengths (BL = 16, 32)

•Directed per-bank refresh for concurrent bank operation and ease of command scheduling

•Up to 8.5GB/s per die

•On-chip temperature sensor to control self refresh rate

•Partial-array self refresh (PASR)

•Selectable output drive strength (DS)

•Clock-stop capability

•RoHS-compliant, “green” packaging

•Programmable VSS (ODT) termination

Options

• VDD1/VDD2/VDDQ: 1.80V/1.10V/0.60V or 1.1V

• Array configuration

– 1 Gig x 32 (2 channels x 16 I/O) 1G32

– 2 Gig x 32 (2 channels x 16 I/O) 2G32

• Device configuration

– 2 die in package

– 4 die in package

• FBGA “green” package

– 200-ball FBGA (10mm x 14.5mm)

• Speed grade, cycle time

– 468ps @ RL = 36/40

• Operating temperature range

– –25°C to +85°C

Clock Rate (MHz)	Data Rate (Mb/s/pin)	RL	WL
		DBI Disabled / Enabled	Set A/ Set B
2133	4266	36/40	18/34

Table1 Key Timing Parameters

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2. Product Information

Part ID	Capacity	Size	Package
BWMEDX32H2A-32Gb-X	32Gb	10mm*14.5mm*0.9mm	FBGA200
BWMEDX32H2A-64Gb-X	64Gb	10mm*14.5mm*0.9mm	FBGA200

		1G32 (32Gb)	2G32(64Gb)
Die organization in the package	Channel A,Rank 0	x16 mode x 1 die	x16 mode x 1 die
	Channel A,Rank 1	-	x16 mode x 1 die
	Channel B,Rank 0	x16 mode x 1 die	x16 mode x 1 die
	Channel B,Rank 1	-	x16 mode x 1 die
Die addressing	Memory Density (per die)	16Gb	16Gb
	Memory Density (per channel)	16Gb	16Gb
	Configuration	128Mb × 16DQ × 8 banks	128Mb × 16DQ × 8 banks
	Number of channels (per die)	1	1
	Number of banks (per channel)	8	8
	Array prefetch (bits, per channel)	256	256
	Number of rows (per channel)	131,072	131,072
	Number of columns (fetch boundaries)	64	64
	Page size (bytes)	2048	2048
	Channel density (bits per channel)	17,179,869,184	17,179,869,184
	Total density (bits per die)	17,179,869,184	17,179,869,184
	Bank address	BA[2:0]	BA[2:0]
	Row address	R[16:0]	R[16:0]
	Column address	C[9:0]	C[9:0]
	Burst starting address boundary	64 bit	64 bit

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2.1 MR0, MR[6:5], MR8, MR13, MR24 Definition

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0			Single-ended mode				Latency mode	REF
	OP[0] = 0b: Both legacy and modified refresh mode supported OP[1] = 0b: Device supports normal latency OP[5] = 1b: Device supports single-ended mode							
MR5	Manufacturer ID							
	1111 1111b							
MR6	**Revision ID1**							
	0000 0110b							
MR8	I/O width		Density					
	OP[7:6]=00b: x16/channel		OP[5:2] = 0110b: 16Gb single channel die					
MR13						VRO		
	OP[2]=0b: Normal operation (default) 1b: Output the VREF(CA) value on DQ7 and VREF(DQ) value on DQ6							
MR24	TRR mode				Unlimited MAC	MAC value		
	OP[3:0] = 1000b: Unlimited MAC; OP[7] = 0b: Disable (default); 1b: Reserved							

Table 2 Mode Register Definition

Note:

1. The contents of MR0, MR[6:5], MR8, MR13, and MR24 reflect information specific to each die in these packages.

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2.2 Part Numbering



Figure 1 Part Numbering

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2.3 Block Diagram

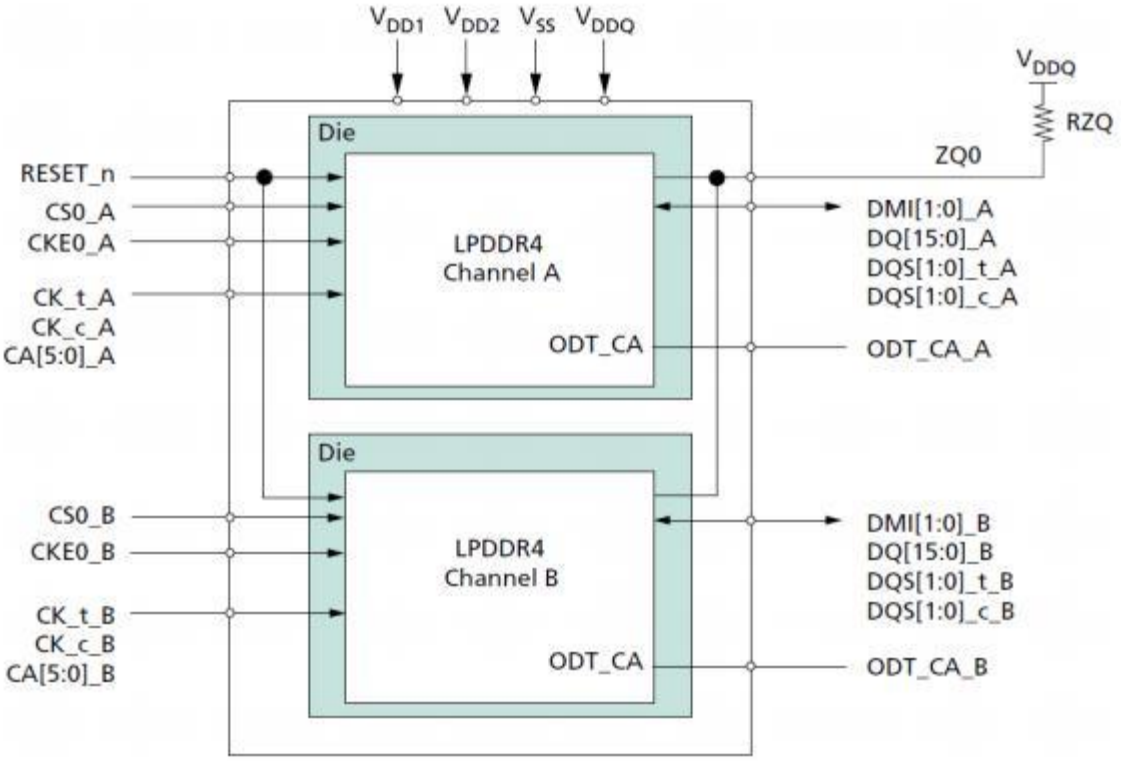

Figure 2-1 Dual-Die, Dual-Channel Package Block Diagram

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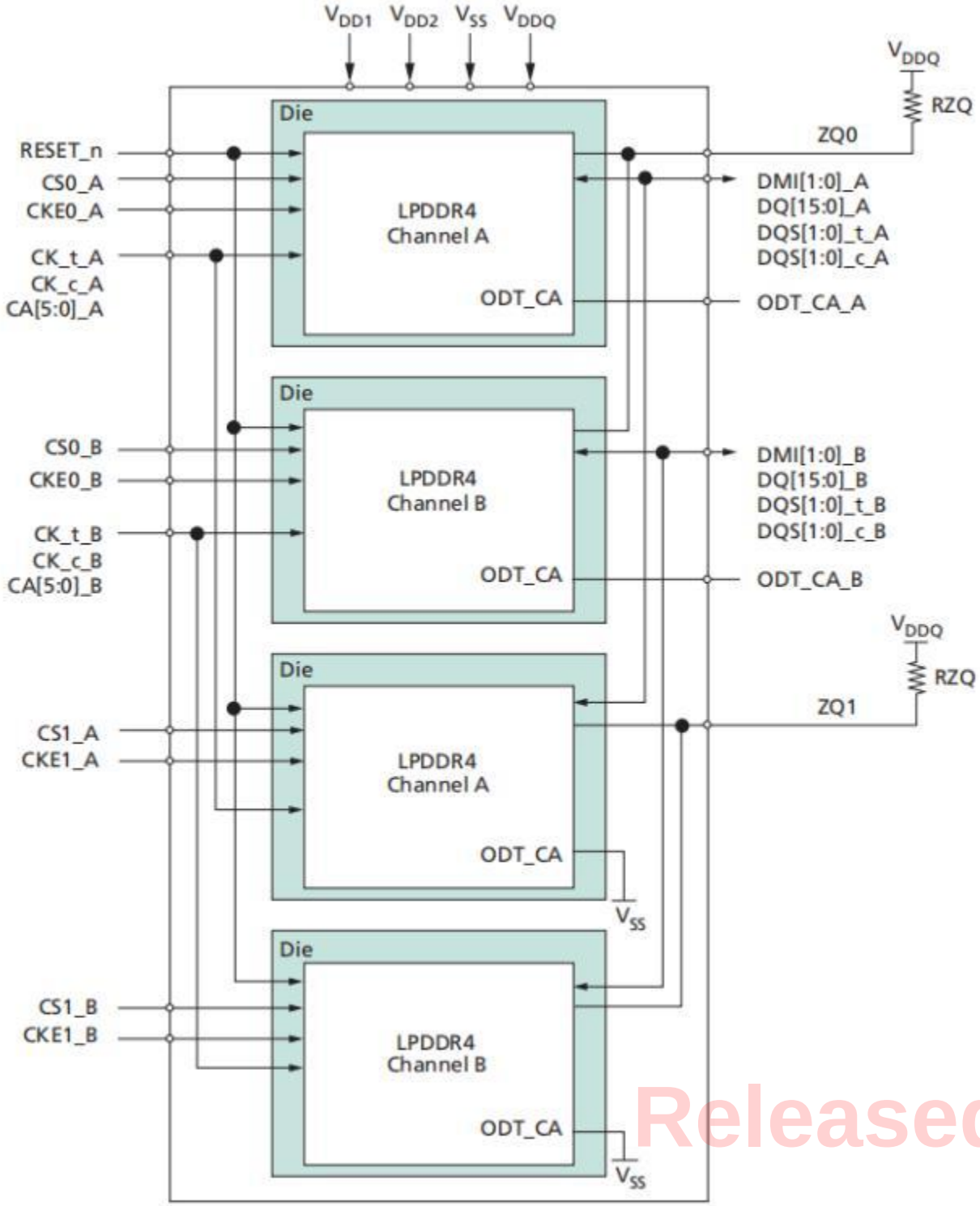

Note: 1. ODT(ca) for rank 0 of each channel is wired to the respective ODT ball. ODT(ca) for rank 1 of each channel is wired to V_{SS} in the package.

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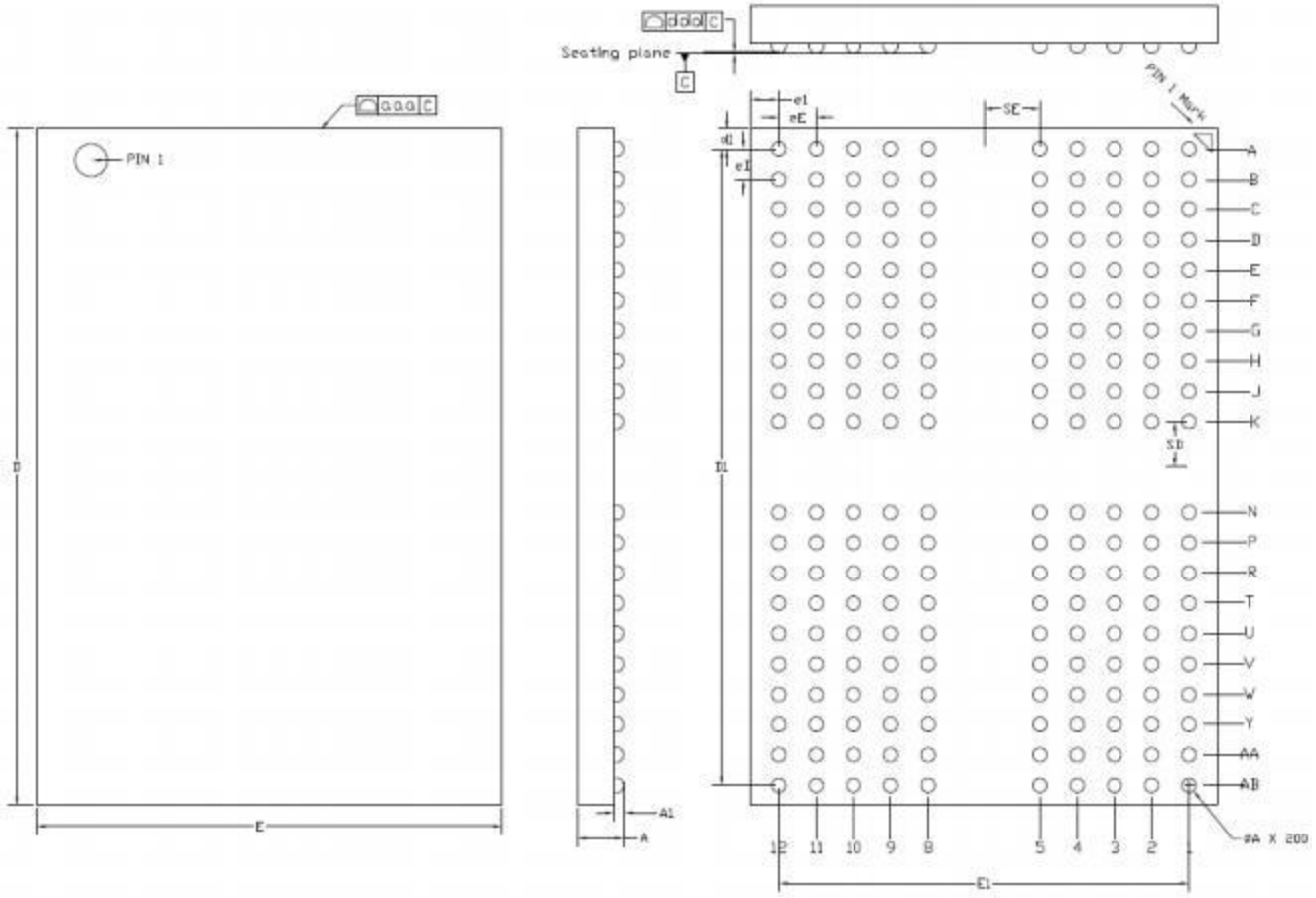
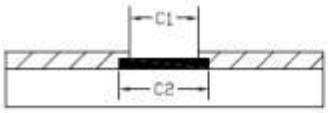
Figure 2-2 Quad-Die, Dual-Channel Package Block Diagram

2.4 Package Dimension



ITEM	Symble	Unit:mm MIN	NORM	MAX
BODY SIZE	D	14.40	14.50	14.60
	E	9.90	10.00	10.10
TOTAL THICNESS	A	0.80	0.90	1.00
STAND OFF	A1	0.18	0.21	0.24
EDGE BALL (CENTER TO CENTER)	D1		13.65	
	E1		8.80	
BALL PITCH	eD		0.65	
	eE		0.80	
even number of balls (eE/2,eD/2) odd number of balls (0)	SE		1.20	
	SD		0.98	
BALL COUNT	n		200	
BALL WIDTH (after reflow)	ΦA	0.29	0.32	0.35
Solder mask opening	C1	0.27	0.30	0.33
Ball pad diameter	C2	0.33	0.36	0.39
BALL TO OUTLINE	d1	0.32	0.42	0.52
	e1	0.50	0.60	0.70
Mold package warpage	aaa		0.08	
COPLANARITY	ddd		0.08	



200ball Ø0.3mm Dimensions apply to solder balls postreflow on Ø0.3mm SMD ball pads.

Notice:
1.Ball diameter: 0.3mm
2."●"---bumping ball location
3.In the diagram,there are 200 ball locations in all.

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Figure 3 Package Dimension (10mm*14.5mm*0.9mm)

2.5 Ball Assignment

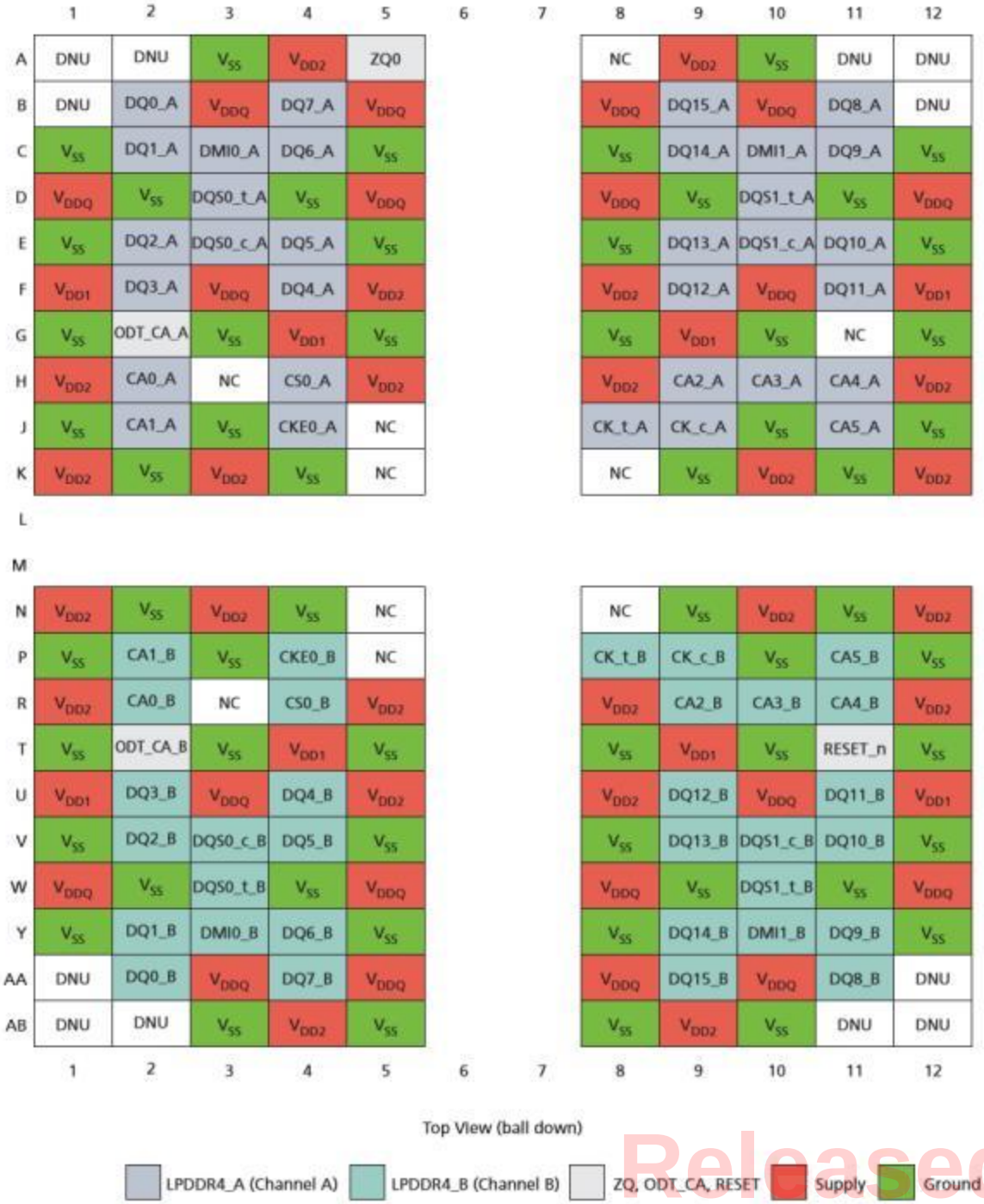

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Figure 4-1 Dual-Channel, Single-Rank Discrete FBGA

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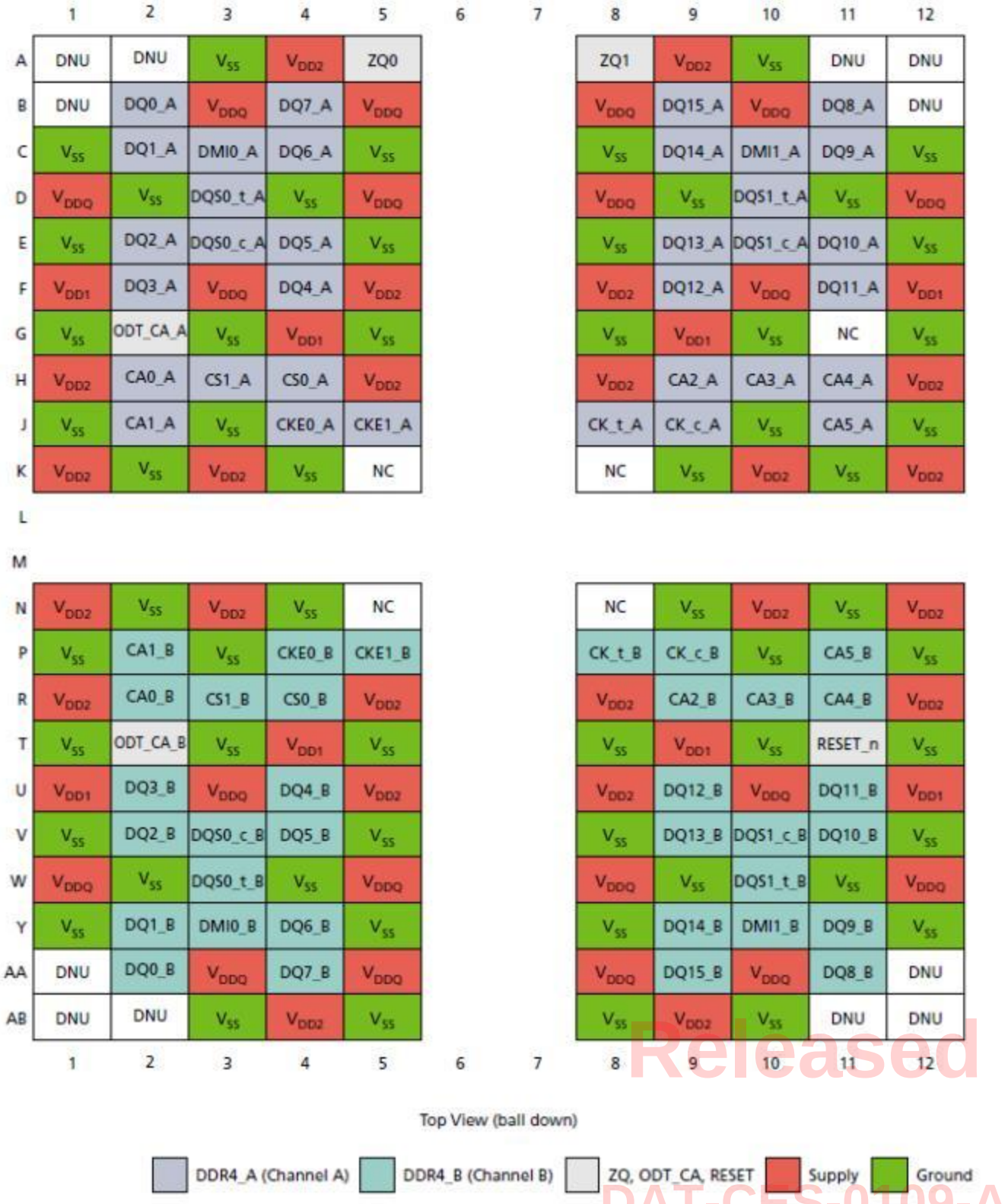

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Figure 4-2 Dual-Channel, Dual-Rank Discrete FBGA

Symbol	Type	Description
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel has its own clock pair.
CKE0_A, CKE1_A, CKE0_B, CKE1_B	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.
CS0_A, CS1_A, CS0_B, CS1_B	Input	Chip select: Each channel (A, B) has its own CS signals.
CA[5:0]_A, CA[5:0]_B	Input	Command/address inputs: Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals.
ODT_CA_A, ODT_CA_B	Input	LPDDR4X CA ODT Control: The ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to a valid logic level.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data input/output: Bidirectional data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	Data strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	Data Mask/Data Bus Inversion: DMI is a dual use bi-directional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion (DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own
ZQ0, ZQ1	Reference	ZQ Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240Ω ±1% resistor.
VDDQ, VDD1, VDD2	Supply	Power supplies: Isolated on the die for improved noise immunity.
VSS	Supply	Ground Reference: Power supply ground reference.
RESET_n	Input	RESET: When asserted LOW, the RESET pin resets both channels of the die.
DNU	_	Do not use: Must be grounded or left floating.
NC	_	No connect: Not internally connected.
RFU	_	Reserved Future Use: Not internally connected.

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Table 3 Ball/Pad Description

Note: ZQ1, CKE1_A, CKE1_B, CS1_A, and CS1_B balls are reserved for 2-rank package. For 1-rank package those balls are NC.

2.6 IDD Parameters(b) Single Die

VDD2=1.06–1.17V,VDDQ=0.57–0.65V or VDDQ = 1.06–1.17V; VDD1=1.70–1.95V

Symbol	Supply	Speed Grade	Unit	Note
		4266 Mb/s		
IDD0 1	VDD1	5.2	mA	
IDD0 2	VDD2	37.0		
IDD0 Q	VDDQ	0.75		
IDD2 P1	VDD1	2.2	mA	
IDD2 P2	VDD2	4.6		
IDD2 PQ	VDDQ	0.75		
IDD2 PS1	VDD1	2.2	mA	
IDD2 PS2	VDD2	4.6		
IDD2 PSQ	VDDQ	0.75		
IDD2 N1	VDD1	2.20	mA	
IDD2 N2	VDD2	20.0		
IDD2 NQ	VDDQ	0.75		
IDD2 NS1	VDD1	2.2	mA	
IDD2 NS2	VDD2	18.0		
IDD2 NSQ	VDDQ	0.75		
IDD3 P1	VDD1	2.20	mA	
IDD3 P2	VDD2	9.8		
IDD3 PQ	VDDQ	0.75		
IDD3 PS1	VDD1	2.2	mA	
IDD3 PS2	VDD2	9.8		
IDD3 PSQ	VDDQ	0.75		
IDD3 N1	VDD1	2.7	mA	
IDD3 N2	VDD2	26.0		
IDD3 NQ	VDDQ	0.75		
IDD3 NS1	VDD1	2.7	mA	
IDD3 NS2	VDD2	25.0		
IDD3 NSQ	VDDQ	0.75		
IDD4 R1	VDD1	4.7	mA	2,3
IDD4 R2	VDD2	285		
IDD4 RQ	VDDQ	79.6		
IDD4 W1	VDD1	3.3	mA	2
IDD4 W2	VDD2	217		
IDD4 WQ	VDDQ	0.75		

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(continued)

Symbol	Supply	Speed Grade	Unit	Note
		4266Mb/s		
IDD5 1	VDD1	34.0	mA	
IDD5 2	VDD2	164		
IDD5 Q	VDDQ	0.75		
IDD5 AB1	VDD1	4.7	mA	
IDD5 AB2	VDD2	29.0		
IDD5 ABQ	VDDQ	0.75		
IDD5 PB1	VDD1	4.7	mA	
IDD5 PB2	VDD2	29.0		
IDD5 PBQ	VDDQ	0.75		

Table 4 IDD Parameters – Single-Die

Notes:

1. Published IDD values except IDD4RQ are the maximum IDD values considering the worst case conditions of process, temperature, and voltage.
2. BL = 16, DBI disabled.
3. IDD4RQ value is reference only. Typical value. VOH = 0.5 × VDDQ, TC = 25°C.
4. IDD values reflect dual-channel operation with the same pattern for each channel.

VDD2=1.06–1.17V,VDDQ=0.57–0.65Vor VDDQ = 1.06–1.17V;VDD1=1.70–1.95V

Temperature	Supply	Full-Array Self Refresh Current	Unit
25°C	VDD1	0.47	mA
	VDD2	1.07	
	VDDQ	0.01	
85°C	VDD1	4.20	
	VDD2	12.00	
	VDDQ	0.90	

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Table 5 IDD6 Full-Array Self Refresh Current

Note:

1. IDD6 25°C is the typical, and IDD6 85°C is the maximum IDD value considering the worst-case conditions of process, temperature, and voltage.
2. IDD values reflect dual-channel operation with the same pattern for each channel.

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3. AC Timing

Parameter	Symbol	Min/ Max	Data Rate				Unit
			1600	3200	3733	4267	
Average clock period	tCK(AVG)	Min	1250	625	535	468	ps
		Max	100	100	100	100	ns
Average HIGH pulse width	tCH(AVG)	Min	0.46				tCK(AVG)
		Max	0.54				
Average LOW pulse width	tCL(AVG)	Min	0.46				tCK(AVG)
		Max	0.54				
Absolute clock period	tCK(ABS)	Min	tCK(AVG)min + tJIT(per)min				ps
Absolute clock HIGH pulse width	tCH(ABS)	Min	0.43				tCK(AVG)
		Max	0.57				
Absolute clock LOW pulse width	tCL(ABS)	Min	0.43				tCK(AVG)
		Max	0.57				
Clock period jitter	tJIT(per)allowed	Min	–70	–40	–34	–30	ps
		Max	70	40	34	30	
Maximum clock jitter between two consecutive clock cycles (includes clock period jitter)	tJIT(cc)allowed	Max	140	80	68	60	ps

Table 6 Clock Timing

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Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
DQS output access time from CK_t/CK_c	tDQSCK	Min	1500								ps	1
		Max	3500									
DQS output access time from CK_t/CK_c - voltage variation	tDQSCK_VOLT	Max	7								ps/mV	2
DQS output access time from CK_t/CK_c - temperature variation	tDQSCK_TEMP	Max	4								ps/°C	3
CK to DQS rank to rank variation	tDQSCK_rank2rank	Max	1.0								ns	4, 5
DQS_t, DQS_c to DQ skew total, per group, per access (DBI Disabled)	tDQSQ	Max	0.18								UI	6
DQ output hold time total from DQS_t, DQS_c (DBI Disabled)	tQH	Min	MIN(tQSH, tQSL)								ps	6
Data output valid window time total, per pin (DBI- Disabled)	tQW_total	Min	0.75			0.73			0.70		UI	6, 11
DQS_t, DQS_c to DQ skew total, per group, per access (DBI- Enabled)	tDQSQ_DBI	Max	0.18								UI	6
DQ output hold time total from DQS_t, DQS_c (DBI- Enabled)	tQH_DBI	Min	MIN(tQSH_DBI, tQSL_DBI)								ps	6
Data output valid window time total, per pin (DBI- Enabled)	tQW_total_DBI	Min	0.75			0.73			0.70		UI	6, 11
DQS_t, DQS_c differential output LOW time (DBI- Disabled)	tQSL	Min	tCL(ABS) – 0.05								tCK(AVG)	9, 11
DQS_t, DQS_c differential output HIGH time (DBI- Disabled)	tQSH	Min	tCH(ABS) – 0.05								tCK(AVG)	10, 11

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DQS_t, DQS_c differential output LOW time (DBI- Enabled)	tQSL- DBI	Min	tCL(ABS) – 0.045	tCK(AVG)	9, 11
DQS_t, DQS_c differential output HIGH time (DBI- Enabled)	tQSH- DBI	Min	tCH(ABS) – 0.045	tCK(AVG)	10, 11
Read preamble	tRPRE	Min	1.8	tCK(AVG)	
Read postamble	tRPST	Min	0.4 (or 1.4 if extra postamble is programmed in MR)	tCK(AVG)	
DQS Low- Z from clock	tLZ(DQS)	Min	(RL × tCK) + tDQSCK(MIN) - (tRPRE(MAX) × tCK) - 200ps	ps	
DQ Low- Z from clock	tLZ(DQ)	Min	(RL × tCK) + tDQSCK(MIN) - 200ps	ps	
DQS High- Z from clock	tHZ(DQS)	Min	(RL × tCK) + tDQSCK(MAX)+(BL/2 × tCK) + (tRPST(MAX) ×tCK) - 100ps	ps	
DQ High- Z from clock	tHZ(DQ)	Min	(RL × tCK) + tDQSCK(MAX) + tDQSQ(MAX) + (BL/2 × tCK) - 100ps	ps	

Table 7 Read Output Timing

Notes:

1. This parameter includes DRAM process, voltage, and temperature variation. It also includes the AC noise impact for frequencies >20 MHz and a max voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply with the component MIN/MAX DC operating conditions.

2. tDQSCK_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. The voltage supply noise must comply with the component MIN/MAX DC operating conditions. The voltage variation is defined as the max[abs(tDQSCK(MIN)@V1- tDQSCK(MAX)@V2), ABS(tDQSCK(MAX)@V1-tDQSCK(MIN)@V2)]/ABS(V1-V2).

3. tDQSCK_temp MAX delay variation as a function of temperature.

4. The same voltage and temperature are applied to tDQSCK_rank2rank.

5. tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

6. DQ-to-DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER.

7. The deterministic component of the total timing.

8. This parameter will be characterized and guaranteed by design.

9. tQSL describes the instantaneous differential output low pulse width on DQS_t -DQS_c, as measured from one falling edge to the next consecutive rising edge.

10. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from one falling edge to the next consecutive rising edge.

11. This parameter is a function of input clock jitter. These values assume MIN tCH(ABS) and tCL(ABS). When the input clock jitter MIN tCH(ABS) and tCL(ABS) is 0.44 or greater than tCK(AVG), the MIN value of tQSL will be tCL(ABS) - 0.04 and tQSH will be tCH(ABS) - 0.04.

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Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
Rx timing window totalat VdIVWvoltage levels	TdIVW_ total	Max	0.22					0.25			UI	1, 2, 3
DQ and DMI input pulse width (at VCENT DQ)	TdIPW	Min	0.45								UI	7
DQ- to- DQS offset	t_{DQS2DQ}	Min	200								ps	6
		Max	800									
DQ- to- DQ offset	t_{DQDQ}	Max	30								ps	7
DQ- to- DQS offset temperature variation	t_{DQS2DQ_temp}	Max	0.6								ps/°C	8
DQ- to- DQS offset voltage variation	t_{DQS2DQ_volt}	Max	33								ps/50mV	9
DQ- to- DQS offset rank to rank variation	$t_{DQS2DQ_rank2rank}$	Max	200								ps	10, 11
WRITE command to first DQS transition	t_{DQSS}	Min	0.75								tCK(AVG)	
		Max	1.25									
DQS input HIGH- level width	t_{DQSH}	Min	0.4								tCK(AVG)	
DQS input LOW- level width	t_{DQSL}	Min	0.4								tCK(AVG)	
DQS falling edge to CK setup time	t_{DSS}	Min	0.2								tCK(AVG)	
DQS falling edge from CK hold time	t_{DSH}	Min	0.2								tCK(AVG)	
Write postamble	t_{WPST}	Min	0.4 (or 1.4 if extra postamble is programmed in MR)								tCK(AVG)	
Write preamble	t_{WPRE}	Min	1.8								tCK(AVG)	

Table 8 Write Timing

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Notes:

1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.

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2. Rx differential DQ-to-DQS jitter total timing window at the VdIVW voltage levels.
3. Defined over the DQ internal VREF range. The Rx mask at the pin must be within the in- ternal VREF(DQ) range irrespective of the input signal common mode.
4. Rx mask defined for one pin toggling with other DQ signals in a steady state.
5. DQ-only minimum input pulse width defined at the VCENT_DQ(pin_mid).
6. DQ-to-DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage, and

temperature variations.

7. DQ-to-DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.

8. tDQS2DQ (MAX) delay variation as a function of temperature.

9. tDQS2DQ (MAX) delay variation as a function of the DC voltage variation for VDDQ and VDD2. It includes the VDDQ and VDD2 AC noise impact for frequencies >20 MHz and MAX voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package.

10. The same voltage and temperature are applied to tDQS2DQ_rank2rank.

11. tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

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Parameter	Symbol	Min/ Max	Data Rate				Unit	Notes
			1600	3200	3733	4267		
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	Min	MAX(7 .5ns, 4*n*CK)				ns	1
Delay from valid command to CKE input LOW	tCMDCKE	Min	MAX(1 .75ns, 3*n*CK)				ns	1
Valid clock requirement after CKE input LOW	tCKELCK	Min	MAX(5ns, 5*n*CK)				ns	1
Valid CS requirement before CKE input LOW	tCSCKE	Min	1.75				ns	
Valid CS requirement after CKE input LOW	tCKELCS	Min	MAX(5ns, 5*n*CK)				ns	1
Valid Clock requirement before CKE Input HIGH	tCKCKEH	Min	MAX(1 .75ns, 3*n*CK)				ns	1
Exit power- down to next valid command delay	tXP	Min	MAX(7 .5ns, 5*n*CK)				ns	1
Valid CS requirement before CKE input HIGH	tCSCKEH	Min	1.75				ns	
Valid CS requirement after CKE input HIGH	tCKEHCS	Min	MAX(7 .5ns, 5*n*CK)				ns	1
Valid clock and CS requirement after CKE input LOW after MRW command	tMRWCKEL	Min	MAX(14ns, 10*n*CK)				ns	1
Valid clock and CS requirement after CKE input LOW after ZQCALSTART command	tZQCKE	Min	MAX(1 .75ns, 3*n*CK)				ns	1

Table 9 CKE Input Timing

Note:

1. Delay time has to satisfy both analog time(ns) and clock count (nCK). For example, tCMDCKE will not expire until CK has toggled through at least 3 full cycles (3tCK) and 3.75ns has transpired. The case that 3nCK is applied to is shown below.

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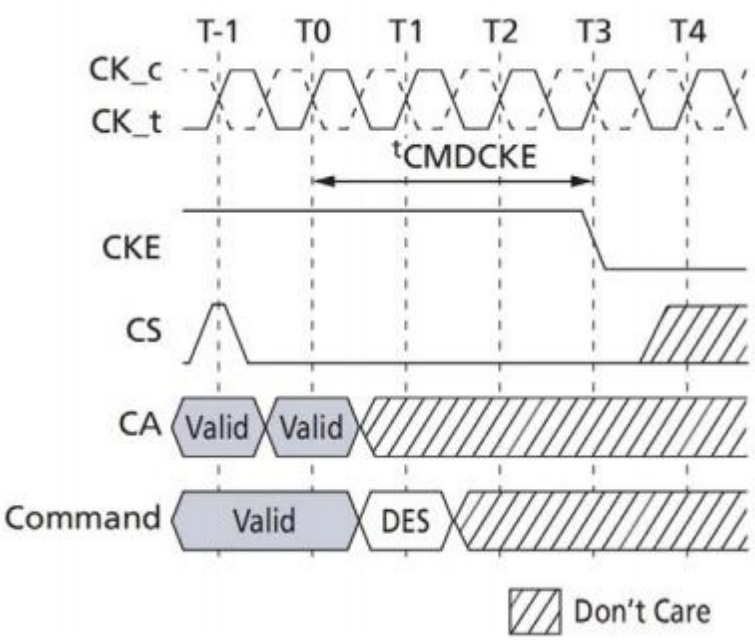

Figure 5 tCMDCKE Timing

Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
Command/address valid window (referenced from CA VIL/VIH to CK VIX)	tcIVW	Min	0.3								tCK(AVG)	1, 2, 3
Address and control input pulse width (referenced to VREF)	tcIPW	Min	0.55	0.55	0.55	0.6	0.6	0.6	0.6	0.6	tCK(AVG)	4

Table 10 Command Address Input Timing

Notes:

1. CA Rx mask timing parameters at the pin including voltage and temperature drift.
2. Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
3. Defined over the CA internal VREF range. The Rx mask at the pin must be within the internal VREF(CA) range irrespective of the input signal common mode.
4. CA only minimum input pulse width defined at the VCENT_CA(pin mid).

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Parameter	Symbol	Min/ Max	Value	Unit
Clock cycle time	tCKb	Min	18	ns
		Max	100	
DQS output data access time from CK	tDQSCKb	Min	1.0	ns
		Max	10.0	
DQS edge to output data edge	tDQSQb	Max	1.2	ns

Table 11 Boot Timing Parameters (10–55 MHz)

Parameter	Symbol	Min/ Max	Data Rate							Unit
			1066	1600	2133	2667	3200	3733	4267	
MODE REGISTER WRITE (MRW) command period	^{t}MRW	Min	MAX(10ns, 10nCK)							ns
MODE REGISTER SET command delay	^{t}MRD	Min	MAX(14ns, 10*n*CK)							ns
MODE REGISTER READ (MRR) command period	^{t}MRR	Min	8							tCK(avg)
Additional time after tXP has expired until the MRR command may be issued	^{t}MRRI	Min	tRCD(min) + 3nCK							ns
Delay from MRW command to DQS driven out	^{t}SDO	Max	MAX(12nCK, 20ns)							ns

Table 12 Mode Register Timing Parameters

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Parameter	Symbol	Min/ Max	Data Rate								Unit	Notes
			533	1066	1600	2133	2667	3200	3733	4267		
READ latency (DBI disabled)	RL-A	Min	6	10	14	20	24	28	32	36	tCK(avg)	
READ latency (DBI enabled)	RL-B	Min	6	12	16	22	28	32	36	40	tCK(avg)	
WRITE latency (Set A)	WL-A	Min	4	6	8	10	12	14	16	18	tCK(avg)	
WRITE latency (Set B)	WL-B	Min	4	8	12	18	22	26	30	34	tCK(avg)	
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	Min	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge)								ns	
Minimum self refresh time (entry to exit)	tSR	Min	MAX(15ns, 3nCK)								ns	
Self refresh exit to next valid command delay	tXSR	Min	MAX(tRFCab + 7.5ns, 2nCK)								ns	
CAS-to-CAS delay	tCCD	Min	8								tCK(avg)	
CAS-to-CAS delay masked write	tCCDMW	MIN	32								tCK(avg)	
Internal READ-to-PRE-CHARGE command delay	tRTP	Min	MAX(7.5ns, 8nCK)								ns	
RAS-to-CAS delay	tRCD	Min	MAX(18ns, 4nCK)								ns	
Row precharge time (single bank)	tRPpb	Min	MAX(18ns, 3nCK)								ns	
Row precharge time (all banks)	tRPab	Min	MAX(21ns, 3nCK)								ns	
Row active time	tRAS	Min	MAX(42ns, 3nCK)								ns	
		Max	MIN(9 × tREFI × Refresh Rate1, 70.2)								μs	
Write recovery time	tWR	Min	MAX(18ns, 4nCK)								ns	
Write-to-read delay	tWTR	Min	MAX(10ns, 8nCK)								ns	
Active bank A to active bank B	tRRD	Min	MAX(10ns, 4nCK)							MAX(7.5ns, 4nCK)	ns	1
Precharge-to-precharge delay	tPPD	Min	4								tCK(avg)	2
Four-bank activate window	tFAW	Min	40							30	ns	1
Delay from SRE command to CKE input LOW	tESCKE	Min	MAX(1.75ns, 3nCK)								–	3

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Table 13 Core Timing Parameters

Notes:

1.Precharge to precharge timing restriction does not apply to AUTO PRECHARGE commands.

2.Delay time has to satisfy both analog time(ns) and clock count (nCK). It means that tESCKE will not expire until CK has toggled through at least three full cycles (3 tCK) and 1.75ns has transpired. The case which 3nCK is applied to is shown below.

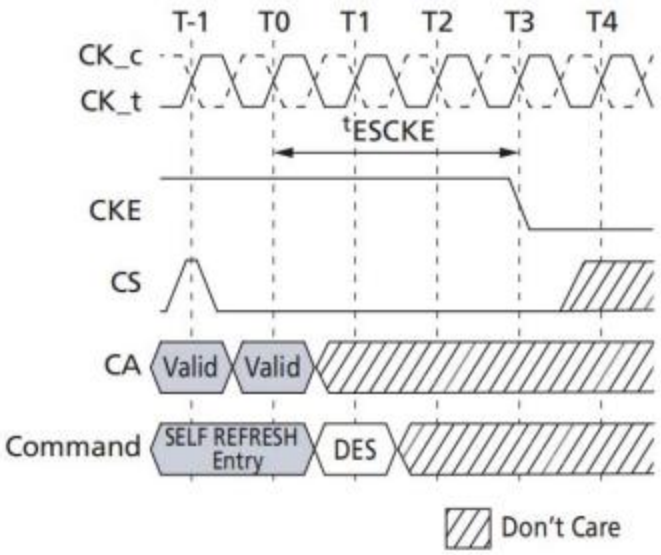

Figure 6 tESCKE Timing

Parameter	Symbol	Min/Max	Data Rate
			533-4267
CA ODT value update time	t_{ODTUP}	Min	RU(20ns/tCK(AVG))

Table 14 CA Bus ODT Timing

Parameter	Symbol	16Gb per Channel	Unit
REFRESH cycle time (all banks)	tRFCab	380	ns
REFRESH cycle time (per bank)	tRFCpb	190	ns
Per bank refresh to per bank refresh time (different bank)	tPBR2PBR	90	ns

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Table 15 Refresh Requirement Parameters

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Note: 1. This table only describes refresh parameters which are density dependent. Refer to Refresh Requirement section in General LPDDR4X specification for all the refresh parameters.

Parameter	Symbol	Min/ Max	Data Rate				Unit	Note
			1600	3200	3733	4267		
Valid clock requirement after CKE input LOW	tCKELCK	Min	MAX(5ns, 5*n*CK)				tCK	
Data setup for VREF training mode	$t_{DStrain}$	Min	2				ns	
Data hold for VREF training mode	$t_{DHtrain}$	Min	2				ns	
Asynchronous data read	tADR	Max	20				ns	
CA BUS TRAINING command- to- command delay	tCACD	Min	RU(tADR/ tCK)				tCK	1
Valid strobe requirement before CKE LOW	tDQSCKE	Min	10				ns	
First CA BUS TRAINING command following CKE LOW	tCAENT	Min	250				ns	
VREF step time – multiple steps	tVREFca_ LONG	Max	250				ns	
VREF step time – one step	tVREFca_ SHORT	Max	80				ns	
Valid clock requirement before CS HIGH	tCKPRECS	Min	2tCK + tXP				–	
Valid clock requirement after CS HIGH	tCKPSTCS	Min	MAX(7 .5ns, 5*n*CK)				–	
Minimum delay from CS to DQS toggle in command bus training	tCS_ VREF	Min	2				tCK	
Minimum delay from CKE HIGH to strobe High- Z	tCKEHDQS	Min	10				ns	
CA bus training CKE HIGH to DQ tristate	tMRZ	Min	1.5				ns	
ODT turn- on latency from CKE	tCKELODTon	Min	20				ns	
ODT turn- off latency from CKE	tCKEHODToff	Min	20				ns	
Exit command bus training mode to next valid command delay	tXCBT_ Short	Min	MAX(200ns, 5*n*CK)				–	2
	tXCBT_ Middle	Min	MAX(200ns, 5*n*CK)				–	2
	tXCBT_ Long	Min	MAX(250ns, 5*n*CK)				–	2

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Table 16 CA Bus Training Parameters

Notes:

1. If tCACD is violated, the data for samples which violate tCACD will not be available, ex- cept for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.

2. Exit command bus training mode to next valid command delay time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in tFC value mapping table. Additionally exit command bus training mode to next valid command delay time may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.

Symbol	800–2133 MHz	Unit
tODTon, min	1.5	ns
tODTon, max	3.5	ns
tODToff, min	1.5	ns
tODToff, max	3.5	ns

Table 17 Asynchronous ODT Turn On and Turn Off Timing

Parameter	Symbol	Min/ Max	Data Rate								Unit
			533	1066	1600	2133	2667	3200	3733	4267	
DQS output access time from CK_t/CK_c (derated)	tDQSCKd	Max	3600								ns
RAS-to-CAS delay (derated)	tRCDd	Min	tRCD + 1.875								ns
ACTIVATE-to-ACTIVATE command period (same bank, derated)	tRCd	Min	tRC + 3.75								ns
Row active time (derated)	tRASd	Min	tRAS + 1.875								ns
Row precharge time (derated)	tRPd	Min	tRP + 1.875								ns
Active bank A to active bank B (derated)	tRRD	Min	tRRD + 1.875								ns

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Table 18 Temperature Derating Parameters

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