Synchronous Buck Controller with Temperature-Compensated Overcurrent Protection and Programmable Thermal

Check for Samples: LGS51403

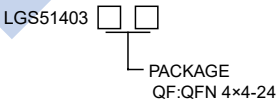
Features

- Wide Input Voltage Range: 3V-20V
- Switching Frequency Range:200KHz-1.2MHz
- Up to 97% Efficiency and 93% Duty Cycle
- Inductor-DCR-Based Overcurrent Protection with Thermal Compensation
- 0.6V Reference with ±1% Feedback Accuracy
- 30-ns Minimum T_{ON} for Low VOUT
- Integrated High-Current MOSFET Drivers
  ——Adaptive Deadtime Control
- Ultrafast Line and Load Transient Response
- Integrated VDD Bias Supply LDO Sub regulator
- Precision Enable with Hysteresis
- Frequency Synchronization
- Programmable Soft-Start with Tracking
- Monotonic Pre-biased Start-up
- Output good identification PG signal
- Output Remote Sense
- Junction temperatures range from -40℃ to +125℃

Applications

- General purpose DC-DC controller
- POL Modules
- Industrial computers, Notebook, Desktop
- Telecommunications Infrastructure
- Computing and storage modules

Ordering Information



Part	Package	Top Mark
LGS51403QF	QFN 4×4-24	LGS51403YW
Y: year code	W: week code	

Description

LGS51403 is a feature-rich synchronous buck controller that achieves superior efficiency in high power density and POL. Stable performance and wide input/output voltage range enable LGS51403 to offer a variety of DC-DC regulator solutions. The resistor-programmable switching frequency from 200 kHz to 1.2 MHz and integrated, high-current MOSFET gate drivers with adaptive deadtime offer flexibility to optimize solution size and maximize conversion efficiency. High precision and low output voltage are easily obtained with a 0.6V,1% accurate voltage reference together with a 30ns high-side MOSFET minimum controllable on-time. Using lossless inductor DCR current sensing and an inexpensive BJT to sense temperature remotely at the inductor, LGS51403 supports accurate and thermally compensated overcurrent protection.

LGS51403 has a conventional voltage mode control loop with high gain bandwidth error amplifier and PWM input voltage feedforward to simplify compensation design and enable excellent transient response throughout the full line voltage and load current ranges. Forced-PWM operation eliminates frequency variation to minimize EMI in sensitive applications. Power Good circuit provides power-rail sequencing and fault reporting.

Other features include programmable system-level thermal shutdown with automatic recovery, output voltage remote sense, configurable soft-start, monotonic start-up into pre-biased loads, an integrated bias supply LDO regulator, external power supply tracking, precision enable with customizable hysteresis for programmable line undervoltage lockout, and synchronization capability for beat frequency sensitive and multiregulated applications.

Draft Version

Typical Application Diagram

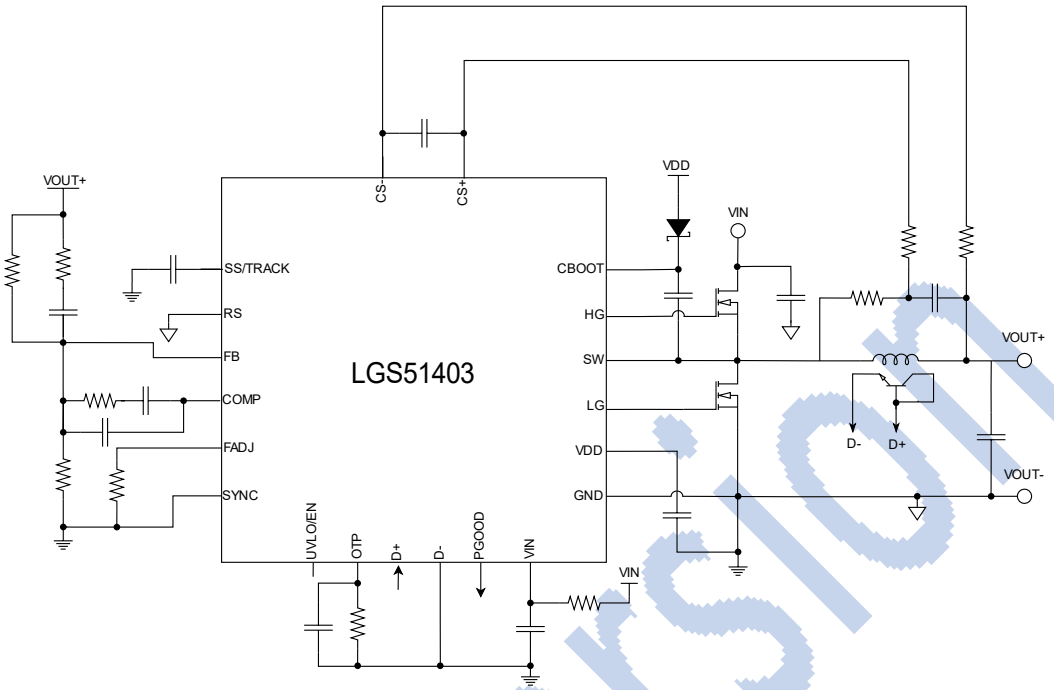


Figure 1 Typical Application

Draft version

Copyright © 2022- present Legend- Si (Nanjing) Semiconductor Co., Ltd.

Package and Pinout Diagram

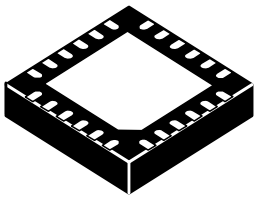


Figure 2 QFN4X4-24L Package

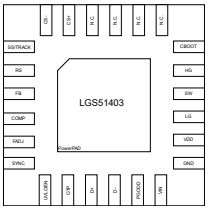


Figure 3 PACKAGE REFERENCE TOP VIEW

Pin Functions

Table 1 Pin Function Description

NO.	NAME	I/O/P(1)	DESCRIPTION
1	SS/TRACK	I/O	Soft-start or tracking input. This pin allows a predetermined startup rate to be defined with the use of a capacitor to GND. SS/TRACK can also be controlled with an external voltage source for tracking applications.
2	RS	I	Negative remote sense input. This pin eliminates the voltage drop between GND and the local ground adjacent to the load. In particularly noisy environments, connect an RC filter between RS and GND. Connect RS to GND at the IC if not used.
3	FB	I	Feedback input. FB is the inverting input of the error amplifier in the voltage mode control loop, which can detect the output voltage fluctuation and feed it back to the IC and also be used to configure the output voltage.
4	COMP	O	Compensation node output. This pin is an output voltage control-loop error amplifier output. COMP is connected to the FB pin through a compensation network to ensure stability.
5	FADJ	I	Frequency adjust input. The switching frequency is programmable between 200 kHz and 1.2 MHz by virtue of the size of resistor connected to this pin and GND.
6	SYNC	I	Synchronization input. This pin enables PLL synchronization to an external clock frequency. If a SYNC signal is not present, the switching frequency defaults to the frequency set by the FADJ pin. This pin should be tied to GND if not used.
7	UVLO/EN	I	High precision enables and undervoltage lock function.
8	OTP	I	Overtemperature protection (OTP) output. A resistor and 0.1 μF capacitor from this pin to GND sets the overtemperature protection setpoint for the DC-DC power supply solution using the temperature sensed at a remotely connected thermal diode. Connect this pin to GND if the system level OTP function is not required.
9	D+	I	External temperature sense. A 2N3904-type NPN transistor configured as a remote thermal diode with the base and collector shorted should be connected to this pin to sense the inductor temperature. The sensed temperature is used to compensate for the inductor DCR drift over temperature and to implement system-level thermal shutdown protection.
10	D-	I	External temperature sense return. This pin is the return current path for the external NPN transistor configured as a thermal diode. This trace should be routed

Draft Version

			as a differential pair with the D+ trace back to the LGS51403 to avoid excessive coupling from external noise sources. Connect D– to GND.
11	PGOOD	O	Power Good monitor output. This open-drain output goes low during overcurrent, short-circuit, UVLO, output overvoltage and undervoltage, overtemperature, or when the output is not regulated (such as an output pre-bias). An external pullup resistor to VDD or to an external rail is required. Included is a 20 μs deglitch filter. The PGOOD voltage should not exceed 5.5 V.
12	VIN	P	Input voltage rail. This input is used to provide the feedforward modulation for output voltage control and for generating the internal bias supply voltage. Decouple VIN to GND locally with a 1μF ceramic capacitor. For better noise rejection, connect to the power stage input rail with an RC filter.
13	GND	G	Common ground terminal of analog signal.
14	VDD	P	Bias supply rail. The pin is a secondary adjustable 4.7V internal power rail. The VDD provides the offset voltage to the gate drive and also provides the current to the CBOOT to enable the high-end power tube to switch on and off properly. Use 10μF ceramic capacitors to locally decouple the VDD to GND.
15	LG	O	Low-side MOSFET gate drive output. This pin is the low-side N-FET gate connection.
16	SW	P	Power stage switch-node connection. This pin is the high-side N-FET gate driver returns.
17	HG	O	High-side MOSFET gate drive output. This pin is the high-side N-FET gate connection.
18	CBOOT	P	Bootstrap circuit pin. Connect a 100nF ceramic capacitor between CBOOT and SW. This pin is the high-side N-FET gate driver power supply.
19-22	NC	G	No connection. Connect directly to GND.
23	CS+	I	The noninverting input of the current-sense comparator. 9.9μA of nominal offset current at room temperature is provided to adjust the current limit setpoint.
24	CS-	I	The inverting input of the current-sense comparator.
-	EP	P	Exposed die attach pad. Connect this pad to the PCB ground plane using multiple thermal vias.

(1) I=Input, O=Output, G=Ground

Draft Version

Absolute Maximum Ratings (1)

Table 2 Temperature range: -40℃-+125℃

Parameter		MIN	MAX	UNIT
Voltage	VIN, CS+, CS-, SW	-0.3	22	V
	VDD, PGOOD	-0.3	6	
	SS/TRACK, SYNC, FADJ, COMP, FB, RS	-0.3	VDD + 0.3	
	UVLO/EN	-0.3	MIN(VIN+0.3,6)	
	CBOOST	-0.3	24	
	CBOOST to SW	-0.3	6	
	CS+ to CS-	-1	1	
	OTP, D+, D-	-0.3	VDD	
Storage temperature, T_{stg}		- 65	+150	℃
Junction Temperature, T_J		- 40	+125	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.

(2) All voltages are with respect to the network ground pin unless otherwise noted.

(3) The SW pin can tolerate negative voltage spikes as low as -10 V and as high as 30 V for a duration up to 10 ns. The CBOOT pin can tolerate positive voltage spikes as high as 35 V for a duration up to 10 ns.

(4) In practical application, parasitic inductance in a real application may result in the SW voltage ringing negative.

Recommended Operating Conditions (1)

Table 3

Parameter			MIN	MAX	UNIT
VIN	Input Voltage	VIN and VDD two power rail	3	20	V
		VIN and VDD are on the same power rail	3	5.5	V
SW	SW pin to GND voltage		-0.3	20	V
VDD	VDD pin to GND voltage		2.6	5.5	V
PGOOD	PGOOD pin to GND voltage		0	5.5	V
UVLO/EN	UVLO/EN pin to GND voltage		0	MIN(VIN,5.5)	V
SS/TRACK	SS/TRACK pin to GND voltage		0	VDD	V
SYNC	SYNC pin to GND voltage		0	5.5	V
RS	RS pin to GND voltage		-0.1	0.1	V
TJ	Operating junction temperature T_J		- 40	+ 125	℃
TA	Operating free-air temperature		- 40	+ 125	℃

(1) The recommended working conditions are designed to make IC work normally, but do not guarantee the performance of specific parameters. For details, please refer to the technical specifications in the following article.

(2) VDD is the output of the internal linear regulator bias supply. Under normal operating conditions, where VIN is greater than 5.5 V, VDD must not be tied to any external voltage source. In an application where VIN is between 3.0 V and 5.5 V, connect VIN to VDD to maximize VDD voltage.

Unofficial version

Detailed Description

Overview

Distributed power architectures are commonly used in communications infrastructure equipment and computing systems that use an intermediate bus and multiple downstream DC-DC regulators. Asics, FPGA and microprocessors as loads require voltage levels to be stable within a certain range. The advantage of POL DC-DC regulators are efficiency, size, load transient response and cost. LGS51403 is a feature-rich, easy-to-use synchronous PWM DC-DC step-down controller capable of delivering ultra-high current outputs for demanding high power density POL applications. Input voltage range of 3 - 20 V compatible with various intermediate bus power rails and batteries (typical 3.3V, 5V, 12V rails). The output voltage is adjustable from 0.6V to 93% VIN with ±1% feedback system regulation accuracy over the entire junction temperature range. With an accurate, adjustable and thermally compensated inductor DCR based current limit setpoint, ferrite and composite core inductors with low DCR and small footprint can be specified to maximize efficiency and reduce power loss. High-current gate drivers with adaptive deadtime are used for the high-side and low-side MOSFETs to provide further efficiency gains.

LGS51403 employs a voltage-mode control loop with output voltage remote sense, input voltage feedforward modulation, and a high gain-bandwidth error amplifier to accurately regulate the output voltage over substantial load, line, and temperature ranges. The switching frequency is programmable between 200 kHz and 1.2 MHz through a resistor or an external synchronization signal.

LGS51403 thermally compensates for the temperature coefficient of the inductor's winding resistance by sensing the inductor temperature with an external NPN transistor configured as a thermal diode. The same thermal diode also monitors the PCB temperature to initiate a thermal shutdown in the event that the sensed temperature exceeds the programmed thermal shutdown setpoint.

LGS51403 comes in a 4mm x 4mm, 24-pin QFN package. This device offers high levels of integration by including MOSFET gate drivers, a low dropout (LDO) bias supply linear regulator, and comprehensive fault protection features to enable highly flexible, reliable, energy-efficient, and high-power density regulator solutions. Multiple fault conditions are accommodated, including overvoltage, undervoltage, overcurrent, and overtemperature.

Input Range: VIN

LGS51403 operational input voltage range is from 3 V to 20 V. It uses an internal LDO sub-regulator to provide a 4.7V bias rail for the gate drive and control circuits. The VDD can be directly connected to VIN at voltages up to 5.5V (absolute maximum 6V). This short-circuiting bypasses the LDO regulator and eliminates the LDO differential pressure and power consumption, providing a larger gate drive voltage for the inherent efficiency advantage. RC filters from the input rail to the VIN pin can provide supplementary filtering at the VIN pin. It is worth noting that when VIN is 3V, VDD voltage is 2.8V, DC operating current IVDD is 40mA, MOSFET conduction resistance RDSON will increase at such a low gate drive level, resulting in an increase in conduction loss, and at low VGS operation, switching speed slows down, dead band time will be longer, switching loss will increase. Low gate threshold voltage MOSFETS are recommended for this configuration. The increase of MOSFET junction temperature will also aggravate the increase of on-resistance, so it is necessary to pay attention to the negative temperature coefficient of power MOSFET threshold voltage. However, by virtue of the low sub-regulator dropout voltage, this VDD to VIN connection is not mandatory, thus enabling input ranges from 3 V up to 20 V.

Input and Bias Rail Voltages: VIN and VDD

LGS51403 internal UVLOs ensure that the input rail (VIN) and bias supply rail (VDD) are charged and stable at 2.7V before switching begins. VDD and VIN have independent UVLO comparators, each with 250 mV of hysteresis. Because LGS51403 will not start switching until the internal temperature detection circuit is ready and stable, there is a definite delay between UVLO power-on and switching power on. The delay is four measurement cycles on D+, equivalent to 512 clock cycles. The VDD bias supply LDO has a nominal current limit of 106 mA during normal operation. However, a lower current

Draft Version

limit is engaged at startup to control the rate of rise of the VDD voltage. The figure below shows the typical scope waveforms of VDD and VOUT when the input voltage is instantaneously applied. Here, the VDD voltage ramps in approximately 1.4 ms based on a 10μF VDD decoupling capacitor and current-limited VDD feature.

Output Voltage: FB Voltage and Accuracy

The reference voltage seen at the FB pin is set at 0.6V, and a feedback system accuracy of ±1% over the full junction temperature range is met. Junction temperature range for the device is -40°C to +125°C. While somewhat dependent on frequency and load current levels, LGS51403 is generally capable of providing output voltages in the range of 0.6V to a maximum of greater than 90% VIN. The DC output voltage during normal operation is set by the feedback resistor network, RFB1 and RFB2, connected to VOUT.

Precision Enable: UVLO/EN

The UVLO/EN pin represents a precision analog enable function for user-defined UVLO power-on input voltage levels and to toggle the output on and off. The UVLO/EN pin is essentially a comparator-based input referenced to a flat bandgap voltage with a fixed hysteresis of 165 mV. The UVLO/EN pin has an internal pullup current of 1.8 μA. There is also a low IQ shutdown mode when UVLO/EN is effectively pulled below a base-emitter voltage drop (approximately 0.7V at room temperature). This mode shuts down the bias currents of the LGS51403, but the UVLO/EN pullup current source is still available. If UVLO/EN is pulled below this hard shutdown threshold, the internal LDO regulator powers off and the VDD rail collapses.

When the precision enable threshold of 1.15 V is exceeded, the UVLO/EN pullup current source increases from 1.8 μA to 10.5μA (that is, an 8.7μA hysteresis current). Use this feature to create a customizable UVLO hysteresis (above the standard 165mV fixed voltage hysteresis) based on the resistor divider from VIN to turn on and off LGS51403 at the required input voltage levels. Also, use a capacitor from the UVLO/EN pin to GND to implement a fixed time delay in power systems with timed sequencing requirements.

Given VIN (on) and VIN (off) as the input voltage turn-on and turn-off thresholds, respectively, select the UVLO resistors using the following expressions:

$$R_{UV1} = \frac{VIN_{(on)}\frac{V_{UVLO1}}{V_{UVLO2}} - VIN_{(off)}}{I_{UVLO2} - I_{UVLO1}\frac{V_{UVLO1}}{V_{UVLO2}}}$$

$$R_{UV2} = R_{UV1}\frac{V_{UVLO2}}{VIN_{(on)} - V_{UVLO2} + R_{UV1}I_{UVLO1}}$$

Switching Frequency: F_{SW}

Adjust LGS51403 free-running switching frequency by using a resistor from the FADJ pin to GND. The switching frequency range of the device is from 200 kHz to 1.2 MHz an open circuit at the FADJ pin forces the frequency to the minimum value. FADJ shorted moves the frequency to its maximum value.

The frequency set resistance, R_{FADJ}, is governed by the following equation:

$$R_{FADJ}[k\Omega] = \frac{10000}{F_{SW}[kHZ]^{0.99} - 100} - 7$$

The following table gives resistance settings for common switching frequencies:

Draft Version

SWITCHING FREQUENCY(KHZ)	FREQUENCY SET RESISTANCE(kΩ)
215	95.3
250	68.1
300	47.5
500	20
600	15
800	7.5
1050	4.12
1200	2.87

Clock Synchronization: SYNC

Apply an external clock synchronization signal to LGS51403 to synchronize switching in both frequency and phase. Requirements for the clock SYNC signal are:

• Clock SYNC range: 200 kHz to 1.2 MHz

• SYNC frequency ranges from FADJ frequency: up to 400 kHz (up only)

In applications where the external clock is not applied to LGS51403, use the external FADJ resistor to set the minimum switching frequency. When the external clock is applied, it takes precedence only if the switching frequency is greater than that set by the FADJ resistor. When the external clock is disconnected, LGS51403 switching frequency does not decrease below the minimum frequency set by the resistor. Setting a minimum frequency in this way prevents the inductor ripple current from increasing dramatically. Externally tie SYNC to GND if synchronization functionality is not required.

Temperature Sensing: D+、D-

LGS51403 controller offers low-cost programmable thermal protection by using remote thermal diode temperature measurements based on the change in forward bias voltage of a diode when operated at two different currents. Acting as a thermal diode is a discrete small signal NPN type BJT located near the power inductor.

The ideality factor is a parameter in the diode I-V relationship that approaches 1.0 or 2.0 as carrier diffusion or recombination current dominate current flow, respectively. The ideality factor for 2N3904 type diode-connected BJTs available from several manufacturers is typically 1.004. Note that 3-terminal BJTs such as the 2N3904 are vastly preferred over true 2-terminal diodes in this application. Discrete 2-terminal diodes with current largely dictated by recombination have a much higher ideality factor (η=1.2 to 1.5) than BJTs and, to such an extent, would cause unacceptable temperature measurement error.

Switched capacitor technology is integrated in LGS51403 to sample and measure the base-emitter voltages created by respective 10μA and 100μA bias currents flowing from the D+ to D− pins. The difference in these voltages, termed ΔV_{BE}, is readily extracted and the sensed temperature is calculated noting that ΔV_{BE} is directly proportional to temperature as follows:

$$V_{BE(high)} - V_{BE(low)} = \frac{\eta kT}{q} \ln\left(\frac{I_{high}}{I_{low}}\right)$$

- k = Boltzmann`s constant, 1.3806488 × 10^{-23} J/K
- T = absolute temperature in Kelvin (K)
- q = electron charge ,1.602176 x 10^{-19} C
- η = diode ideality factor ,1.004
- I_{low} = bias current in state 1,10 μA
- I_{high} = bias current in state 2,100 μA

Draft Version

The source currents from the D+ pin during state 1 and state 2 are 10 μA and 100 μA, respectively. The sensed temperature in Kelvin becomes:

$$T = \frac{q\Delta V_{BE}}{\eta k \ln(10)}$$

Thermal Shutdown: OTP

A current proportional to the sensed temperature is sourced from the OTP pin. The resultant voltage at the OTP pin (set by a resistor connected from OTP to GND) is compared to an internal shutdown threshold of 1.15 V with 80-mV hysteresis. When the threshold is exceeded, the device stops switching until the sensed temperature drops to a level where the OTP pin voltage falls to the restart threshold. The external thermal protection is disabled by grounding the OTP pin.

A 100nF capacitor connected in parallel with R_{OTP} is required. When the IC detects an overtemperature event, it responds with the normal hiccup-mode sequence of events when going into shutdown. More specifically, the following steps occur when an internal or external OTP event is detected:

1. The high-side MOSFET immediately turns off.
2. An internal zero-cross circuit is enabled to detect whether the inductor current is positive or negative:
   (a) If the current is negative, the low-side MOSFET immediately turns off.
   (b) If the current is positive, the low-side MOSFET turns off when the inductor current ramps down to zero.

Note that it is important to prevent water-soluble flux residues from contaminating the PCB during the manufacturing process. Contaminants such as these can result in unexpected leakage currents and consequent temperature-measurement errors.

Inductor-DCR-Based Overcurrent Protection

LGS51403 exploits the filter inductor DCR to detect overcurrent events. This technique enables lossless and continuous monitoring of the output current using an RC sense network in parallel with the inductor. DCR current sensing allows the system designer to use inductors specified with low tolerance DCRs to improve the current limit setpoint accuracy. A DC current limit setpoint accuracy within the range of 10% to 15% is easily achieved using inductors with low DCR tolerances.

Current Sensing: CS+ and CS－

As mentioned, LGS51403 implements an inductor DCR lossless current sense scheme designed to provide both accurate overload (current limit) and short-circuit protection. Components RS and CS create a low-pass filter across the inductor to enable differential sensing of the inductor DCR voltage drop. When R_SC_S is equal to L/R_{dcr}, the voltage developed across the sense capacitor, CS, is a replica of the inductor DCR's voltage waveform. Choose the capacitance of CS greater than 0.1 μF to maintain low impedance of the sense network, thus reducing the susceptibility of noise pickup from the switch node. Inductor DCR temperature compensation is automatically provided using the remote-diode sensed temperature. The temperature coefficient of the inductor winding resistance is typically 3720 ppm/℃. The current-limit setpoint is maintained essentially constant over temperature by the slope of CS－ pin current over temperature. An increase in sensed DCR voltage associated with an increase of inductor winding temperature is matched by a concomitant increase in current limit comparator reference voltage. The inductor temperature is measured by placing an external diode-connected 2N3904 discrete NPN transistor , in close proximity to the inductor (see the Temperature Sensing: D+ and D－section for more details).

Current Limit Handling

LGS51403 implements a hiccup mode to allow the device to cool down during overcurrent events. If five overcurrent events are detected during any 32 clock cycle interval, the LGS51403 shuts down and stops switching for a period of 5 ms. During this time, negative inductor current is not allowed, and the output cannot swing negative. After 5 ms, the LGS51403 starts up in the normal startup routine at an output voltage ramp rate determined by the internal soft-start function or the

Draft Version

external soft-start capacitor (if one is used). With each detected current limit event, the high-side MOSFET is turned off and the low-side MOSFET is turned on.

Soft-Start: SS/TRACK

After the UVLO/EN pin exceeds the rising threshold of 1.15 V, the LGS51403 begins charging the output to the dc level dictated by the feedback resistor network. LGS51403 features an adjustable soft-start (set by a capacitor from the SS/TRACK pin to GND) that determines the charging time of the output. A 3 μA current source charges this soft-start capacitor. Soft-start limits inrush current as a result of high output capacitance and avoids an overcurrent condition. Stress on the input supply rail is also reduced. The soft-start time, t_{SS}, for the output voltage to ramp to its nominal level is set by the following Equation:

$$t_{ss} = \frac{C_{SS} V_{REF}}{I_{SS}}$$

If a soft-start capacitor is not used, then LGS51403 defaults to a minimum internal soft-start time of 1.28 ms and provides a resolution of 128 steps. Thus, the internal soft-start dictates the fastest startup time for the circuit. When the SS/TRACK voltage exceeds 91% of the reference voltage, the Power Good flag transitions high. Conversely, the Power Good flag goes low when the SS/TRACK voltage goes below 87% of the reference.

Tracking

The SS/TRACK pin also doubles as a tracking pin when master-slave power supply tracking is required. This tracking is achieved by simply dividing down the master's output voltage with a simple resistor network. If an external voltage source is connected to the SS/TRACK pin, the external soft-start capability of the LGS51403 is effectively disabled (the internal soft-start is still enabled). The regulated output voltage level is reached when the SS/TRACK pin reaches the 0.6 V reference voltage level. It is the responsibility of the system designer to determine if an external soft-start capacitor is required to keep the device from entering current limit during a startup event.

Monotonic Startup

LGS51403 has monotonic startup capability with no dips or flat spots in the output voltage waveform during startup (including pre-biased startup) and fault recovery. During the soft-start interval, FB follows SS/TRACK, and the output voltage linearly increases to the nominal output setpoint. The startup time is determined by the use of an external soft-start capacitor at the SS/TRACK pin charged by an internally generated 3μA constant current source. If a soft-start capacitor is not used, the device automatically enables the internal 7-bit (128 step) digital soft-start. The PGOOD flag transitions high when FB reaches its 91% threshold. As described previously, there is a calibration interval based on four cycles on the D+ pin (that is, 512 clock cycles) that creates a delay from UVLO/EN crossing its precision threshold to SS/TRACK being released.

Voltage-Mode Control

LGS51403 incorporates a voltage-mode control loop implementation with input voltage feedforward to eliminate the input voltage dependence of the PWM modulator gain. This configuration allows the controller to maintain stability throughout the entire input voltage operating range and provides for optimal response to input voltage transient disturbances. The constant gain provided by the controller greatly simplifies feedback loop design because loop characteristics remain constant as the input voltage changes, unlike a buck converter without voltage feedforward. An increase in input voltage is matched by a concomitant increase in ramp voltage amplitude to maintain constant modulator gain.

Output Voltage Remote Sense: RS

High-current switching power supplies typically use output voltage remote sensing to achieve the greatest accuracy at the point of load. Remote ground sensing is implemented in LGS51403 by bringing another amplifier input, designated RS, outside of the device package to act as a kelvin ground sense. This circuit is created by replacing the standard error amplifier used in the PWM loop with a new amplifier that has two pairs of differential inputs. If remote sense is not required, RS is simply shorted to GND.

Draft Version

Power Good: PGOOD

To implement an open-drain power-good function for sequencing and fault detection, use the PGOOD pin of LGS51403. The PGOOD open-drain MOSFET is pulled low during current limit, UVLO, output undervoltage and overvoltage, or if the output is not regulated.

This function can be triggered by multiple events, including the output voltage either exceeding the overvoltage threshold (117% VREF) or decreasing below the undervoltage threshold (91% VREF), heavy overcurrent, soft-start voltage (both internal and external) below 91% VREF, UVLO, thermal shutdown, enable delay, or disabled state.

To prevent momentary glitches to the PGOOD pin, a 20μs deglitch filter is built into LGS51403 to prevent multiple triggering of the flag. Note that the primary objective of PGOOD is to signal to the system that the soft-start period has expired and the output voltage is in regulation for loads within the rated limit. This can be used for sequencing downstream regulators.

Gate Drivers: LG and HG

LGS51403 gate driver impedances are low enough to perform effectively in high output current applications where large die-size or paralleled MOSFETs with correspondingly large gate charge. Measured at VDD = 4.5V, LGS51403's low-side driver has a low impedance pull-down path of 0.9Ω to minimize the effect of dv/dt induced turn-on, particularly with low gate-threshold voltage MOSFETs. Similarly, the high-side driver has 1.5Ω and 1.0Ω pull-up and pull-down impedances, respectively, for faster switching transition times, lower switching loss, and greater efficiency. Furthermore, there is a proprietary adaptive deadtime control on both switching edges to prevent shoot-through and cross-conduction, minimize body diode conduction time, and reduce body diode reverse recovery related losses.

Sink and Source Capability

Even though an LGS51403 based DC/DC regulator is capable of sinking and sourcing current, the inductor DCR-based overcurrent protection operates only with positive currents. Negative currents are detected through the low-side MOSFET only when the device is in an overvoltage condition. Pre-bias startup still operates normally.

PCB Layout Reference

Figure 3 provides a reference PCB drawing for LGS51403 applications. For more information about recommended application solutions, refer to the LGS51403 EVM Board user manual.

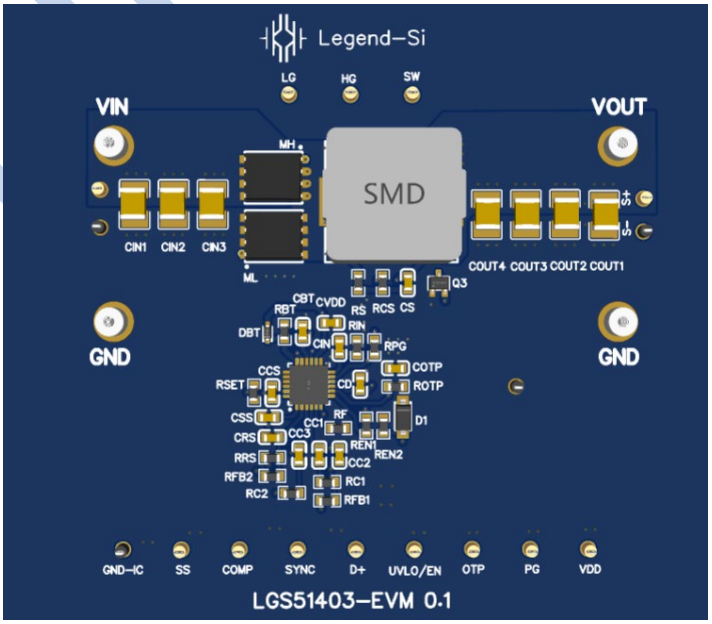
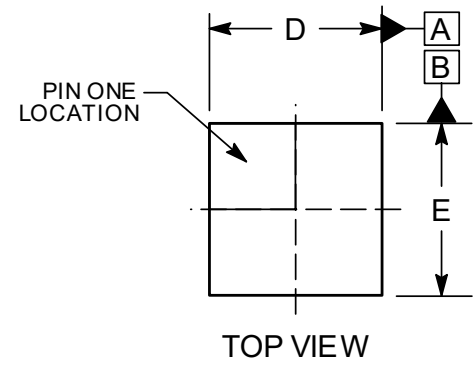


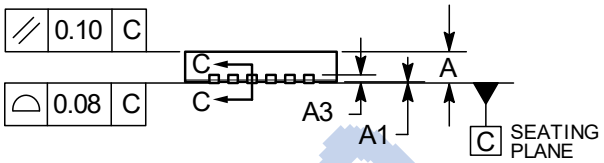
Figure 4 PCB Layout Reference

Draft Version

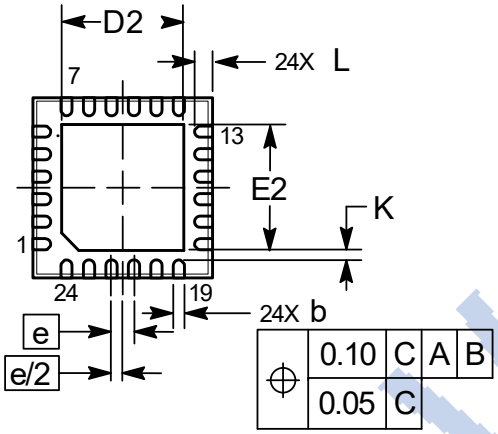
Description of Package



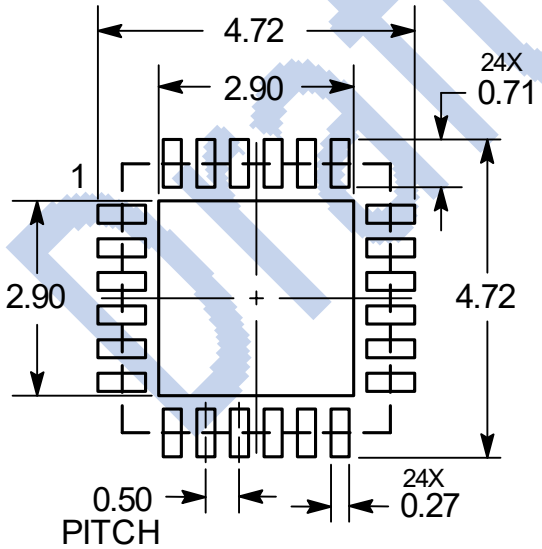
TOP VIEW



SIDE VIEW



BOTTOM VIEW



DIMENSIONS: MILLIMETERS

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	--	--	0.05
A3	0.20 REF		
A4	0.10	--	--
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
e	0.50 BSC		
K	0.20	--	--
L	0.35	0.40	0.45
L3	0.00	0.05	0.10

NOTE:

(1) Alllinear dimensions are in millimeters. Any dimensions in parentheses are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

(2) This drawing is subject to change without notice.

(3) This dimension does not include the burrs of the moulds. The burrs or protrusions on each side of the moulds shall not exceed 0.25 mm.

RECOMMENDED
SOLDERING FOOTPRINT

Draft Version

IMPORTANT NOTICE AND DISCLAIMER

and Legend- si are trademarks of Legend- Si Semiconductor Co., Ltd.

Legend- si holds a number of patents, trademarks, trade secrets and other intellectual property rights. Legend-Si provides technical and reliability data (including datasheets), design resources (including reference designs), applications or other design recommendations, networking tools, safety information and other resources "as is". No warranty is made that it is free from any defect, and no warranty, express or implied, is made, including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose or infringement of any third party's intellectual property rights.

The resources are available for professional developers to design with the Legend-Si product. You are solely responsible for: (1) selecting the appropriate Legend-Si product for your application; (2) Design, validate and test your application; (3) Ensure that your application meets relevant standards and any other safety, security or other requirements. Resources are subject to change without notice. Legend- Si's license for your use of the Resources is limited to applications related to the Legend- Si products involved in the development of the resources. Otherwise, no copying or display of the resources is permitted, and no other Legend- Si or any third-party intellectual property licenses are provided. Legend- Si will not be liable for any claims, damages, costs, losses or liabilities arising out of the use of the Resources and you shall indemnify Legend-si and its representatives for damages arising therefrom.

The Products provided by Legend- Si are subject to the Terms of Sale of Legend- Si and other applicable terms provided by Legend- Si Products on or with www.Legend-si.com. The provision of the resources by Legend- Si does not extend or otherwise change the applicable warranty coverage or warranty disclaimer issued by Legend- Si with respect to the Legend- Si Products.

Mailing address: Rm 1403, Tengfei Suite C Bldg., No.88 jiangmiao Rd., Pukou Dist., Nanjing, Jiangsu Prov.
Telephone: 025-58196091

Copyright © 2022- present Legend- Si (Nanjing) Semiconductor Co., Ltd.

Draft Version