ADC356x 16 位 0.5MSPS 至 65MSPS 低噪声、低功耗 ADC

1 特性

- 16 位、10MSPS 至 65MSPS ADC
- 本底噪声：-158dBFS/Hz
- 低功耗：
  77 mW (10 MSPS) 至 122 mW (65 MSPS)
- 延迟：1 个时钟周期（1 线 SLVDS）
- 指定的 16 位，无丢码
- INL：±3LSB；DNL：±0.7LSB
- 基准：外部或内部
- 输入带宽：900MHz (3dB)
- 工业温度范围：-40°C 至 +105°C
- 片上双频带数字滤波器（可选）
  - 2 倍、4 倍、8 倍、16 倍、32 倍抽取率
  - 32 位 NCO
- 串行 LVDS 数字接口（2 线、1 线和 1/2 线）
- 小尺寸: 40 引脚 WQFN (5mm × 5mm) 封装
- 频谱性能 (f_{IN} = 10MHz)：
  - SNR：81.9dBFS
  - SFDR：95dBc HD2、HD3
  - SFDR：100dBFS 最严重毛刺

2 应用

- 高速数据采集
- 工业监控
- 软件定义无线电
- 电能质量分析仪
- 源测量单元 (SMU)
- 通信基础设施
- 频谱分析仪
- 控制环路
- 仪表
- 成像
- 光谱分析
- 雷达
- 声纳

3 说明

ADC3561、ADC3562、ADC3563 (ADC356x) 系列器件是低噪声、超低功耗、16 位、10MSPS 至 65MSPS 高速模数转换器 (ADC)。这些器件可实现低功耗，噪声频谱密度为 –158dBFS/Hz，并提供出色的线性度和动态范围。ADC356x 器件可提供出色的直流精度以及中频采样支持，因此非常适合各种应用。高速控制环路受益于只有一个时钟的低延迟。该 ADC 在 65MSPS 下的功耗仅为 122mW，功耗随采样率减小而迅速降低。

ADC356x 使用串行 LVDS (SLVDS) 接口输出数据，可更大限度减少数字互连的次数。该器件提供双通道、单通道和半通道选项。ADC356x 和 ADC358x 属于引脚对引脚兼容系列，具有 16 位和 18 位分辨率和不同的速度等级。这些器件采用 40 引脚 QFN 封装 (5mm × 5mm)，支持 –40°C 至 +105ºC 的工业级工作温度范围。

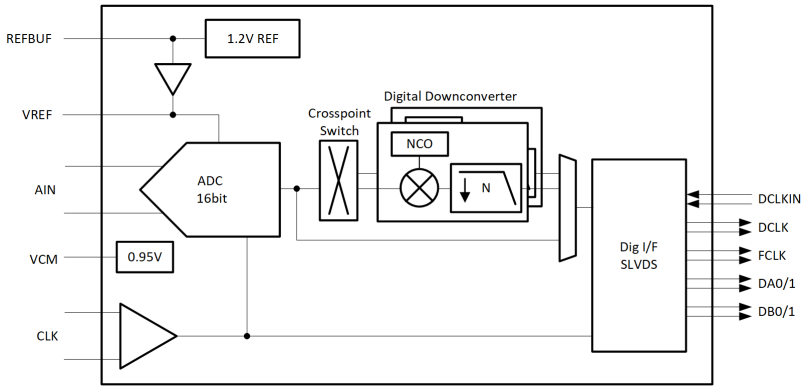
封装信息

器件型号	封装(1)	封装尺寸（标称值）
ADC356x	WQFN (40)	5.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

表 3-1. 器件比较

器件型号	分辨率	采样率
ADC3563	16 位	65MSPS
ADC3562	16 位	25MSPS
ADC3561	16 位	10MSPS



简化版方框图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (October 2022) to Revision B (October 2022)	Page
• 为 ADC3561 (10MSPS) 下的增益误差添加了缺少的典型值 0.43% FSR	7

Changes from Revision * (February 2021) to Revision A (October 2022)	Page
• 删除了*器件比较*表中器件型号 ADC3561 和 ADC3562 的“产品预发布”说明	1
• Corrected pin numbers for DB0P/M, DB1P/M, IOVDD and IOGND	3
• Added the Typical Characteristics - ADC3561 graphs	14
• Added the Typical Characteristics - ADC3562 graphs	17
• Added GND symbol to REFGND pin for all voltage reference option diagrams	37
• Added the section Output Bit Mapper	50

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5 Pin Configuration and Functions

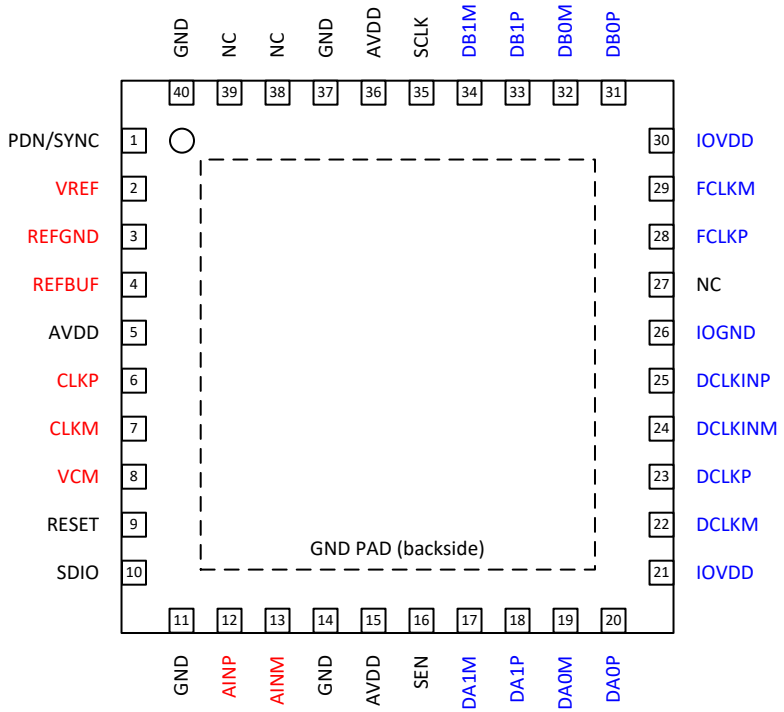

图 5-1. RSB (WQFN) Package, 40-Pin (Top View)

表 5-1. Pin Descriptions

PIN		TYPE	DESCRIPTION
NAME	NO.		
INPUT/REFERENCE			
AINP	12	I	Positive analog input
AINM	13	I	Negative analog input
VCM	8	O	Common-mode voltage output for the analog inputs, 0.95 V
VREF	2	I	External voltage reference input, 1.6 V
REFBUF	4	I	1.2V external voltage reference input for use with internal reference buffer
REFGND	3	I	Reference ground input, 0 V
CLOCK			
CLKM	7	I	Negative differential sampling clock input for the ADC
CLKP	6	I	Positive differential sampling clock input for the ADC
CONFIGURATION			
PDN/SYNC	1	I	Power down/Synchronization input. This pin can be configured via the SPI interface. Active high. This pin has an internal 21 kΩ pull-down resistor.
RESET	9	I	Hardware reset. Active high. This pin has an internal 21 kΩ pull-down resistor.
SEN	16	I	Serial interface enable. Active low. This pin has an internal 21 kΩ pull-up resistor to AVDD.

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表 5-1. Pin Descriptions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
SCLK	35	I	Serial interface clock input. This pin has an internal 21 kΩ pull-down resistor.
SDIO	10	I	Serial interface data input and output. This pin has an internal 21 kΩ pull-down resistor.
NC	27,38,39	-	Do not connect
DIGITAL INTERFACE			
DA0P	20	O	Positive differential serial LVDS output for lane 0, channel A
DA0M	19	O	Negative differential serial LVDS output for lane 0, channel A
DA1P	18	O	Positive differential serial LVDS output for lane 1, channel A
DA1M	17	O	Negative differential serial LVDS output for lane 1, channel A
DB0P	31	O	Positive differential serial LVDS output for lane 0, channel B. Used only in dual band complex decimation. Default is powered down.
DB0M	32	O	Negative differential serial LVDS output for lane 0, channel B. Used only in dual band complex decimation. Default is powered down.
DB1P	33	O	Positive differential serial LVDS output for lane 1, channel B. Used only in dual band complex decimation. Default is powered down.
DB1M	34	O	Negative differential serial LVDS output for lane 1, channel B. Used only in dual band complex decimation. Default is powered down.
DCLKP	23	O	Positive differential serial LVDS bit clock output.
DCLKM	22	O	Negative differential serial LVDS bit clock output.
FCLKP	28	O	Positive differential serial LVDS frame clock output.
FCLKM	29	O	Negative differential serial LVDS frame clock output.
DCLKINP	25	I	Positive differential serial LVDS bit clock input.
DCLKINM	24	I	Negative differential serial LVDS bit clock input.
POWER SUPPLY			
AVDD	5,15,36	I	Analog 1.8-V power supply
GND	11,14,37,40, PowerPad	I	Ground, 0 V
IOGND	26	I	Ground, 0 V for digital interface
IOVDD	21,30	I	1.8-V power supply for digital interface

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6 Specifications

6.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

参数	测试条件	最小值	最大值	单位
电源电压范围，AVDD，IOVDD		-0.3	2.1	V
电源电压范围，GND，IOGND，REFGND		-0.3	0.3	V
施加到输入引脚的电压	AINP/M、CLKP/M、VREF、REFBUF	-0.3	最小值（2.1，AVDD+0.3）	V
	PDN/SYNC、RESET、SCLK、SEN、SDIO	-0.3	最小值（2.1，AVDD+0.3）	
	DCLKINP/M	-0.3	最小值（2.1，IOVDD+0.3）	
结温，T_J			105	℃
贮存温度，T_{stg}		-65	150	°C

(1) 应力超出*绝对最大额定值*下所列的值可能会对器件造成永久损坏。这些列出的值仅仅是应力额定值，这并不表示器件在这些条件下以及在*建议运行条件*以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。

6.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001，所有引脚(1)	2500	V
		充电器件模式（CDM），符合 JEDEC 规范 JESD22-C101，所有引脚(2)	1000	

(1) JEDEC 文件 JEP155 指出：500V HBM 可实现在标准 ESD 控制流程下安全生产。
(2) JEDEC 文件 JEP157 指出：250V CDM 可实现在标准 ESD 控制流程下安全生产。

6.3 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）

		最小值	标称值	最大值	单位
电源电压范围	AVDD(1)	1.75	1.8	1.85	V
	IOVDD(1)	1.75	1.8	1.85	V
T_A	自然通风工作温度	-40		105	°C
T_J	工作结温			105(2)	°C

(1) 接地测量。
(2) 长时间高于此结温使用可能会增加器件的时基故障率。

6.4 热性能信息

热指标(1)		ADC356x RSB (QFN) 40 引脚	单位
$R_{\Theta JA}$	结至环境热阻	30.7	°C/W
$R_{\Theta JC(top)}$	结至外壳（顶部）热阻	16.4	°C/W
$R_{\Theta JB}$	结至电路板热阻	10.5	°C/W
Ψ_{JT}	结至顶部特征参数	0.2	°C/W
Ψ_{JB}	结至电路板特征参数	10.5	°C/W
$R_{\Theta JC(bot)}$	结至外壳（底部）热阻	2.0	°C/W

(1) 有关新旧热指标的更多信息，请参阅*《半导体和 IC 封装热指标》*应用报告，SPRA953。

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6.5 电气特性 - 功耗

在自然通风条件下的工作温度范围内（T_A = 25°C，整个温度范围为 T_{MIN} = –40°C 至 T_{MAX} = 105°C）的典型值：ADC 采样率 = 65MSPS，50% 时钟占空比，AVDD = IOVDD = 1.8V，外部 1.6V 基准电压，–1dBFS 差分输入，除非另有说明

参数		测试条件	最小值	典型值	最大值	单位
ADC3561：10MSPS						
I_{AVDD}	模拟电源电流	外部基准		18	27	mA
I_{IOVDD}	I/O 电源电流	SLVDS 1 线		25	43	mA
P_{DIS}	功率耗散	外部基准，SLVDS 1 线		77	126	mW
I_{IOVDD}	I/O 电源电流	1 线，1/2 摆幅		19		mA
		2 线		29		
		4 倍实时抽取率，1 线		26		
ADC3562：25MSPS						
I_{AVDD}	模拟电源电流	外部基准		20	27	mA
I_{IOVDD}	I/O 电源电流	单线		27	43	mA
P_{DIS}	功率耗散	外部基准，1 线		85	126	mW
I_{IOVDD}	I/O 电源电流	1 线，1/2 摆幅		21		mA
		2 线		30		
		4 倍实时抽取率，1 线		29		
ADC3563：65MSPS						
I_{AVDD}	模拟电源电流	外部基准		40	51	mA
I_{IOVDD}	I/O 电源电流	2 线		28	43	mA
P_{DIS}	功率耗散	外部基准，2 线		123	169	mW
I_{IOVDD}	I/O 电源电流	2 线，1/2 摆幅		21		mA
		4 倍实时抽取率，1 线		27		
		16 倍实时抽取率，1 线		25		
		4 倍复杂抽取率，1 线		33		
		16 倍复杂抽取率，1 线		28		
其他						
I_{AVDD}	内部基准，额外模拟电源电流			1		mA
	外部 1.2V 基准 (REFBUF)，额外模拟电源电流			0.3		
	单端时钟输入，将模拟电源电流减少	通过 SPI 启用		0.7		
P_{DIS}	全局断电模式下的功耗	默认掩码设置，内部基准		5		mW
		默认掩码设置，外部基准		9		

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6.6 电气特征 - 直流规格

在自然通风条件下的工作温度范围内（T_A = 25°C，整个温度范围为 T_{MIN} = –40°C 至 T_{MAX} = 105°C）的典型值：ADC 采样率 = 65MSPS，50% 时钟占空比，AVDD = IOVDD = 1.8V，外部 1.6V 基准电压，–1dBFS 差分输入，除非另有说明

参数		测试条件	最小值	典型值	最大值	单位
直流精度						
无丢码			16			位
PSRR		F_{IN} = 1MHz		50		dB
ADC3561 - 10MSPS：直流精度						
DNL	微分非线性	F_{IN} = 4.9 MHz		± 0.4	± 0.85	LSB
INL	积分非线性	F_{IN} = 4.9 MHz		± 3	± 5	LSB
V_{OS_ERR}	失调电压误差			32	135	LSB
V_{OS_DRIFT}	不同温度下的温漂			-0.004		LSB/°C
增益$_{误差}$	增益误差	外部 1.6V 基准		0.43		%FSR
增益$_{漂移}$	不同温度下的增益漂移	外部 1.6V 基准		0.85		ppm/°C
增益$_{误差}$	增益误差	内部基准		-1.15		%FSR
增益$_{漂移}$	不同温度下的增益漂移	内部基准		90		ppm/°C
切换噪声	切换噪声			1.3		LSB
ADC3562 - 25MSPS：直流精度						
DNL	微分非线性	F_{IN} = 5MHz		± 0.4	± 0.85	LSB
INL	积分非线性	F_{IN} = 5MHz		± 3	± 5	LSB
V_{OS_ERR}	失调电压误差			32	± 135	LSB
V_{OS_DRIFT}	不同温度下的温漂			0.009		LSB/°C
增益$_{误差}$	增益误差	外部 1.6V 基准		-0.25		%FSR
增益$_{漂移}$	不同温度下的增益漂移	外部 1.6V 基准		0.08		ppm/°C
增益$_{误差}$	增益误差	内部基准		-1.9		%FSR
增益$_{漂移}$	不同温度下的增益漂移	内部基准		86		ppm/°C
切换噪声				1.3		LSB
ADC3563 - 65MSPS：直流精度						
DNL	微分非线性	F_{IN} = 5MHz		± 0.7	± 0.85	LSB
INL	积分非线性	F_{IN} = 5MHz		± 3	± 5	LSB
V_{OS_ERR}	失调电压误差			± 33	± 135	LSB
V_{OS_DRIFT}	不同温度下的温漂			0.05		LSB/°C
增益$_{误差}$	增益误差	外部 1.6V 基准		± 2.3		%FSR
增益$_{漂移}$	不同温度下的增益漂移	外部 1.6V 基准		68		ppm/°C
增益$_{误差}$	增益误差	内部基准		± 3.5		%FSR
增益$_{漂移}$	不同温度下的增益漂移	内部基准		242		ppm/°C
切换噪声				1.3		LSB

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6.6 电气特征 - 直流规格 (continued)

在自然通风条件下的工作温度范围内（T_A = 25°C，整个温度范围为 T_{MIN} = –40°C 至 T_{MAX} = 105°C）的典型值：ADC 采样率 = 65MSPS，50% 时钟占空比，AVDD = IOVDD = 1.8V，外部 1.6V 基准电压，–1dBFS 差分输入，除非另有说明

参数		测试条件	最小值	典型值	最大值	单位
ADC 模拟输入（AINP/M）						
FS	满量程输入	差分电压		3.2		Vpp
V_{CM}	输入共模电压		0.9	0.95	1.0	V
R_{IN}	差分输入电阻	F_{IN} = 100kHz		8		kΩ
C_{IN}	差分输入电容	F_{IN} = 100kHz		7		pF
V_{OCM}	输出共模电压			0.95		V
BW	模拟输入带宽 (-3dB)			900		MHz
内部电压基准						
V_{REF}	内部基准电压			1.6		V
V_{REF} 输出阻抗				8		Ω
外部基准电压				1.2		V
参考输入缓冲器 (REFBUF)						
V_{REF}				1.6		V
输入电流				0.3		mA
输入阻抗				5.3		kΩ
外部电压基准 (VREF)						
输入时钟频率	输入时钟频率		0.5		65	MHz
V_{ID}		差分输入电压		1	3.6	Vpp
V_{CM}		输入共模电压		0.9		V
时钟输入 (CLKP/M)						
R_{IN}				5		kΩ
C_{IN}	单端输入电容			1.5		pF
时钟占空比	时钟占空比		40	50	60	%
数字输入（RESET、PDN、SCLK、SEN、SDIO）						
V_{IH}	高电平输入电压		1.4			V
V_{IL}	低电平输入电压				0.4	V
I_{IH}	高电平输入电流			90	150	uA
I_{IL}	低电平输入电流		-150	-90		uA
C_I	输入电容			1.5		pF
V_{OH}	高电平输出电压		IOVDD – 0.1	IOVDD		V
数字输出 (SDOUT)						
V_{OL}	低电平输出电压	I_{LOAD} = 400uA			0.1	V
每个 CMOS 输出引脚	每个 CMOS 输出引脚	每个差分 SLVDS 输出对			1000	Mbps
SLVDS 接口						
V_{ID}	差分输入电压	DCLKIN	200	350	650	mVpp
V_{CM}	输入共模电压	DCLKIN	1	1.2	1.3	V
V_{OD}	差分输出电压		500	700	850	mVpp
V_{CM}	输出共模电压			1.0		V

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6.7 电气特征 - 交流规格

在自然通风条件下的工作温度范围内（T_A = 25°C，整个温度范围为 T_{MIN} = –40°C 至 T_{MAX} = 105°C）的典型值：ADC 采样率 = 10MSPS 至 65MSPS，50% 时钟占空比，AVDD = IOVDD = 1.8V，外部 1.6V 基准电压，–1dBFS 差分输入，除非另有说明

参数		测试条件	最小值	典型值	最大值	单位
ADC3561：10MSPS						
NSD	噪声频谱密度	无输入信号		-150.0		dBFS/Hz
SNR	信噪比	f_{IN} = 1.1MHz		82.0		dBFS
		f_{IN} = 4.9 MHz	80.5	82.0		
		f_{IN} = 9.9 MHz		81.9		
SINAD	信噪比和失真比	f_{IN} = 1.1MHz		81.9		dBFS
		f_{IN} = 4.9 MHz	80.0	81.9		
		f_{IN} = 9.9 MHz		81.8		
ENOB	有效位数	f_{IN} = 1.1MHz		13.3		位
		f_{IN} = 4.9 MHz	13.0	13.3		
		f_{IN} = 9.9 MHz		13.3		
THD	总谐波失真（前五个谐波）	f_{IN} = 1.1MHz		86		dBc
		f_{IN} = 4.9 MHz	81	86		
		f_{IN} = 9.9 MHz		95		
SFDR	无杂散动态范围，包括第二和第三个谐波失真	f_{IN} = 1.1MHz		86		dBc
		f_{IN} = 4.9 MHz	81	86		
		f_{IN} = 9.9 MHz		94		
非 HD2,3	无杂散动态范围（不包括 HD2 和 HD3）	f_{IN} = 1.1MHz		100		dBFS
		f_{IN} = 4.9 MHz	92	100		
		f_{IN} = 9.9 MHz		102		
IMD3	双音互调失真	f_1 = 3MHz，f_2 = 4MHz，A_{IN} = -7dBFS/音调		88		dBc
		f_1 = 10MHz，f_2 = 12MHz，A_{IN} = -7dBFS/音调		90		

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6.7 电气特征 - 交流规格 (continued)

在自然通风条件下的工作温度范围内（T_A = 25°C，整个温度范围为 T_{MIN} = –40°C 至 T_{MAX} = 105°C）的典型值：ADC 采样率 = 10MSPS 至 65MSPS，50% 时钟占空比，AVDD = IOVDD = 1.8V，外部 1.6V 基准电压，–1dBFS 差分输入，除非另有说明

参数		测试条件	最小值	典型值	最大值	单位
ADC3562：25MSPS						
NSD	噪声频谱密度	无输入信号		-154.0		dBFS/Hz
SNR	信噪比	f_{IN} = 1.1MHz		82.0		dBFS
		f_{IN} = 5MHz	80.5	82.0		
		f_{IN} = 10MHz		81.9		
		f_{IN} = 20MHz		81.6		
		f_{IN} = 40MHz		78.6		
SINAD	信噪比和失真比	f_{IN} = 1.1MHz		81.9		dBFS
		f_{IN} = 5MHz	80.0	81.9		
		f_{IN} = 10MHz		81.9		
		f_{IN} = 20MHz		81.5		
		f_{IN} = 40MHz		78.5		
ENOB	有效位数	f_{IN} = 1.1MHz		13.3		位
		f_{IN} = 5MHz	13.0	13.3		
		f_{IN} = 10MHz		13.3		
		f_{IN} = 20MHz		13.2		
		f_{IN} = 40MHz		12.7		
THD	总谐波失真（前五个谐波）	f_{IN} = 1.1MHz		85		dBc
		f_{IN} = 5MHz	81	89		
		f_{IN} = 10MHz		88		
		f_{IN} = 20MHz		83		
		f_{IN} = 40MHz		85		
SFDR	无杂散动态范围，包括第二和第三个谐波失真	f_{IN} = 1.1MHz		86		dBc
		f_{IN} = 5MHz	81	90		
		f_{IN} = 10MHz		89		
		f_{IN} = 20MHz		83		
		f_{IN} = 40MHz		86		
非 HD2,3	无杂散动态范围（不包括 HD2 和 HD3）	f_{IN} = 1.1MHz		101		dBFS
		f_{IN} = 5MHz	92	101		
		f_{IN} = 10MHz		100		
		f_{IN} = 20MHz		99		
		f_{IN} = 40MHz		94		
IMD3	双音互调失真	f_1 = 3MHz，f_2 = 4MHz，A_{IN} = -7dBFS/音调		84		dBc
		f_1 = 10MHz，f_2 = 12MHz，A_{IN} = -7dBFS/音调		86		

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6.7 电气特征 - 交流规格 (continued)

在自然通风条件下的工作温度范围内（T_A = 25°C，整个温度范围为 T_{MIN} = –40°C 至 T_{MAX} = 105°C）的典型值：ADC 采样率 = 10MSPS 至 65MSPS，50% 时钟占空比，AVDD = IOVDD = 1.8V，外部 1.6V 基准电压，–1dBFS 差分输入，除非另有说明

参数		测试条件	最小值	典型值	最大值	单位
ADC3563：65MSPS						
NSD	噪声频谱密度	无输入信号		-158.0		dBFS/Hz
SNR	信噪比	f_{IN} = 1.1MHz		82.0		dBFS
		f_{IN} = 5MHz	80.0	82.0		
		f_{IN} = 10MHz		81.9		
		f_{IN} = 20MHz		81.6		
		f_{IN} = 40MHz		80.5		
		f_{IN} = 70MHz		77.0		
SINAD	信噪比和失真比	f_{IN} = 1.1MHz		80.2		dBFS
		f_{IN} = 5MHz		80.2		
		f_{IN} = 10MHz		80.2		
		f_{IN} = 20MHz		80.0		
		f_{IN} = 40MHz		78.5		
		f_{IN} = 70MHz		75.5		
ENOB	有效位数	f_{IN} = 1.1MHz		13.0		位
		f_{IN} = 5MHz		13.0		
		f_{IN} = 10MHz		13.0		
		f_{IN} = 20MHz		13.0		
		f_{IN} = 40MHz		12.8		
		f_{IN} = 70MHz		12.3		
THD	总谐波失真（前五个谐波）	f_{IN} = 1.1MHz		81		dBc
		f_{IN} = 5MHz	81	89		
		f_{IN} = 10MHz		87		
		f_{IN} = 20MHz		82		
		f_{IN} = 40MHz		82		
		f_{IN} = 70MHz		81		
SFDR	无杂散动态范围，包括第二和第三个谐波失真	f_{IN} = 1.1MHz		82		dBc
		f_{IN} = 5MHz	82	90		
		f_{IN} = 10MHz		90		
		f_{IN} = 20MHz		83		
		f_{IN} = 40MHz		84		
		f_{IN} = 70MHz		83		
非 HD2,3	无杂散动态范围（不包括 HD2 和 HD3）	f_{IN} = 1.1MHz		100		dBFS
		f_{IN} = 5MHz	91	100		
		f_{IN} = 10MHz		98		
		f_{IN} = 20MHz		97		
		f_{IN} = 40MHz		92		
		f_{IN} = 70MHz		86		
IMD3	双音互调失真	f_1 = 1MHz，f_2 = 2MHz，A_{IN} = -7dBFS/音调		97		dBc
		f_1 = 10MHz，f_2 = 12MHz，A_{IN} = -7dBFS/音调		96		

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6.8 时序要求

在自然通风条件下的工作温度范围内（T_A = 25°C，整个温度范围为 T_{MIN} = –40°C 至 T_{MAX} = 105°C）的典型值：ADC 采样率 = 65MSPS，50% 时钟占空比，AVDD = IOVDD = 1.8V，外部 1.6V 基准电压，–1dBFS 差分输入，除非另有说明

参数		测试条件	最小值	标称值	最大值	单位
ADC 时序规格						
t_{AD}	孔径延迟			0.85		ns
t_A	孔径抖动	具有快速边缘的方波时钟		180		fs
t_J	DCLKIN 上的抖动				± 50	ps
t_{ACQ}	信号采集周期，以采样时钟下降沿为基准	F_S = 65Msps		$-T_S/4$		采样时钟周期
		F_S = 25Msps		$-T_S/2$		
		F_S = 10Msps		$-T_S/2$		
t_{CONV}	信号转换周期，以采样时钟下降沿为基准	F_S = 65Msps		$+T_S \times 5/8$		采样时钟周期
		F_S = 25Msps		$+T_S \times 3/8$		
		F_S = 10Msps		$+T_S \times 1/5$		
唤醒时间	断电后的数据有效时间。内部基准。	已启用带隙基准，单端时钟			17.6	us
		已启用带隙基准，差分时钟			12.9	
		已禁用带隙基准，单端时钟			2.2	ms
		已禁用带隙基准，差分时钟			2.2	
	断电后的数据有效时间。外部 1.6V 基准。	已启用带隙基准，单端时钟			15.9	us
		已启用带隙基准，差分时钟			12.9	
		已禁用带隙基准，单端时钟			1.7	ms
		已禁用带隙基准，差分时钟			1.7	
$t_{S\ ,\ SYNC}$	SYNC 输入信号的设置时间	以采样时钟上升沿为基准	500			ps
$t_{H\ ,\ SYNC}$	SYNC 输入信号的保持时间		600			
ADC 延迟	信号输入到数据输出	2 线 SLVDS		2		时钟周期
		1 线 SLVDS		1		
		1/2 线 SLVDS		1		
添加。延迟	2 倍实时抽取率			21		输出时钟周期
	2 倍复杂抽取率			22		
	4 倍、8 倍、16 倍、32 倍实时或复杂抽取率			23		
接口时序：串行低压差分信号 (LVDS) 接口						
t_{PD}	传播延迟：采样时钟下降沿到 DCLK 上升沿	采样时钟下降沿到 DCLKIN 上升沿的延迟小于 2.5ns。 T_{DCLK} = DCLK 周期 t_{CDCLK} = 采样时钟下降沿到 DCLKIN 下降沿	$2 + T_{DCLK} + t_{CDCLK}$	$3 + T_{DCLK} + t_{CDCLK}$	$4 + T_{DCLK} + t_{CDCLK}$	ns
		采样时钟下降沿到 DCLKIN 上升沿的延迟大于或等于 2.5ns。 T_{DCLK} = DCLK 周期 t_{CDCLK} = 采样时钟下降沿到 DCLKIN 下降沿	$2 + t_{CDCLK}$	$3 + t_{CDCLK}$	$4 + t_{CDCLK}$	

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6.8 时序要求 (continued)

在自然通风条件下的工作温度范围内（T_A = 25°C，整个温度范围为 T_{MIN} = –40°C 至 T_{MAX} = 105°C）的典型值：ADC 采样率 = 65MSPS，50% 时钟占空比，AVDD = IOVDD = 1.8V，外部 1.6V 基准电压，–1dBFS 差分输入，除非另有说明

参数		测试条件	最小值	标称值	最大值	单位
t_{CD}	DCLK 上升沿到输出数据延迟，2 线 SLVDS	Fout = 10MSPS，DA/B0,1 = 80MBPS	0.0	0.1		ns
		Fout = 25MSPS，DA/B0,1 = 200MBPS	0.0	0.1		
		Fout = 65MSPS，DA/B0,1 = 520MBPS	0.0	0.1		
	DCLK 上升沿到输出数据延迟，1 线 SLVDS	Fout = 10MSPS，DA/B0 = 160MBPS	0.0	0.1		
		Fout = 25MSPS，DA/B0 = 400MBPS	0.0	0.1		
		Fout = 62.5MSPS，DA/B0 = 1000MBPS	-0.6	0.1		
	DCLK 上升沿到输出数据延迟，1/2 线 SLVDS	Fout = 5MSPS，DA0 = 160MBPS	0.0	0.1		
		Fout = 10MSPS，DA0 = 320MBPS	0.0	0.1		
		Fout = 25MSPS，DA0 = 800MBPS	0.0	0.1		
t_{DV}	数据有效，2 线 SLVDS	Fout = 10MSPS，DA/B0,1 = 80MBPS	11.9	12.1		ns
		Fout = 25MSPS，DA/B0,1 = 200MBPS	4.5	4.6		
		Fout = 65MSPS，DA/B0,1 = 520MBPS	1.4	1.5		
	数据有效，1 线 SLVDS	Fout = 10MSPS，DA/B0 = 160MBPS	5.7	5.8		
		Fout = 25MSPS，DA/B0 = 400MBPS	2.0	2.1		
		Fout = 62.5MSPS，DA/B0 = 1000MBPS	0.5	0.6		
	数据有效，1/2 线 SLVDS	Fout = 5MSPS，DA0 = 160MBPS	5.7	5.8		
		Fout = 10MSPS，DA0 = 320MBPS	2.7	2.8		
		Fout = 25MSPS，DA0 = 800MBPS	0.8	0.9		
串行编程接口（SCLK、SEN、SDIO）- 输入						
$f_{CLK(SCLK)}$	串行时钟频率				20	MHz
$t_{SU(SEN)}$	SEN 到 SCLK 的上升沿		10			ns
$t_{H(SEN)}$	通过 SCLK 上升沿进行 SEN		9			ns
$t_{SU(SDIO)}$	SDIO 到 SCLK 的上升沿		17			ns
$t_{H(SDIO)}$	通过 SCLK 上升沿进行 SDIO		9			ns
串行编程接口 (SDIO) - 输出						
$t_{(OZD)}$	SDIO 三态到被驱动		3.9		10.8	ns
$t_{(ODZ)}$	SDIO 数据到三态		3.4		14	ns
$t_{(OD)}$	从 SCLK 的下降沿到 SDIO 有效		3.9		10.8	ns

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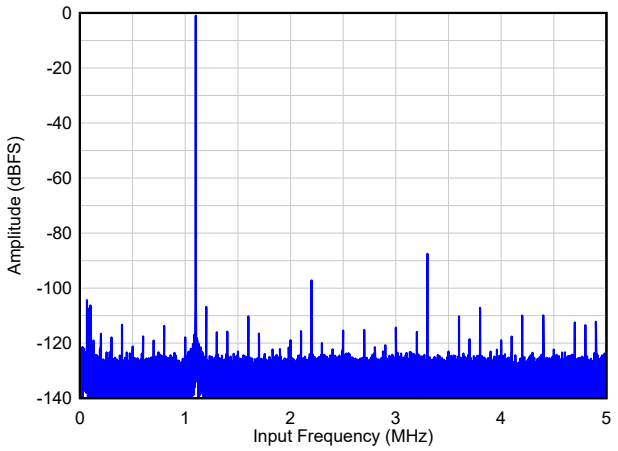
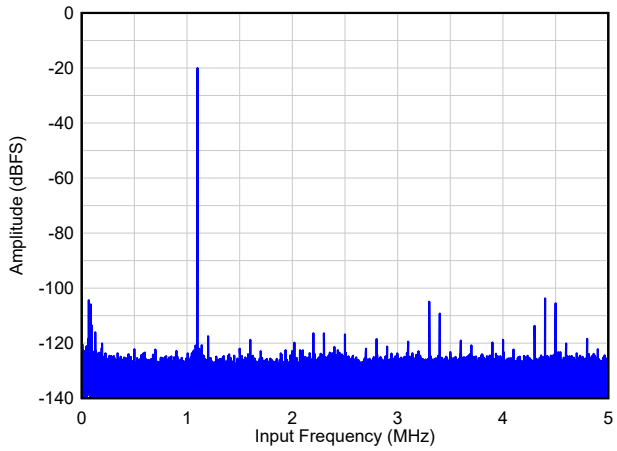
6.9 Typical Characteristics - ADC3561

Typical values at T_A = 25 °C, ADC sampling rate = 10 MSPS, A_{IN} = – 1 dBFS differential input, AVDD = IOVDD = 1.8 V, external 1.6 V voltage reference, unless otherwise noted.



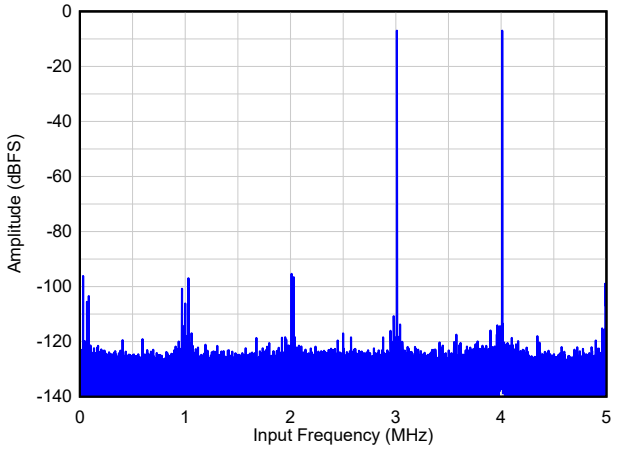
SNR = 82.1 dBFS, SFDR = 87 dBc, Non HD23 = 102 dBFS

图 6-1. Single Tone FFT at F_{IN} = 1.1 MHz



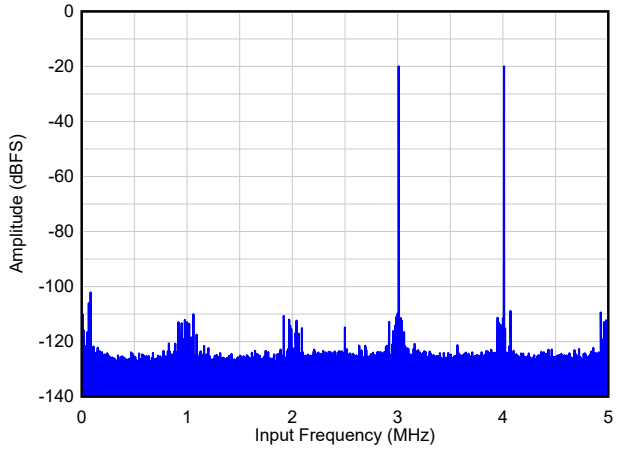
SNR = 82.5 dBFS, SFDR = 82 dBc, Non HD23 = 103 dBFS

图 6-2. Single Tone FFT at F_{IN} = 1.1 MHz, A_{IN} = -20 dBFS



A_{IN} = -7 dBFS/tone, IMD3 = 88 dBc

图 6-3. Two Tone FFT at F_{IN} = 3,4 MHz



A_{IN} = -20 dBFS/tone, IMD3 = 89 dBc

图 6-4. Two Tone FFT at F_{IN} = 3,4 MHz

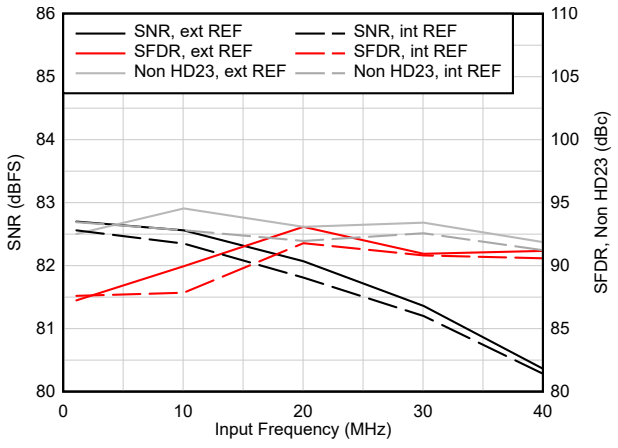


图 6-5. AC Performance vs Input Frequency

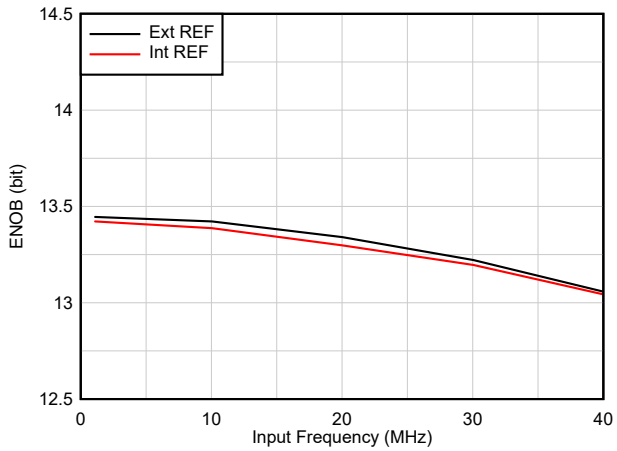


图 6-6. ENOB vs Input Frequency

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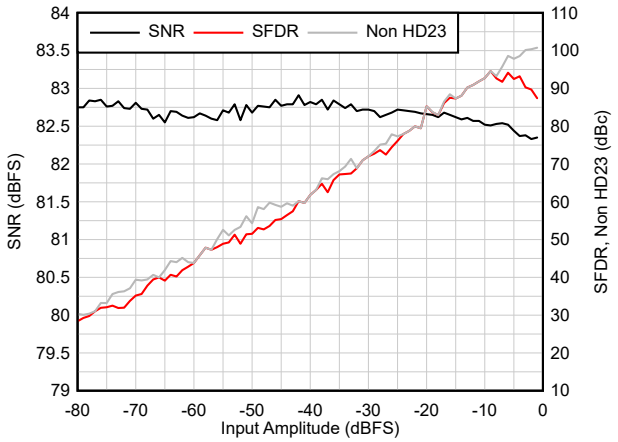
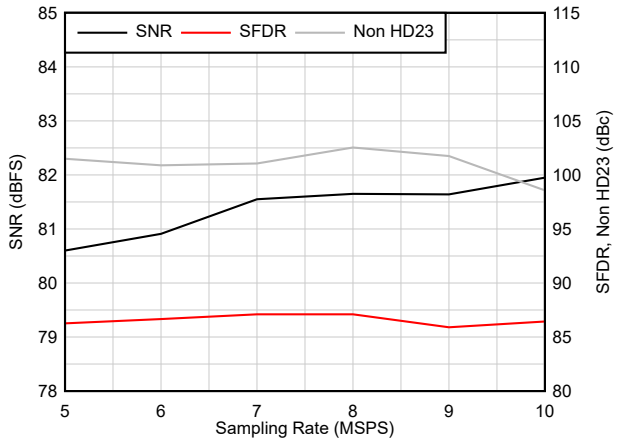
6.9 Typical Characteristics - ADC3561 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 10 MSPS, A_{IN} = – 1 dBFS differential input, AVDD = IOVDD = 1.8 V, external 1.6 V voltage reference, unless otherwise noted.



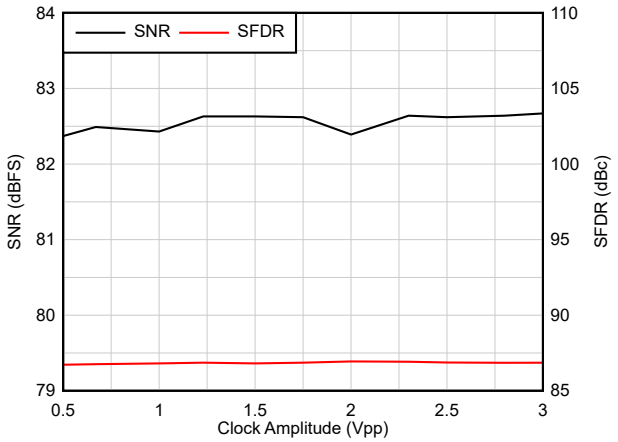
F_{IN} = 1.1 MHz

图 6-7. AC Performance vs Input Amplitude



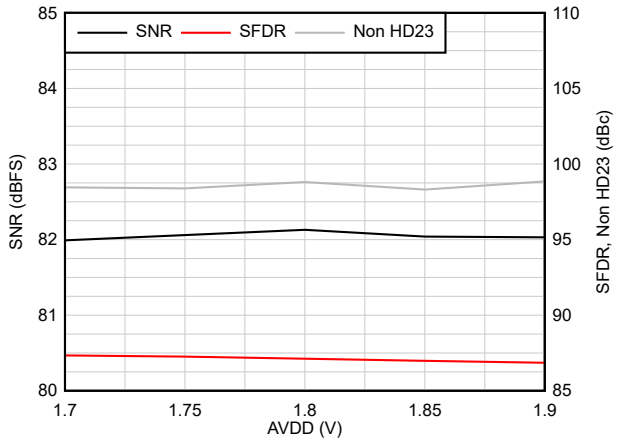
F_{IN} = 1.1 MHz

图 6-8. AC Performance vs Sampling Rate



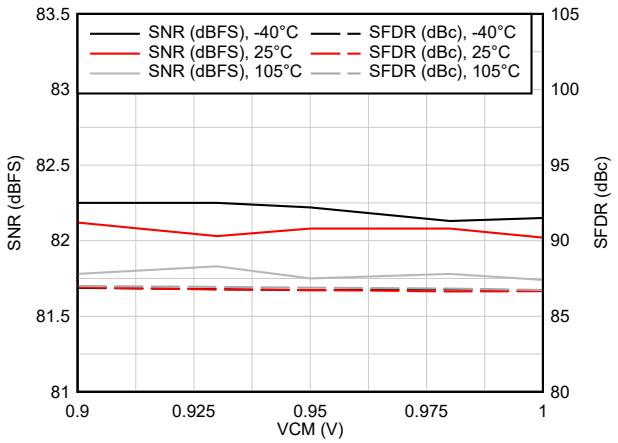
F_{IN} = 1.1 MHz

图 6-9. AC Performance vs Clock Amplitude



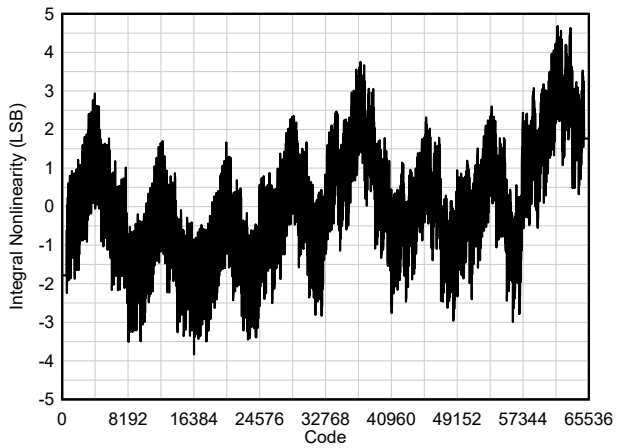
F_{IN} = 1.1 MHz

图 6-10. AC Performance vs AVDD



F_{IN} = 1.1 MHz

图 6-11. AC Performance vs VCM vs Temperature

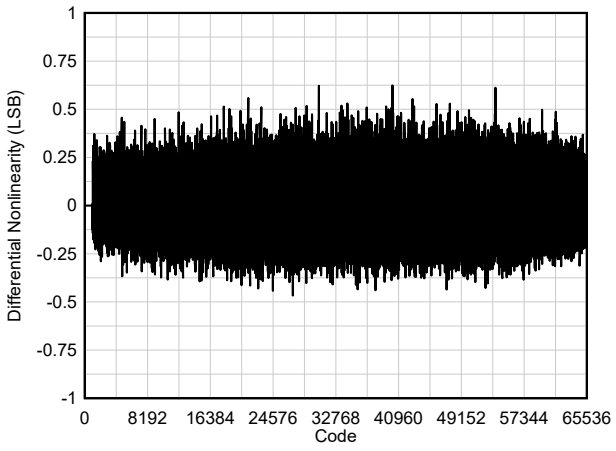


F_{IN} = 1.1 MHz

图 6-12. INL vs Code

6.9 Typical Characteristics - ADC3561 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 10 MSPS, A_{IN} = – 1 dBFS differential input, AVDD = IOVDD = 1.8 V, external 1.6 V voltage reference, unless otherwise noted.



F_{IN} = 1.1 MHz

图 6-13. DNL vs Code

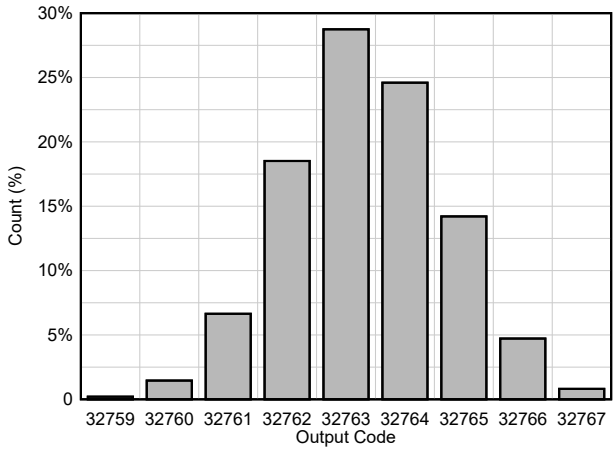
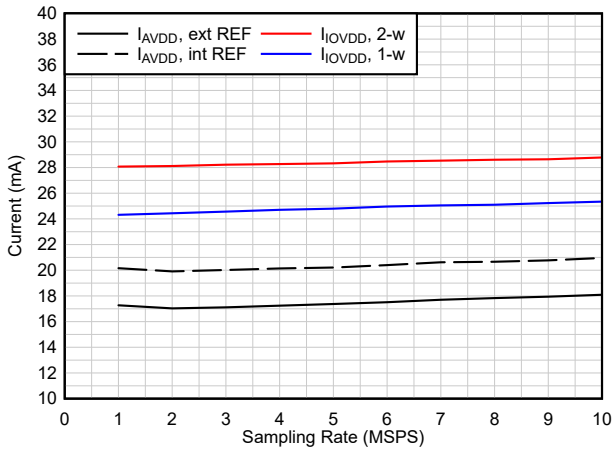
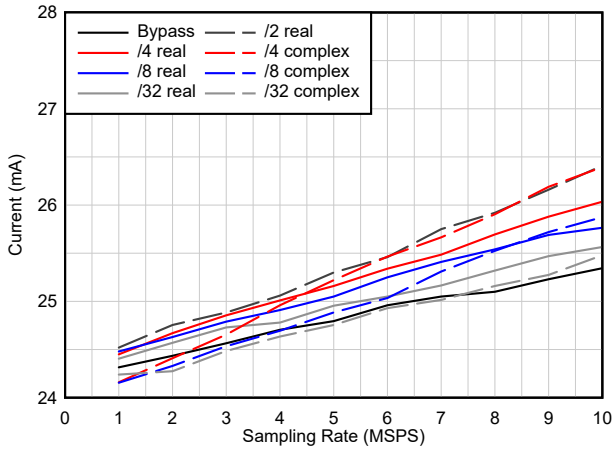


图 6-14. DC Offset Histogram



F_{IN} = 1.1 MHz, DDC Bypass

图 6-15. Current vs Sampling Rate



F_{IN} = 1.1 MHz, 1-wire

图 6-16. I_{IOVDD} Current vs Decimation

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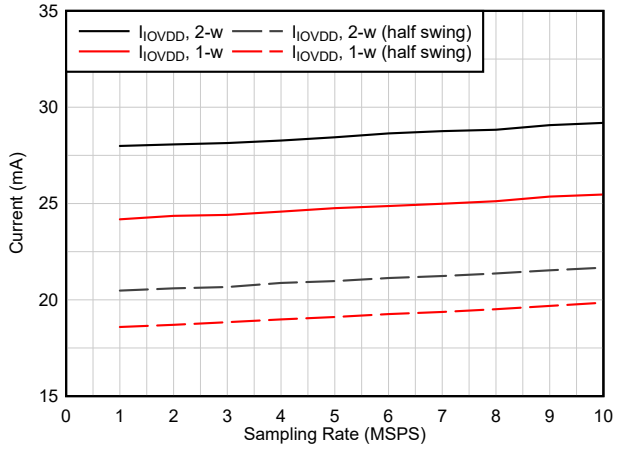
6.9 Typical Characteristics - ADC3561 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 10 MSPS, A_{IN} = – 1 dBFS differential input, AVDD = IOVDD = 1.8 V, external 1.6 V voltage reference, unless otherwise noted.

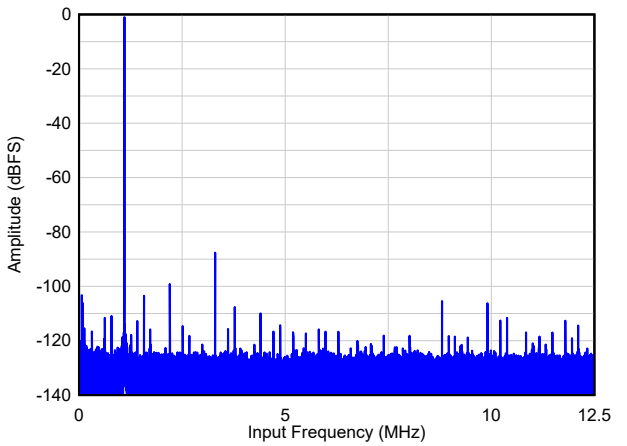


F_{IN} = 1.1 MHz, Complex Decimation by 32

图 6-17. I_{IOVDD} Current vs Interface

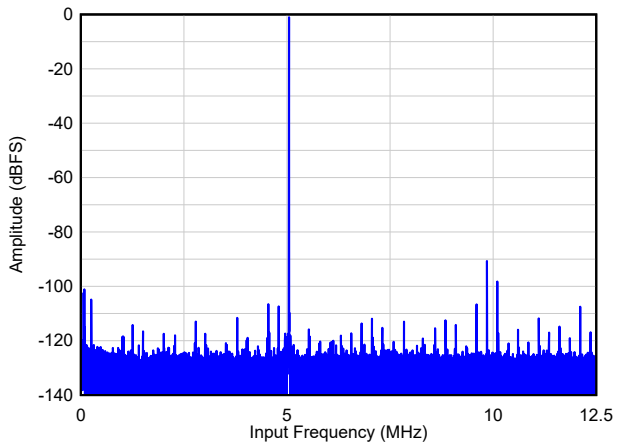
6.10 Typical Characteristics - ADC3562

Typical values at T_A = 25 °C, ADC sampling rate = 25 MSPS, A_{IN} = – 1 dBFS differential input, AVDD = IOVDD = 1.8 V, external 1.6 V voltage reference, unless otherwise noted.



SNR = 82.1 dBFS, SFDR = 87 dBc, Non HD23 = 102 dBFS

图 6-18. Single Tone FFT at F_{IN} = 1 MHz



SNR = 82.0 dBFS, SFDR = 92 dBc, Non HD23 = 101 dBFS

图 6-19. Single Tone FFT at F_{IN} = 5 MHz

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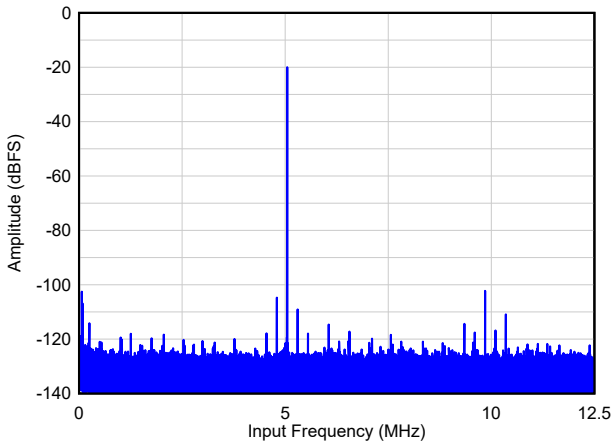
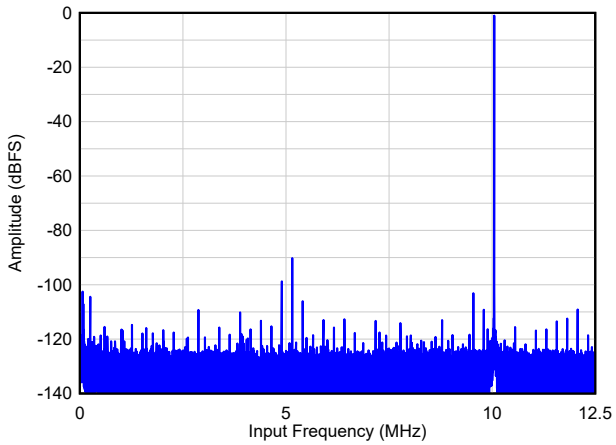
6.10 Typical Characteristics - ADC3562 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 25 MSPS, A_{IN} = – 1 dBFS differential input, AVDD = IOVDD = 1.8 V, external 1.6 V voltage reference, unless otherwise noted.



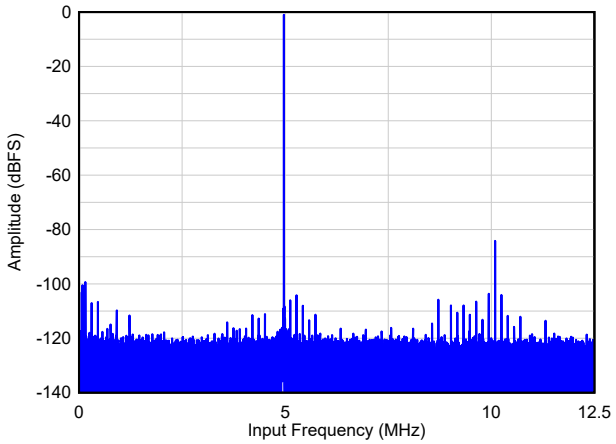
SNR = 82.5 dBFS, SFDR = 82 dBc, Non HD23 = 101 dBFS

图 6-20. Single Tone FFT at F_{IN} = 5 MHz, A_{IN} = -20 dBFS



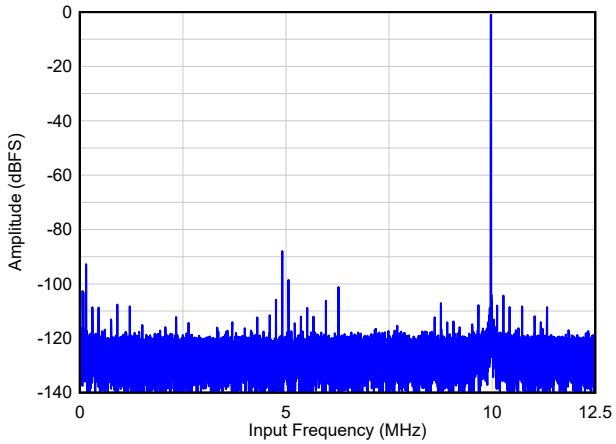
SNR = 81.9 dBFS, SFDR = 85 dBc, Non HD23 = 101 dBFS

图 6-21. Single Tone FFT at F_{IN} = 10 MHz



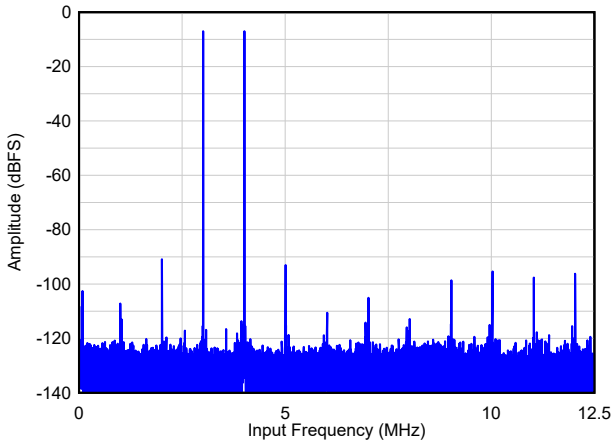
SNR = 81.7 dBFS, SFDR = 83 dBc, Non HD23 = 98 dBFS

图 6-22. Single Tone FFT at F_{IN} = 20 MHz



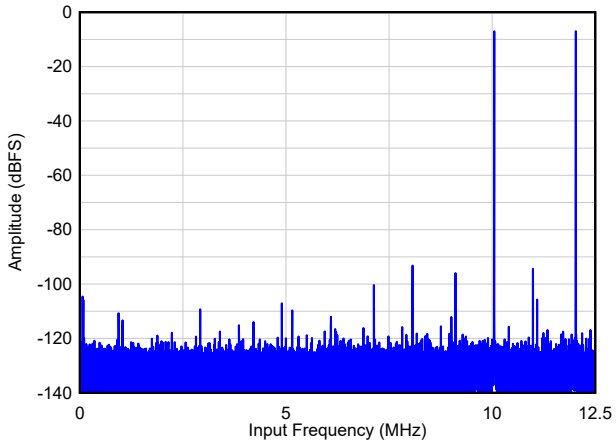
SNR = 78.8 dBFS, SFDR = 87 dBc, Non HD23 = 98 dBFS

图 6-23. Single Tone FFT at F_{IN} = 40 MHz



A_{IN} = -7 dBFS/tone, IMD3 = 84 dBc

图 6-24. Two Tone FFT at F_{IN} = 3/4 MHz



A_{IN} = -7 dBFS/tone, IMD3 = 87 dBc

图 6-25. Two Tone FFT at F_{IN} = 10/12 MHz

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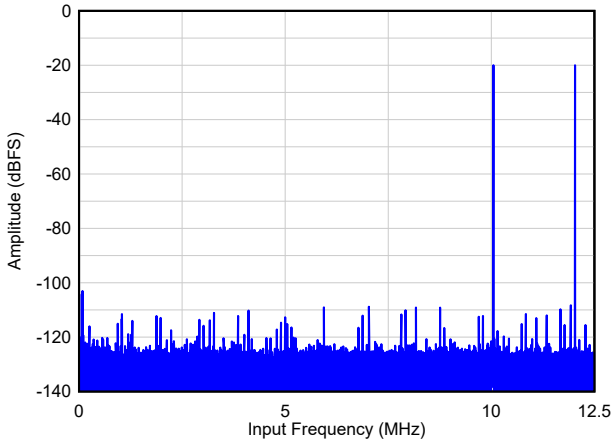
6.10 Typical Characteristics - ADC3562 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 25 MSPS, A_{IN} = – 1 dBFS differential input, AVDD = IOVDD = 1.8 V, external 1.6 V voltage reference, unless otherwise noted.



A_{IN} = -20 dBFS/tone, IMD3 = 88 dBc

图 6-26. Two Tone FFT at F_{IN} = 10/12 MHz

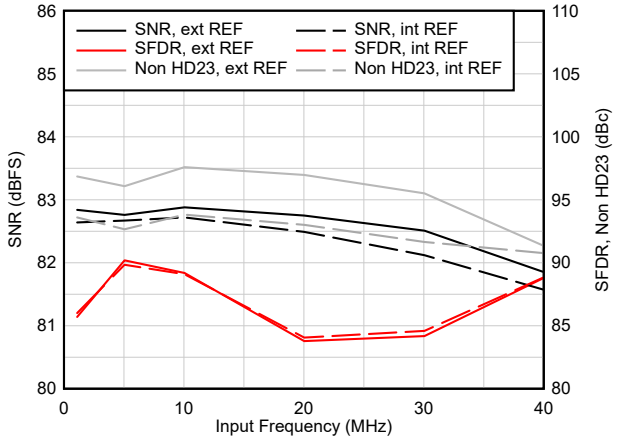


图 6-27. AC Performance vs Input Frequency

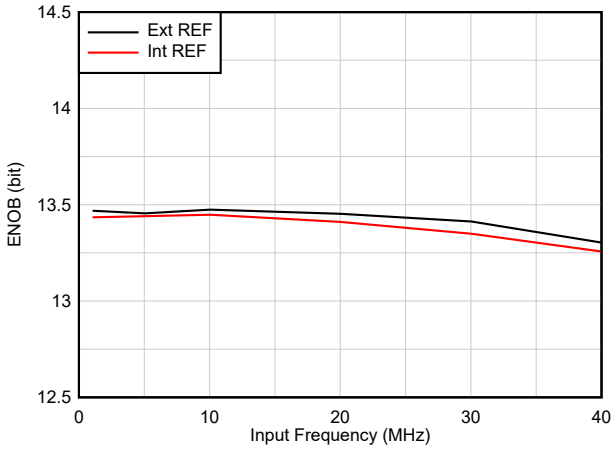
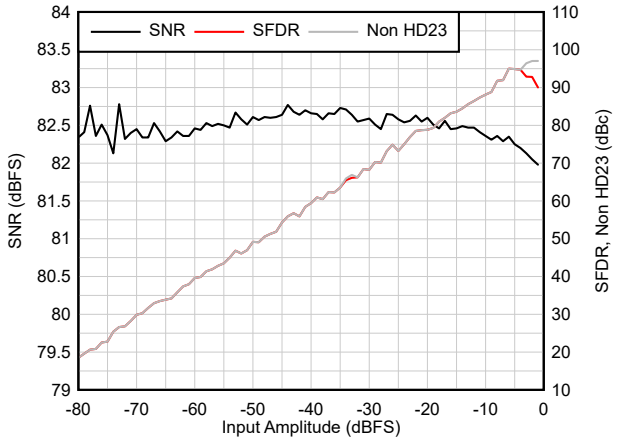
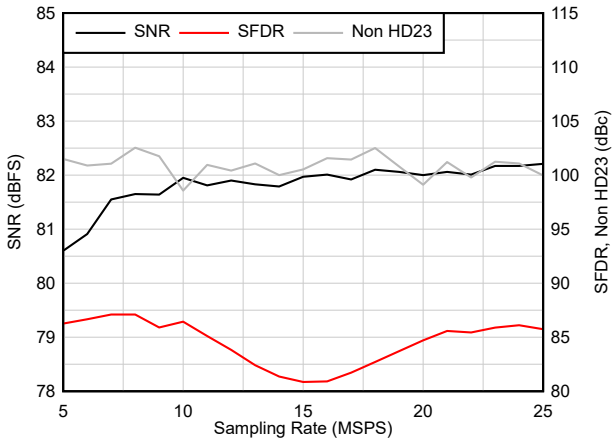


图 6-28. ENOB vs Input Frequency



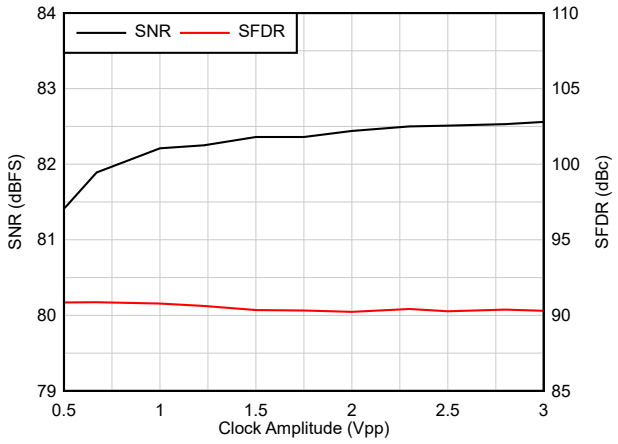
F_{IN} = 1.1 MHz

图 6-29. AC Performance vs Input Amplitude



F_{IN} = 1.1 MHz

图 6-30. AC Performance vs Sampling Rate



F_{IN} = 1.1 MHz

图 6-31. AC Performance vs Clock Amplitude

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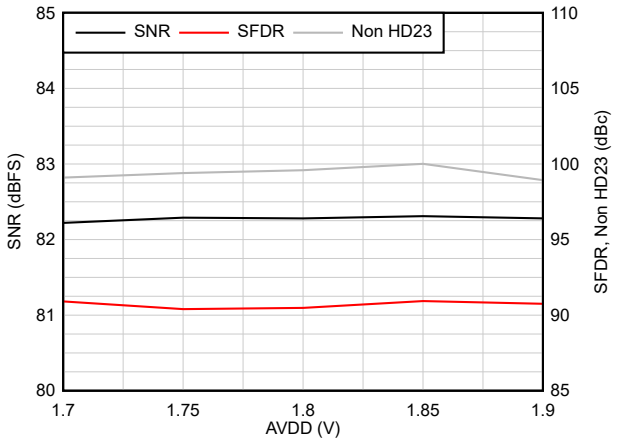
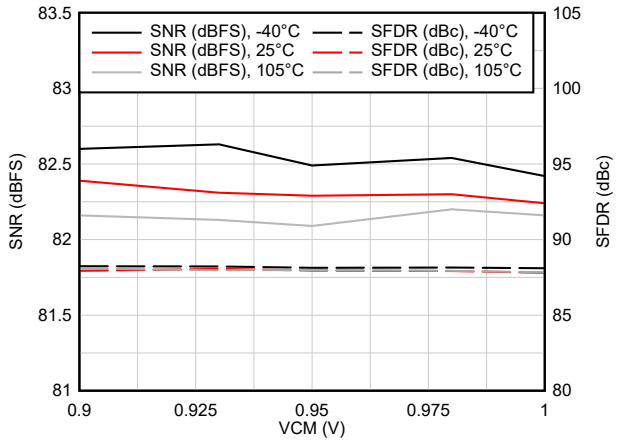
6.10 Typical Characteristics - ADC3562 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 25 MSPS, A_{IN} = – 1 dBFS differential input, AVDD = IOVDD = 1.8 V, external 1.6 V voltage reference, unless otherwise noted.



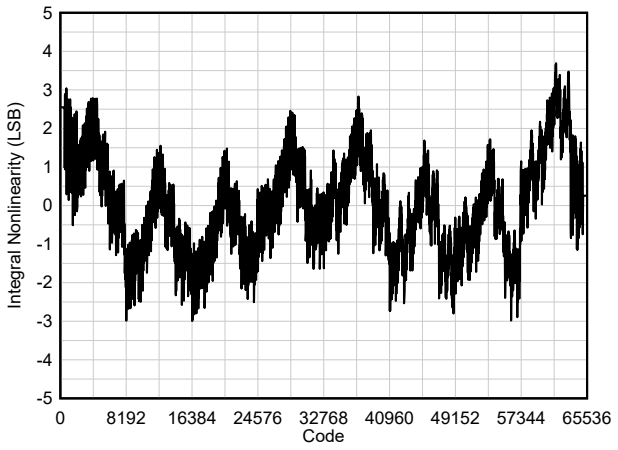
F_{IN} = 1.1 MHz

图 6-32. AC Performance vs AVDD



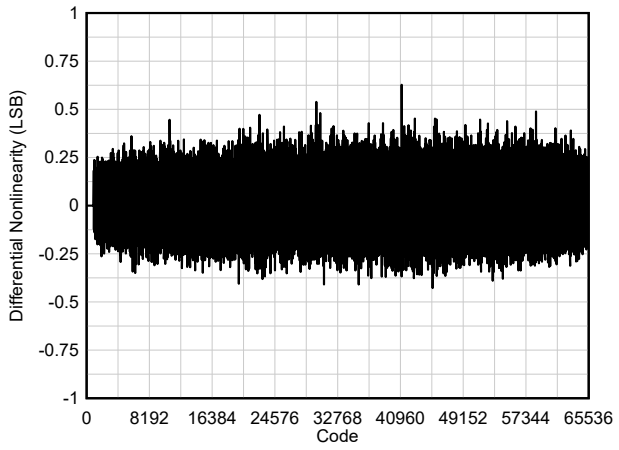
F_{IN} = 1.1 MHz

图 6-33. AC Performance vs VCM vs Temperature



F_{IN} = 1.1 MHz

图 6-34. INL vs Code



F_{IN} = 1.1 MHz

图 6-35. DNL vs Code

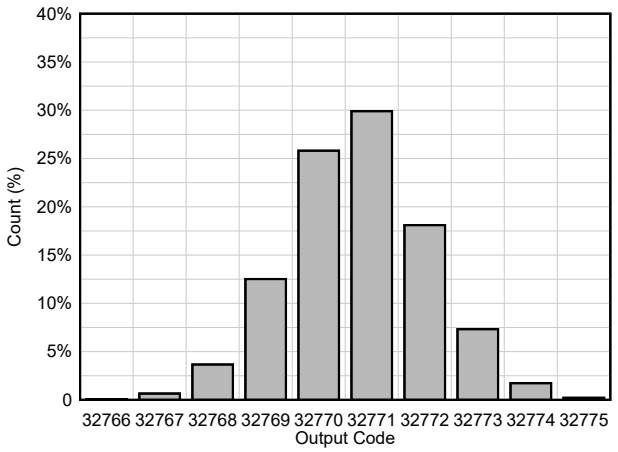
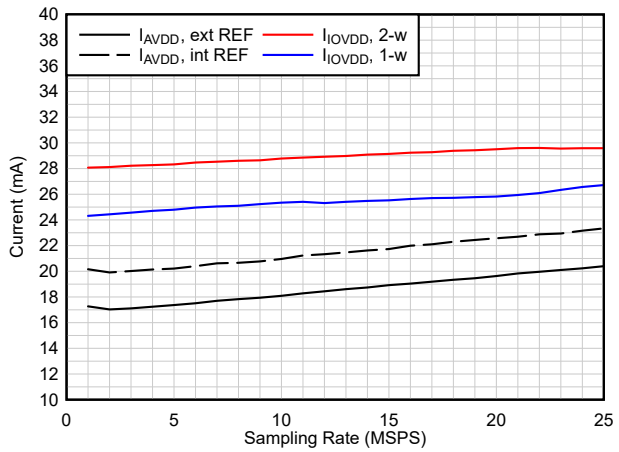


图 6-36. DC Offset Histogram



F_{IN} = 1.1 MHz, DDC Bypass

图 6-37. Current vs Sampling Rate

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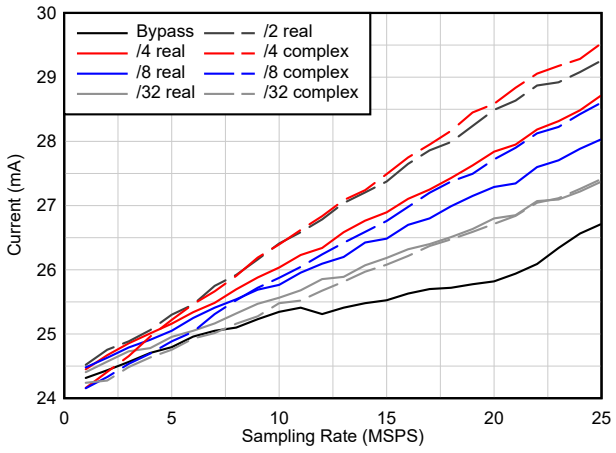
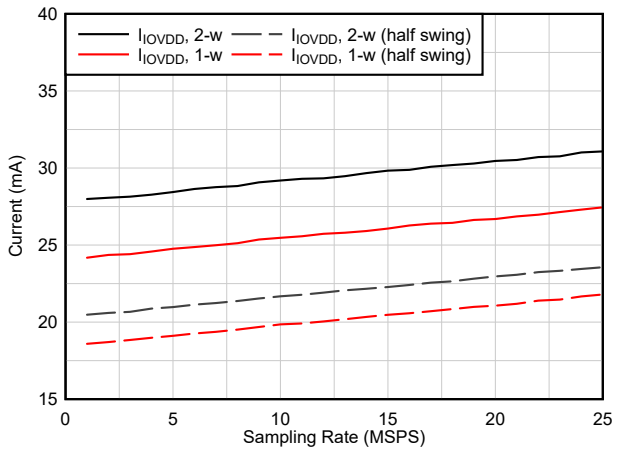
6.10 Typical Characteristics - ADC3562 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 25 MSPS, A_{IN} = – 1 dBFS differential input, AVDD = IOVDD = 1.8 V, external 1.6 V voltage reference, unless otherwise noted.



F_{IN} = 1.1 MHz, 1-wire

图 6-38. I_{IOVDD} Current vs Decimation

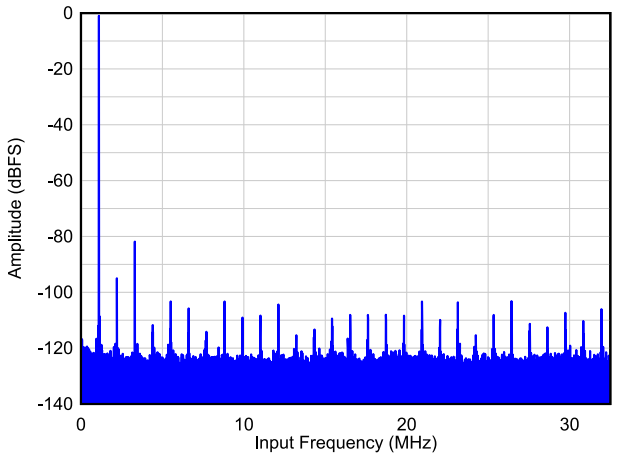


F_{IN} = 1.1 MHz, Complex Decimation by 32

图 6-39. I_{IOVDD} Current vs Interface

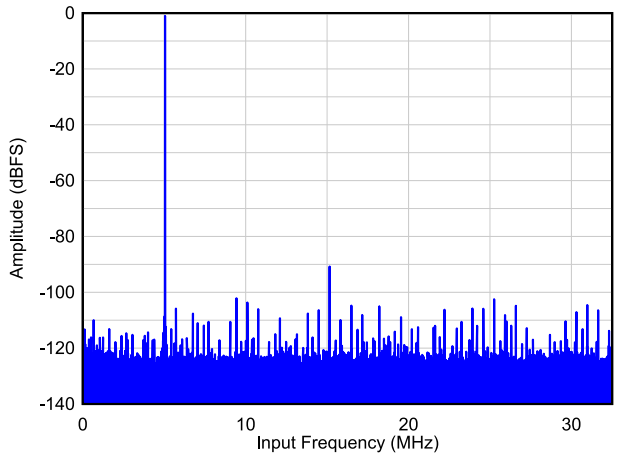
6.11 Typical Characteristics - ADC3563

Typical values at T_A = 25 °C, ADC sampling rate = 65 MSPS, A_{IN} = – 1 dBFS differential input, AVDD = IOVDD = 1.8 V, external 1.6 V voltage reference, unless otherwise noted.



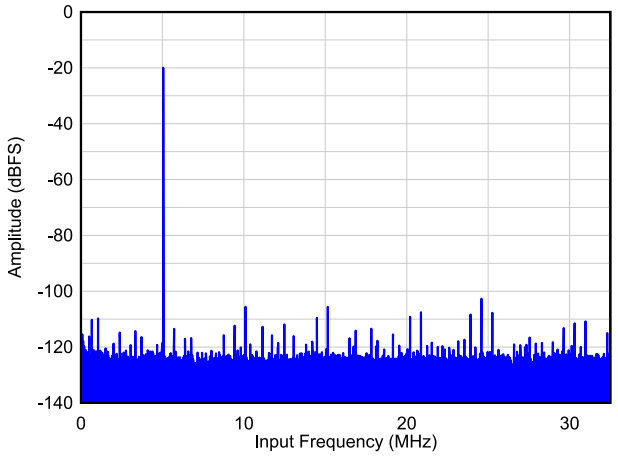
SNR = 82.2 dBFS, SFDR = 81 dBc, Non HD23 = 103 dBFS

图 6-40. Single Tone FFT at F_{IN} = 1 MHz



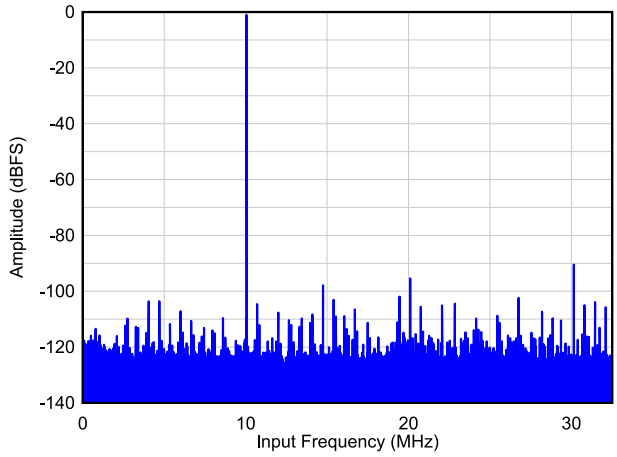
SNR = 82.2 dBFS, SFDR = 90 dBc, Non HD23 = 102 dBFS

图 6-41. Single Tone FFT at F_{IN} = 5 MHz



SNR = 82.4 dBFS, SFDR = 86 dBc, Non HD23 = 103 dBFS

图 6-42. Single Tone FFT at F_{IN} = 5 MHz, A_{IN} = -20 dBFS



SNR = 81.9 dBFS, SFDR = 89 dBc, Non HD23 = 98 dBFS

图 6-43. Single Tone FFT at F_{IN} = 10 MHz

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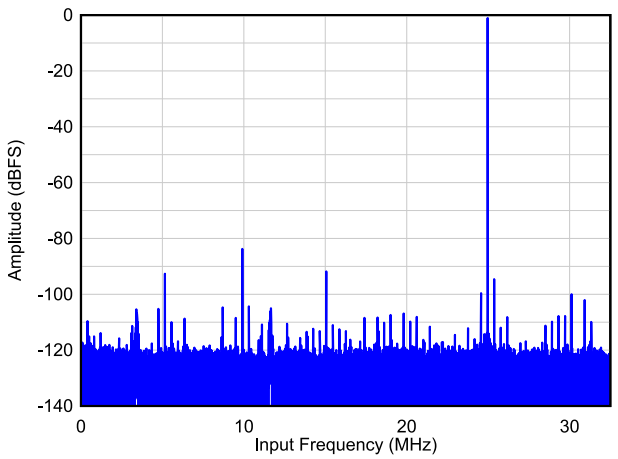
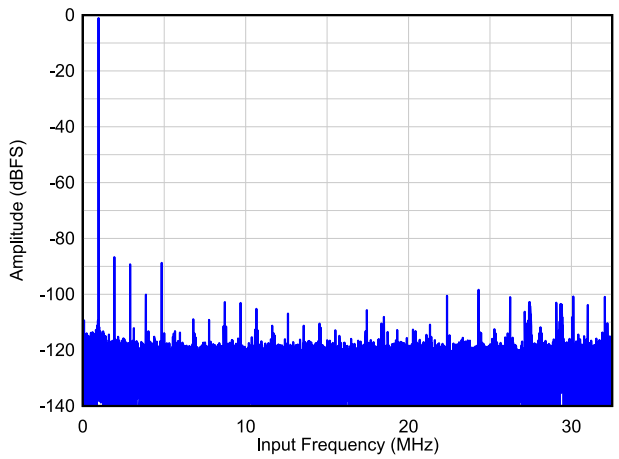
6.11 Typical Characteristics - ADC3563 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 65 MSPS, A_{IN} = – 1 dBFS differential input, AVDD = IOVDD = 1.8 V, external 1.6 V voltage reference, unless otherwise noted.



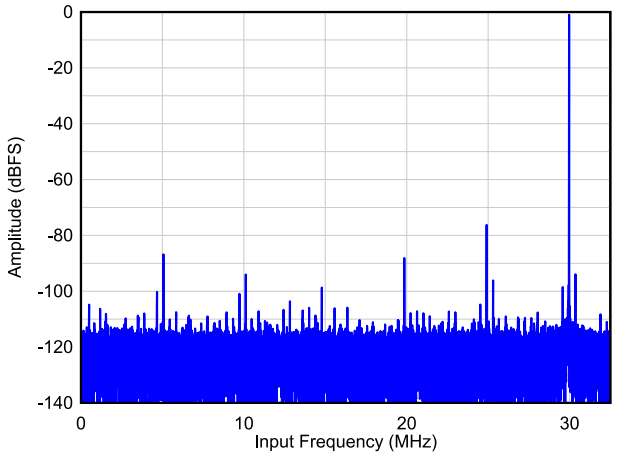
SNR = 80.0 dBFS, SFDR = 83 dBc, Non HD23 = 93 dBFS

图 6-44. Single Tone FFT at F_{IN} = 40 MHz



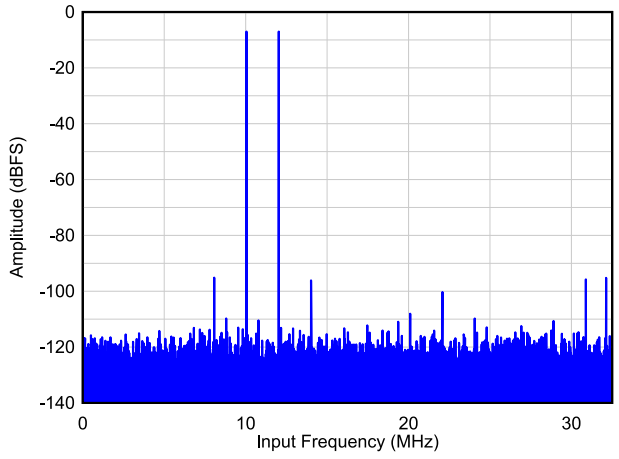
SNR = 77.7 dBFS, SFDR = 86 dBc, Non HD23 = 89 dBFS

图 6-45. Single Tone FFT at F_{IN} = 64 MHz



SNR = 74.1 dBFS, SFDR = 75 dBc, Non HD23 = 88 dBFS

图 6-46. Single Tone FFT at F_{IN} = 100 MHz



A_{IN} = -7 dBFS/tone, IMD3 = 88 dBc

图 6-47. Two Tone FFT at F_{IN} = 10/12 MHz

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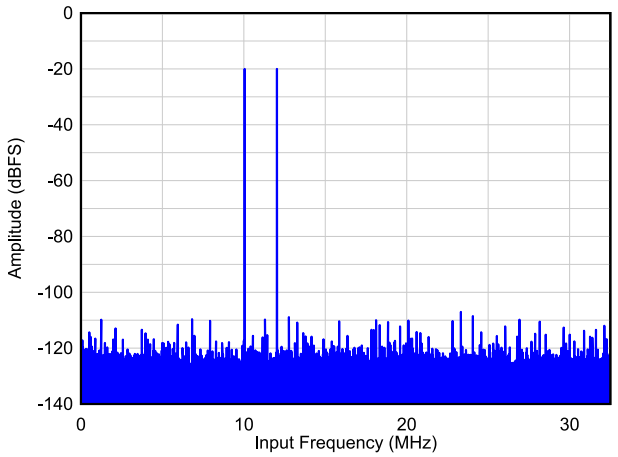
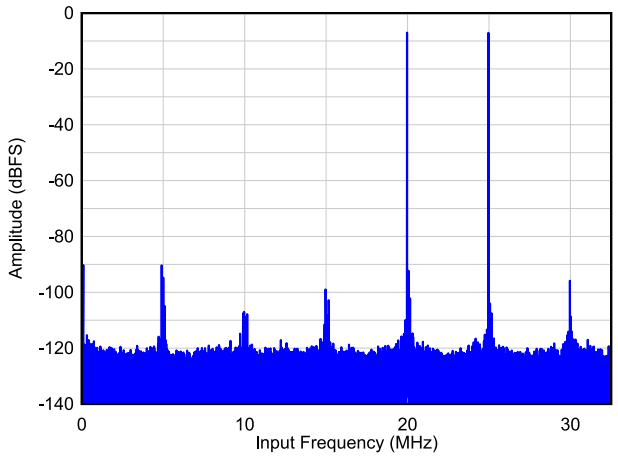
6.11 Typical Characteristics - ADC3563 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 65 MSPS, A_{IN} = – 1 dBFS differential input, AVDD = IOVDD = 1.8 V, external 1.6 V voltage reference, unless otherwise noted.



A_{IN} = -20 dBFS/tone, IMD3 = 98 dBc

图 6-48. Two Tone FFT at F_{IN} = 10/12 MHz



A_{IN} = -7 dBFS/tone, IMD3 = 89 dBc

图 6-49. Two Tone FFT at F_{IN} = 40/45 MHz

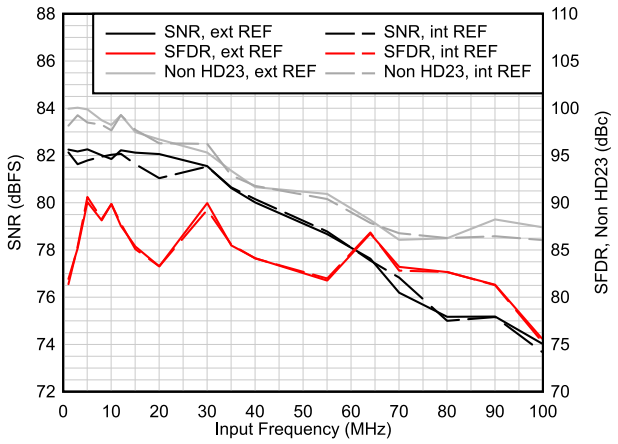


图 6-50. AC Performance vs Input Frequency

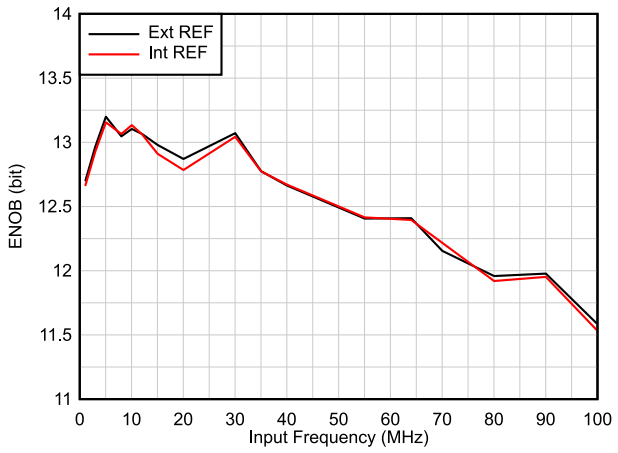
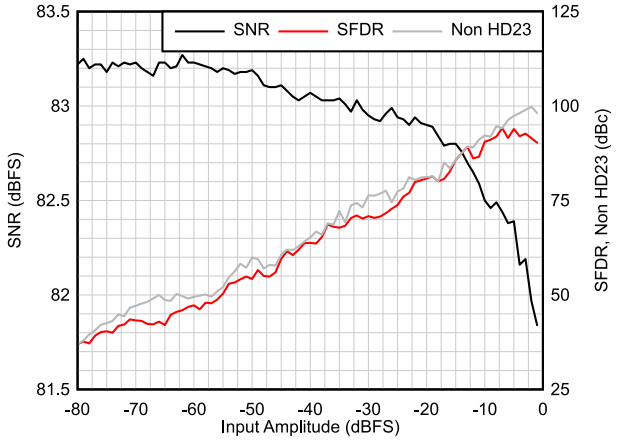
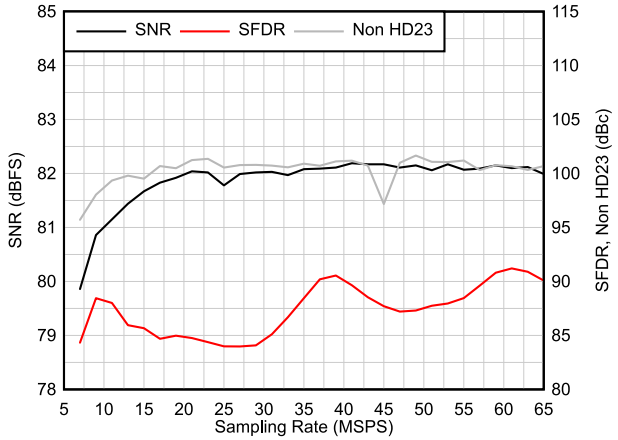


图 6-51. ENOB vs Input Frequency



F_{IN} = 5 MHz

图 6-52. AC Performance vs Input Amplitude



F_{IN} = 5 MHz

图 6-53. AC Performance vs Sampling Rate

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6.11 Typical Characteristics - ADC3563 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 65 MSPS, A_{IN} = – 1 dBFS differential input, AVDD = IOVDD = 1.8 V, external 1.6 V voltage reference, unless otherwise noted.

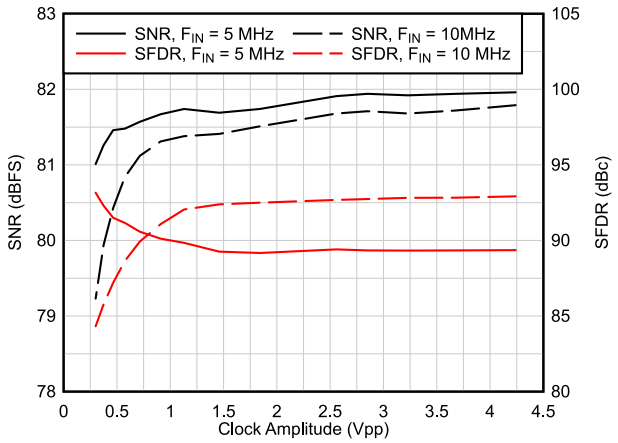
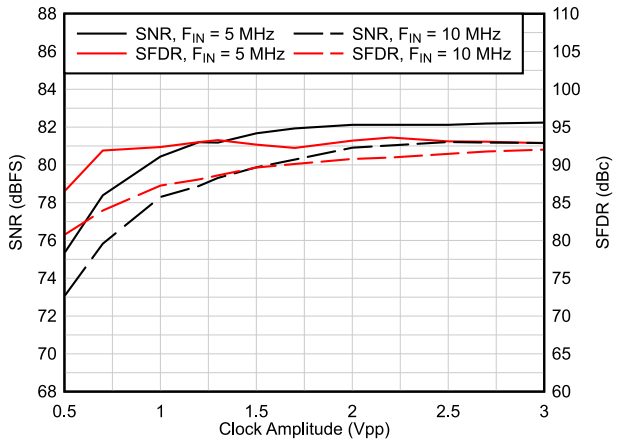
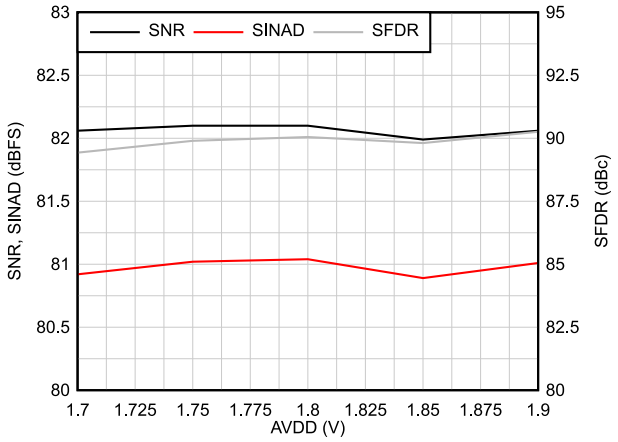


图 6-54. AC Performance vs Clock Amplitude



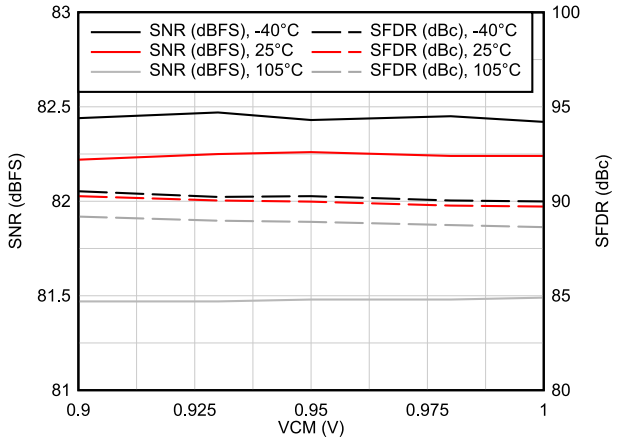
Single Ended Clock Input

图 6-55. AC Performance vs Clock Amplitude



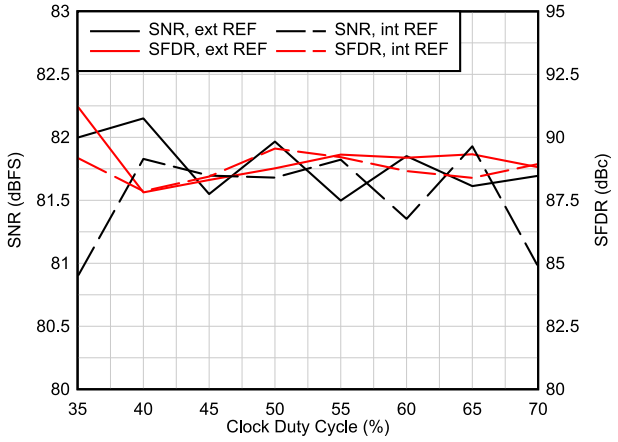
F_{IN} = 5 MHz

图 6-56. AC Performance vs AVDD



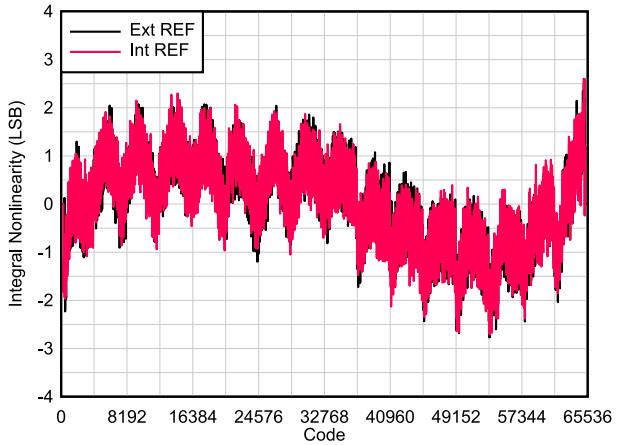
F_{IN} = 5 MHz

图 6-57. AC Performance vs VCM vs Temperature



F_{IN} = 5 MHz

图 6-58. AC Performance vs Clock Duty Cycle



F_{IN} = 5 MHz

图 6-59. INL vs Code

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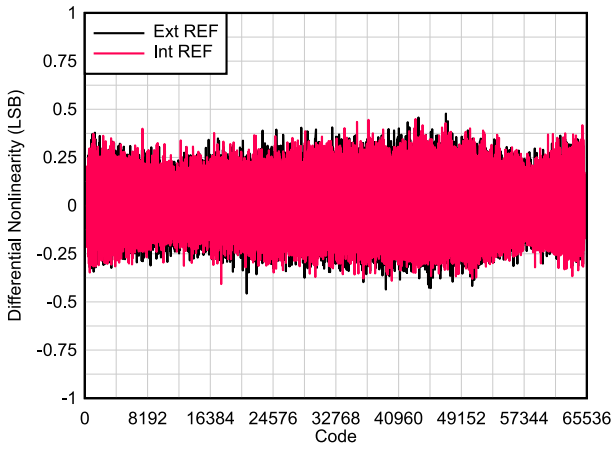
6.11 Typical Characteristics - ADC3563 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 65 MSPS, A_{IN} = – 1 dBFS differential input, AVDD = IOVDD = 1.8 V, external 1.6 V voltage reference, unless otherwise noted.



F_{IN} = 5 MHz

图 6-60. DNL vs Code

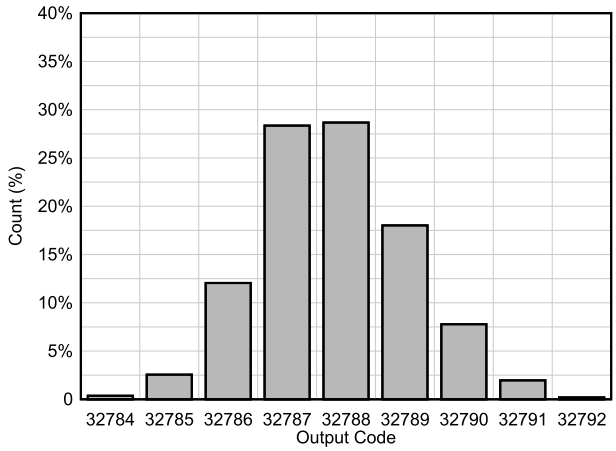
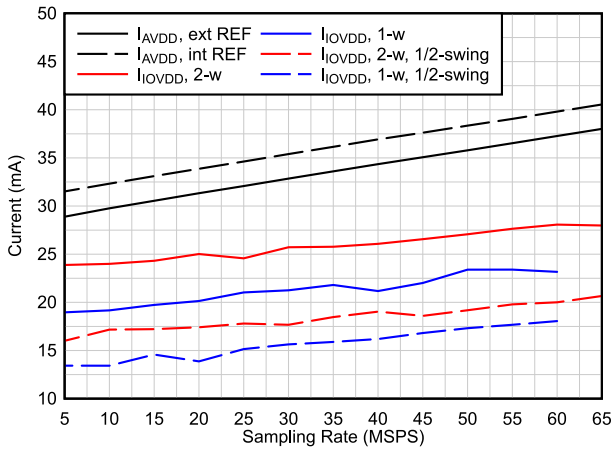
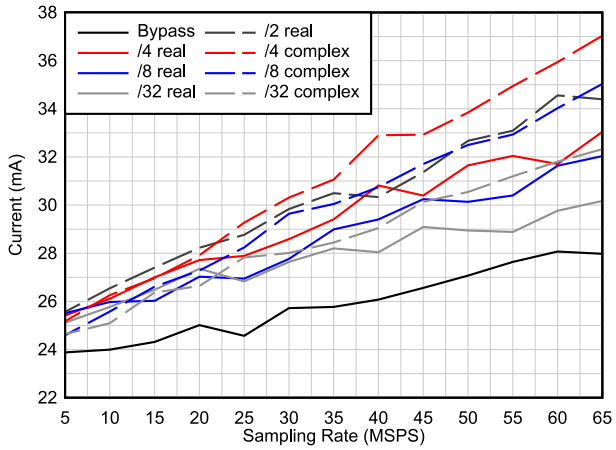


图 6-61. DC Offset Histogram



F_{IN} = 5 MHz, DDC Bypass

图 6-62. Current vs Sampling Rate



F_{IN} = 5 MHz, 2-wire

图 6-63. Current vs Decimation

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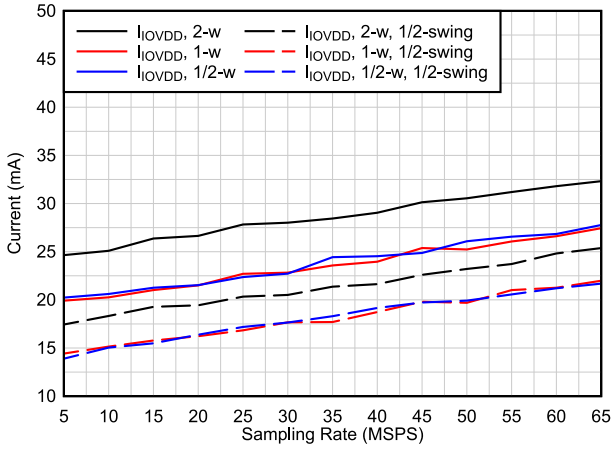
6.11 Typical Characteristics - ADC3563 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 65 MSPS, A_{IN} = – 1 dBFS differential input, AVDD = IOVDD = 1.8 V, external 1.6 V voltage reference, unless otherwise noted.



F_{IN} = 5 MHz, Complex Decimation by 32

图 6-64. Current vs Output Interface

7 Parameter Measurement Information

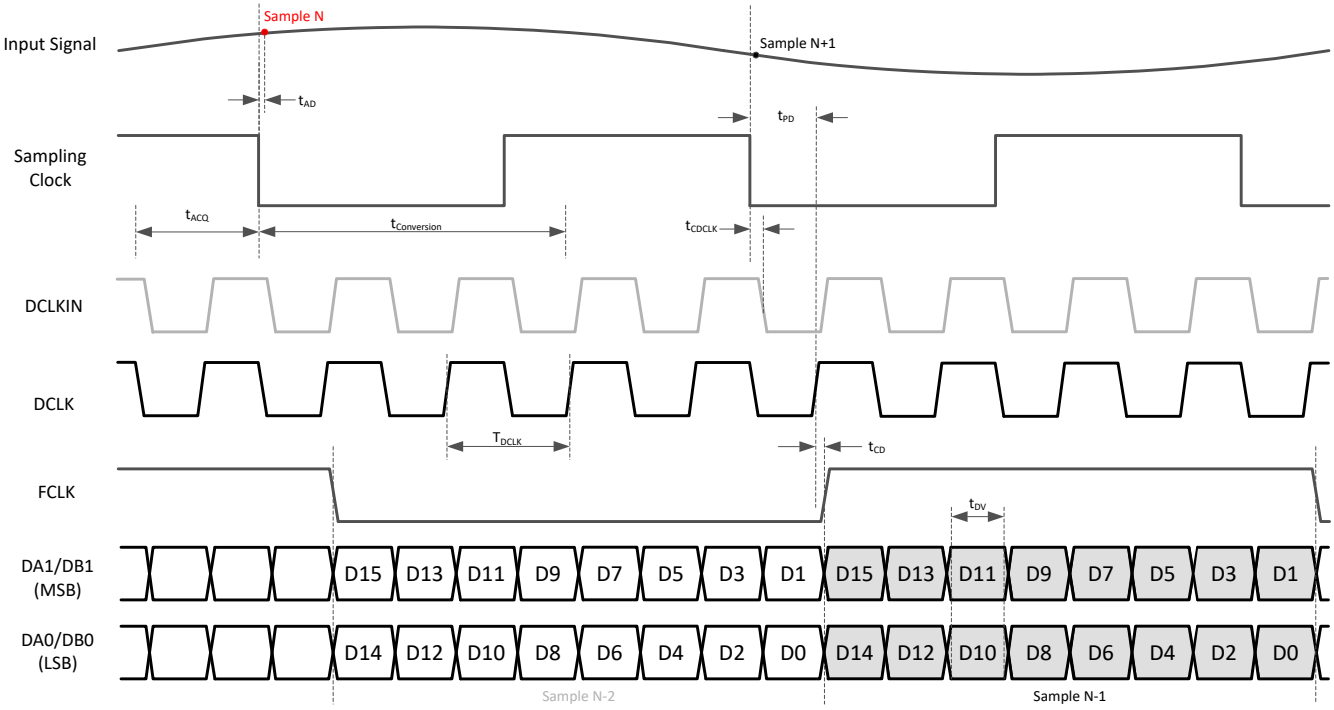


图 7-1. Timing diagram: 2-wire SLVDS (default output bit mapper)

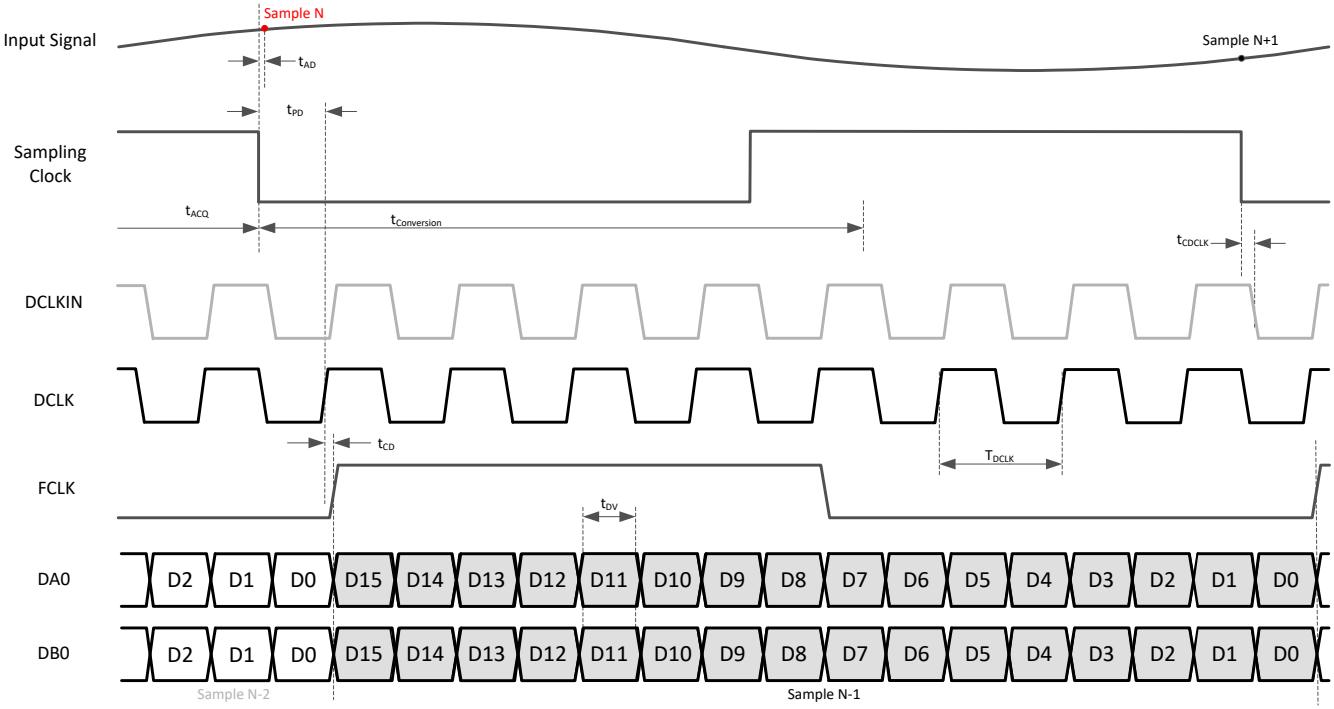


图 7-2. Timing diagram: 1-wire SLVDS (default output bit mapper)

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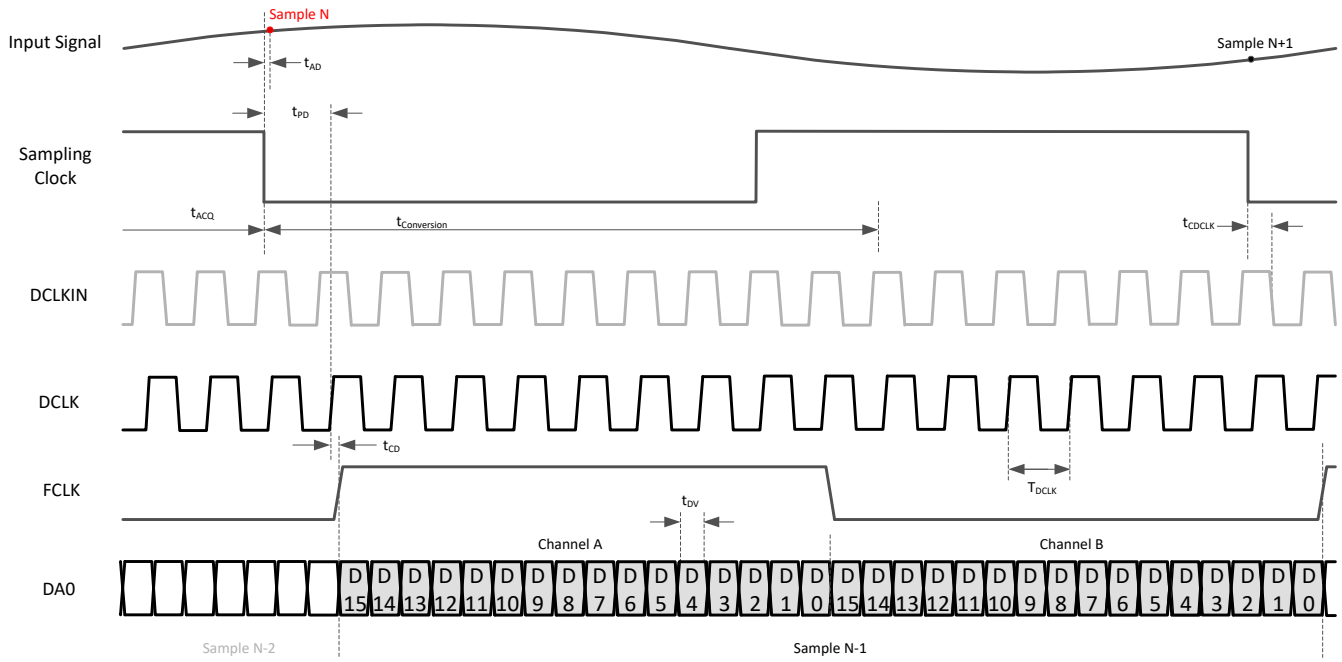


图 7-3. Timing diagram:1/2-wire SLVDS (default output bit mapper)

8 Detailed Description

8.1 Overview

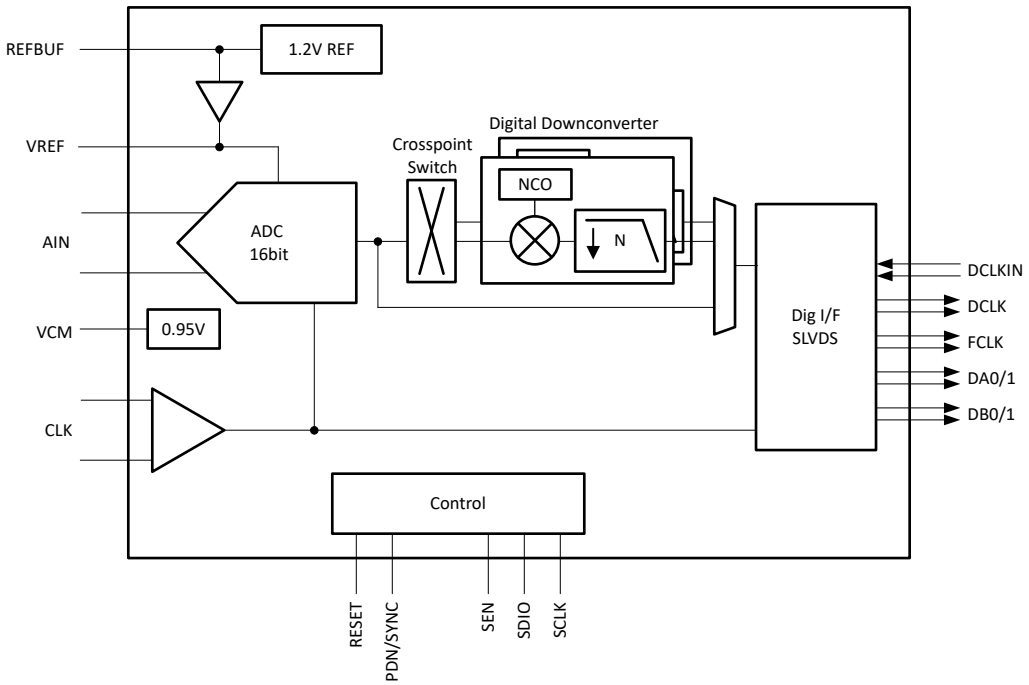
The ADC356x is a low noise, ultra-low power 16-bit high-speed single channel ADC supporting sampling rates up to 65 Msps. It offers very good DC precision together with IF sampling support which makes it ideally suited for a wide range of applications. The ADC356x is equipped with an on-chip internal reference option but it also supports the use of an external, high precision 1.6 V voltage reference or an external 1.2V reference which is buffered and gained up internally. Because of the inherent low latency architecture, the digital output result is available after only one to two clock cycles. Single ended as well as differential input signaling is supported.

An optional programmable digital down converter enables external anti-alias filter relaxation as well as output data rate reduction. An internal mux enables dual band complex decimation with independent NCO frequency tuning. The digital filter provides a 32-bit programmable NCO and supports both real or complex decimation.

The ADC356x family uses a serial LVDS (SLVDS) interface to output the data which minimizes the number of digital interconnects. The device supports a two-lane (2-wire), a one-lane (1-wire) and a half-lane (1/2-wire) option. The ADC356x includes a digital output formatter which supports output resolutions from 14 to 20-bit.

The device features and control options can be set up either through pin configurations or via SPI register writes.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Analog Input

The analog inputs of ADC356x are intended to be driven differentially. Both AC coupling and DC coupling of the analog inputs is supported. The analog inputs are designed for an input common mode voltage of 0.95 V which must be provided externally on each input pin. DC-coupled input signals must have a common mode voltage that meets the device input common mode voltage range.

The equivalent input network diagram is shown in 图 8-1. All four sampling switches, on-resistance shown in red are in same position (open or closed) simultaneously.

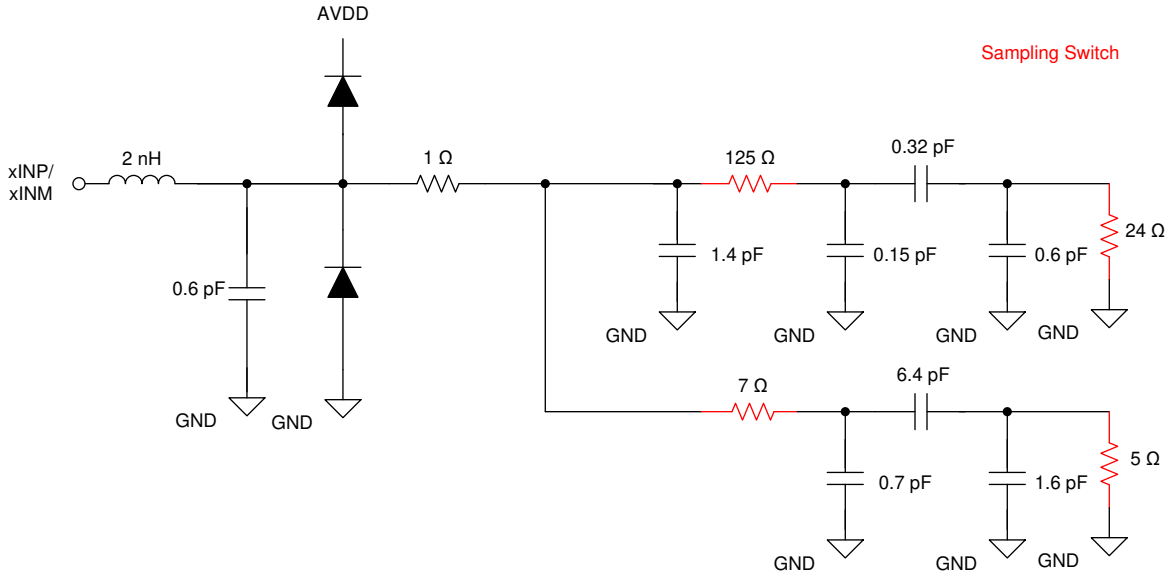

图 8-1. Equivalent Input Network

8.3.1.1 Analog Input Bandwidth

图 8-2 shows the analog full power input bandwidth of the ADC356x with a 50 Ω differential termination. The -3 dB bandwidth is approximately 900 MHz and the useful input bandwidth with good AC performance is approximately 120 MHz.

The equivalent differential input resistance R_{IN} and input capacitance C_{IN} vs frequency are shown in 图 8-3.

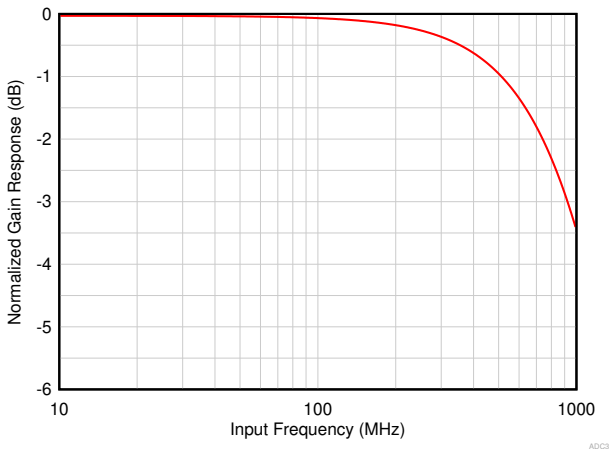

图 8-2. ADC Analog Input bandwidth response

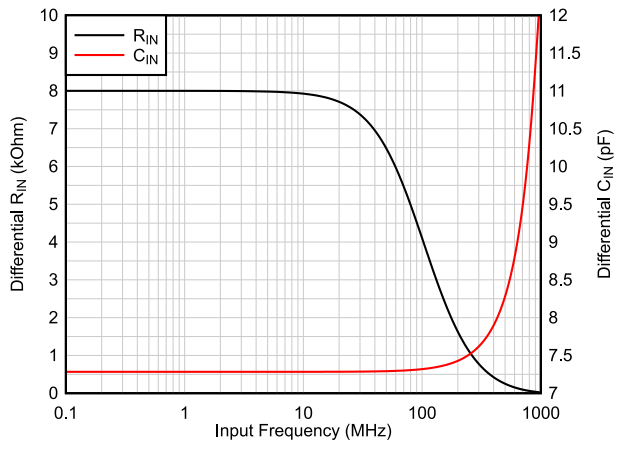

图 8-3. Equivant R_{IN}, C_{IN} vs Input Frequency

8.3.1.2 Analog Front End Design

The ADC356x is an unbuffered ADC and thus a passive kick-back filter is recommended to absorb the glitch from the sampling operation. Depending on if the input is driven by a balun or a differential amplifier with low output impedance, a termination network may be needed. Additionally a passive DC bias circuit is needed in AC-coupled applications which can be combined with the termination network.

8.3.1.2.1 Sampling Glitch Filter Design

The front end sampling glitch filter is designed to optimize the SNR and HD3 performance of the ADC. The filter performance is dependent on input frequency and therefore the following filter designs are recommended for different input frequency ranges as shown in 图 8-4 and 图 8-5.

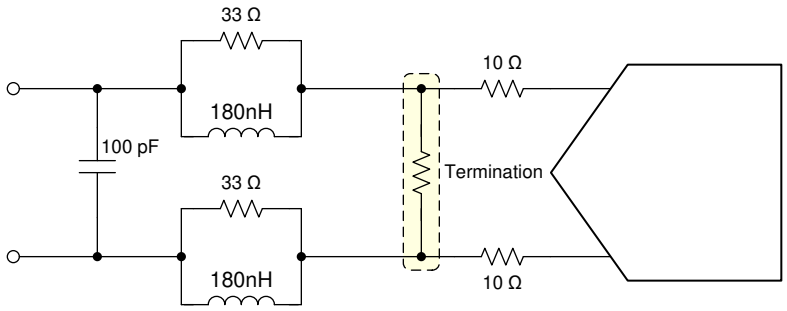

图 8-4. Sampling glitch filter example for input frequencies from DC to 30 MHz

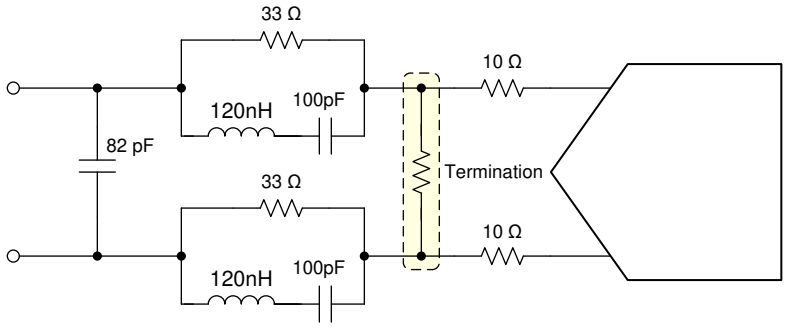

图 8-5. Sampling glitch filter example for input frequencies from 30 to 70 MHz

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8.3.1.2.2 Analog Input Termination and DC Bias

Depending on the input drive circuitry, a termination network and/or DC biasing needs to be provided.

8.3.1.2.2.1 AC-Coupling

The ADC356x requires external DC bias using the common mode output voltage (VCM) of the ADC together with the termination network as shown in 图 8-6. The termination is located within the glitch filter network. When using a balun on the input, the termination impedance has to be adjusted to account for the turns ratio of the transformer. When using an amplifier, the termination impedance can be adjusted to optimize the amplifier performance.

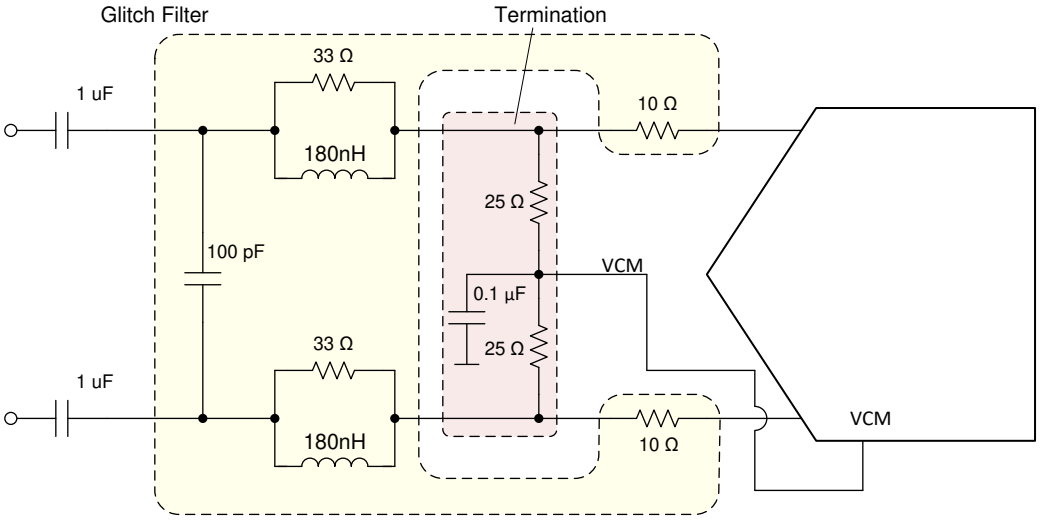

图 8-6. AC-Coupling: termination network provides DC bias (glitch filter example for DC - 30 MHz)

8.3.1.2.2.2 DC-Coupling

In DC coupled applications the DC bias needs to be provided from the fully differential amplifier (FDA) using VCM output of the ADC as shown in 图 8-7. The glitch filter in this case is located between the anti-alias filter and the ADC. No termination may be needed if amplifier is located close to the ADC or if the termination is part of the anti-alias filter.

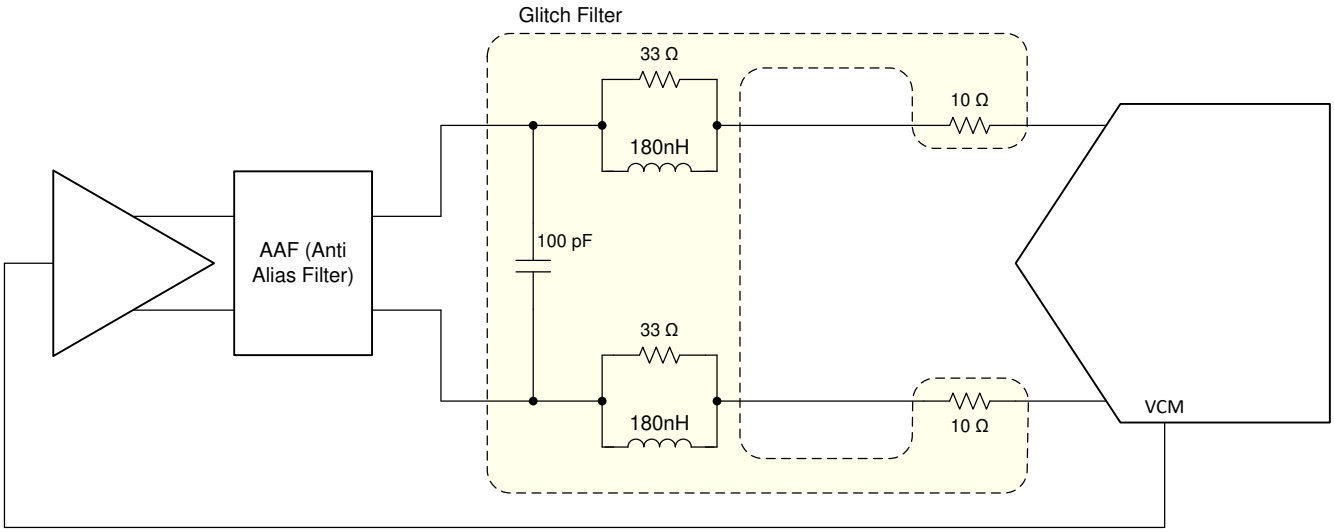

图 8-7. DC-Coupling: DC bias provided by FDA (glitch filter example for DC - 30 MHz)

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8.3.1.3 Auto-Zero Feature

The ADC356x includes an internal auto-zero front end amplifier circuit which improves the 1/f flicker noise. This auto-zero feature is enabled by default for the ADC3561/2 and can be enabled using SPI register writes for the ADC3563 (register 0x11, D0). The 4M point FFTs below show the autozero feature enabled vs disabled.

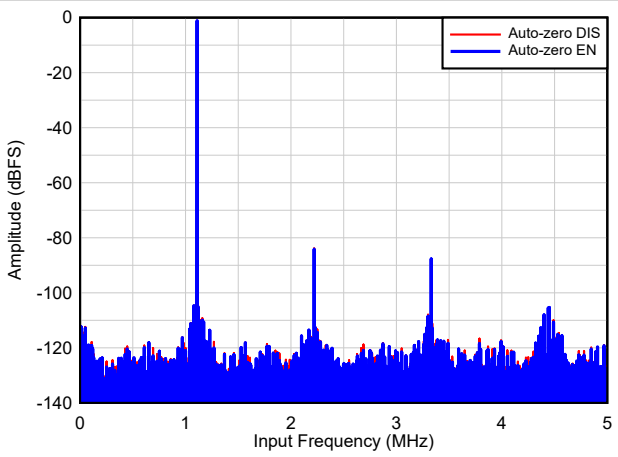

图 8-8. F_S = 10 MSPS, F_{IN} = 1.1 MHz

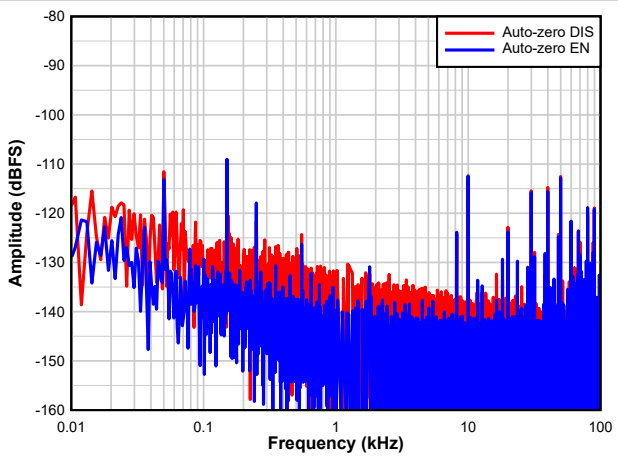

图 8-9. F_S = 10 MSPS, F_{IN} = 1.1 MHz

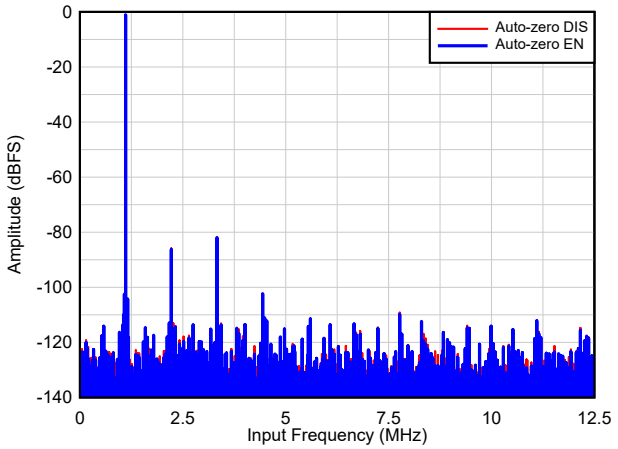

图 8-10. F_S = 25 MSPS, F_{IN} = 1.1 MHz

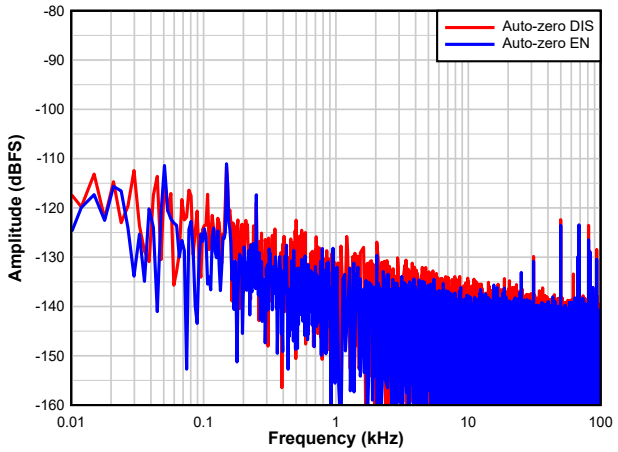

图 8-11. F_S = 25 MSPS, F_{IN} = 1.1 MHz

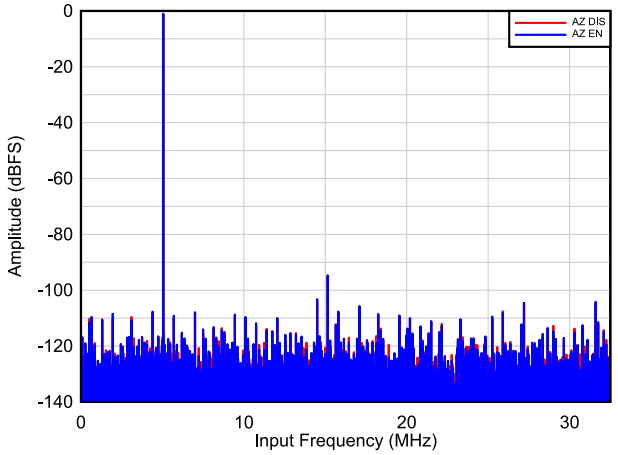

图 8-12. F_S = 65 MSPS, F_{IN} = 5 MHz

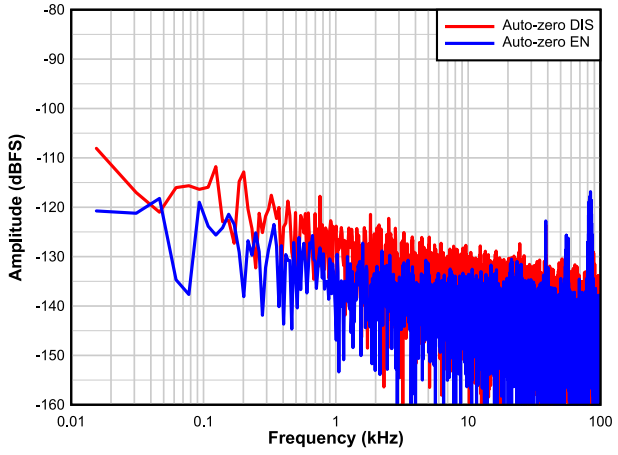

图 8-13. F_S = 65 MSPS, F_{IN} = 5 MHz

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8.3.2 Clock Input

In order to maximize the ADC SNR performance, the external sampling clock should be low jitter and differential signaling with a high slew rate. This is especially important in IF sampling applications (图 8-14 and 图 8-15). For less jitter sensitive applications, the ADC356x provides the option to operate with single ended signaling which saves additional power consumption.

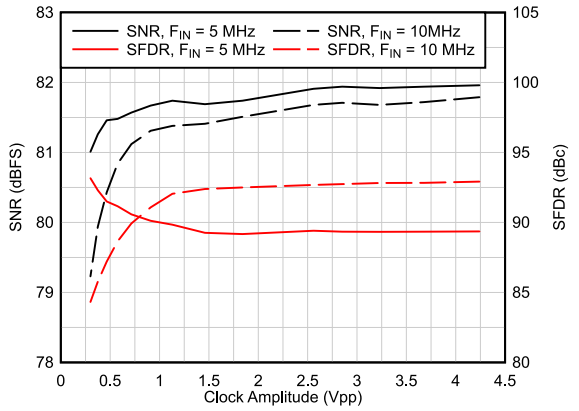

图 8-14. AC Performance vs Clock Amplitude (Differential Clock Input)

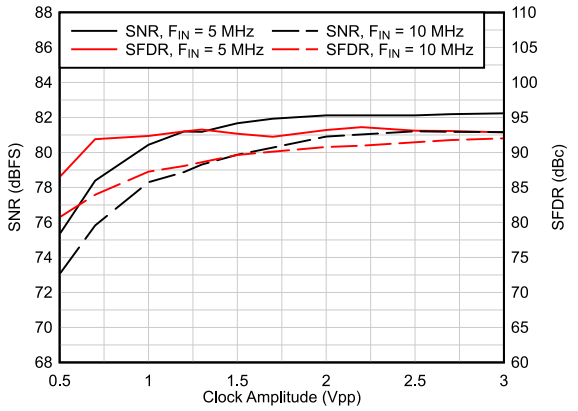

图 8-15. AC Performance vs Clock Amplitude (Single Ended Clock Input)

8.3.2.1 Single Ended vs Differential Clock Input

The ADC356x can be operated using a differential or a single ended clock input where the single ended clock consumes less power consumption. However clock amplitude impacts the ADC aperture jitter and consequently the SNR. For maximum SNR performance, a large clock signal with fast slew rates needs to be provided.

- Differential Clock Input: The clock input can be AC coupled externally. The ADC356x provides internal bias.
- Single Ended Clock Input: This mode needs to be configured using SPI register (0x0E, D2 and D0) or with the REFBUF pin. In this mode there is no internal clock biasing and thus the clock input needs to be DC coupled around a 0.9V center. The unused input needs to be AC coupled to ground.

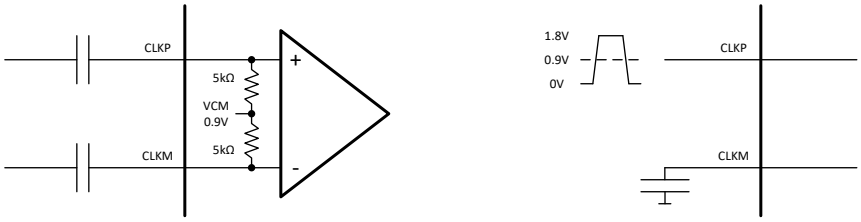

图 8-16. External and internal connection using differential (left) and single ended (right) clock input

8.3.2.2 Signal Acquisition Time Adjust

The ADC356x includes a register (DLL PDN (0x11, D2) which increases the signal acquisition time window for clock rates below 40 MSPS from 25% to 50% of the clock period. Increasing the sampling time provides a longer time for the driving amplifier to settle out the signal which can improve the SNR performance of the system. This register should only be used for the 65 MSPS speed grade (ADC3563) For the 10 and 25 MSPS device speed grades the sampling time is already set to TS/2. When powering down the DLL, the acquisition time will track the clock duty cycle (50% is recommended).

表 8-1. Acquisition time vs DLL PDN setting

SAMPLING CLOCK F_S (MSPS)	DLL PDN (0x11, D2)	ACQUISITION TIME (t_{ACQ})
65	0	T_S / 4

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表 8-1. Acquisition time vs DLL PDN setting (continued)

SAMPLING CLOCK F_S (MSPS)	DLL PDN (0x11, D2)	ACQUISITION TIME (t_{ACQ})
⩽ 40	1	T_S / 2

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8.3.3 Voltage Reference

The ADC356x provides three different options for supplying the voltage reference to the ADC. An external 1.6V reference can be directly connected to the VREF input; a voltage 1.2V reference can be connected to the REFBUF input using the internal gain buffer or the internal 1.2V reference can be enabled to generate a 1.6V reference voltage. For best performance, the reference noise should be filtered by connecting a 10 uF and a 0.1 uF ceramic bypass capacitor to the VREF pin. The internal reference circuitry of the ADC356x is shown in 图 8-17.

备注

The voltage reference mode can be selected using SPI writes or by using the REFBUF pin (default) as a control pin (Configuration using PINs only). If the REFBUF pin is not used for configuration, the REFBUF pin should be connected to AVDD (even though the REFBUF pin has a weak internal pullup to AVDD) and the voltage reference option has to be selected using the SPI interface.

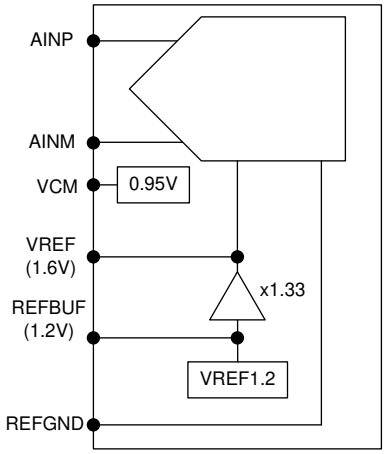

图 8-17. Different voltage reference options for ADC356x

8.3.3.1 Internal voltage reference

The 1.6V reference for the ADC can be generated internal using the on-chip 1.2V reference along with the internal gain buffer. A 10 uF and a 0.1 uF ceramic bypass capacitor (C_{VREF}) should be connected between the VREF and REFGND pins as close to the pins as possible.

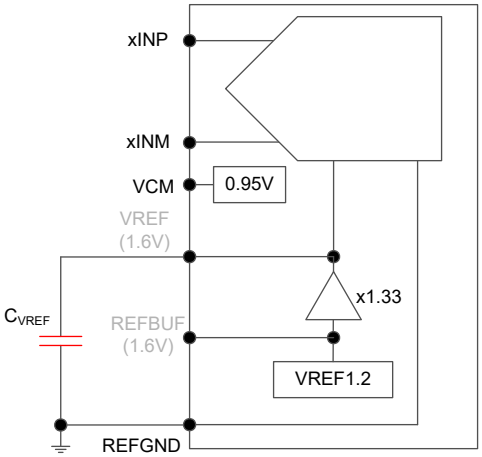

图 8-18. Internal reference

8.3.3.2 External voltage reference (VREF)

For highest accuracy and lowest temperature drift, the VREF input can be directly connected to an external 1.6V reference. A 10 uF and a 0.1 uF ceramic bypass capacitor (C_{VREF}) connected between the VREF and REFGND pins and placed as close to the pins as possible is recommended. The load current from the external reference is about 1mA.
Note: The internal reference is also used for other functions inside the device, therefore the reference amplifier should only be powered down in power down state but not during normal operation.

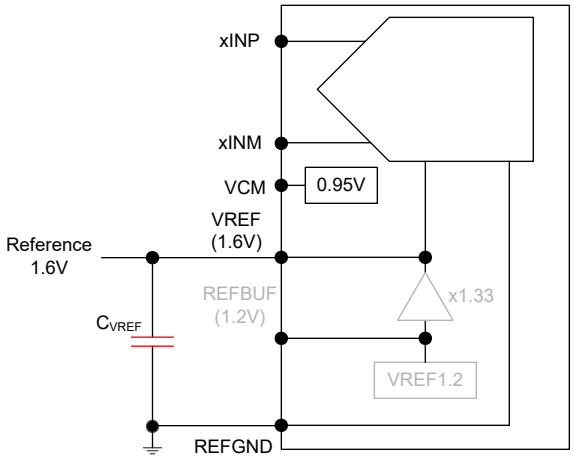

图 8-19. External 1.6V reference

8.3.3.3 External voltage reference with internal buffer (REFBUF)

The ADC356x is equipped with an on-chip reference buffer that also includes gain to generate the 1.6V reference voltage from an external 1.2V reference. A 10 uF and a 0.1 uF ceramic bypass capacitor (C_{VREF}) between the VREF and REFGND pins and a 10 uF and a 0.1 uF ceramic bypass capacitor between the REFBUF and REFGND pins are recommended. Both capacitors should be placed as close to the pins as possible. The load current from the external reference is less than 100uA.

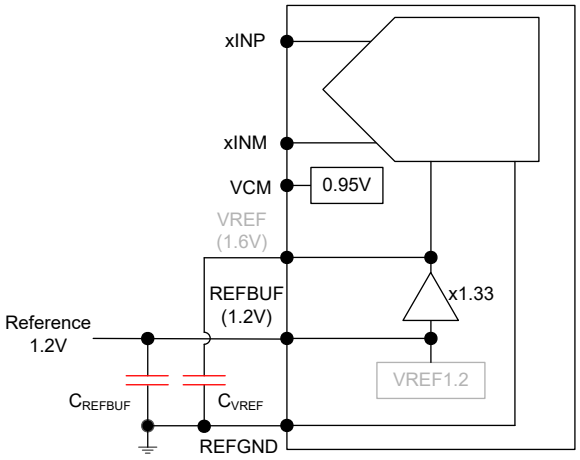

图 8-20. External 1.2V reference using internal reference buffer

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8.3.4 Digital Down Converter

The ADC356x includes an optional on-chip digital down conversion (DDC) decimation filter that can be enabled via SPI register settings. It supports complex decimation by 2, 4, 8, 16 and 32 using a digital mixer and a 32-bit numerically controlled oscillator (NCO) as shown in 图 8-21. Furthermore it supports a mode with real decimation where the complex mixer is bypassed (NCO should be set to 0 for lowest power consumption) and the digital filter acts as a low pass filter.

Internally the decimation filter calculations are performed with a 20-bit resolution in order to avoid any SNR degradation due to quantization noise. The Output Formatter truncates to the selected resolution prior to outputting the data on the digital interface.

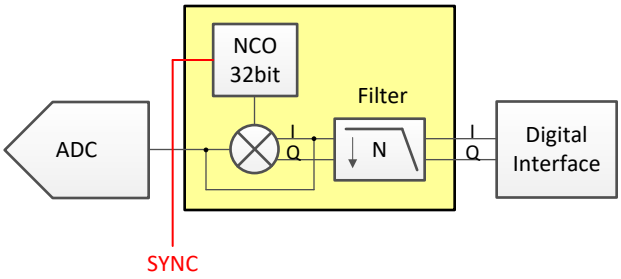

图 8-21. Internal Digital Decimation Filter

8.3.4.1 DDC MUX for Dual Band Decimation

The ADC356x contains a MUX in front of the digital decimation filter which allows the ADC to be connected to two digital down converters (see 图 8-22). This enables dual band complex decimation. The NCO of each digital down converter can be tuned to an independent frequency across the Nyquist zone as illustrated in the example in 图 8-23. The second DDC is output using the DB0/1 SLVDS interface.

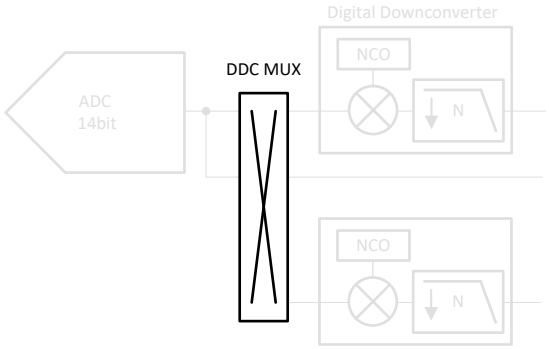

图 8-22. DDC MUX

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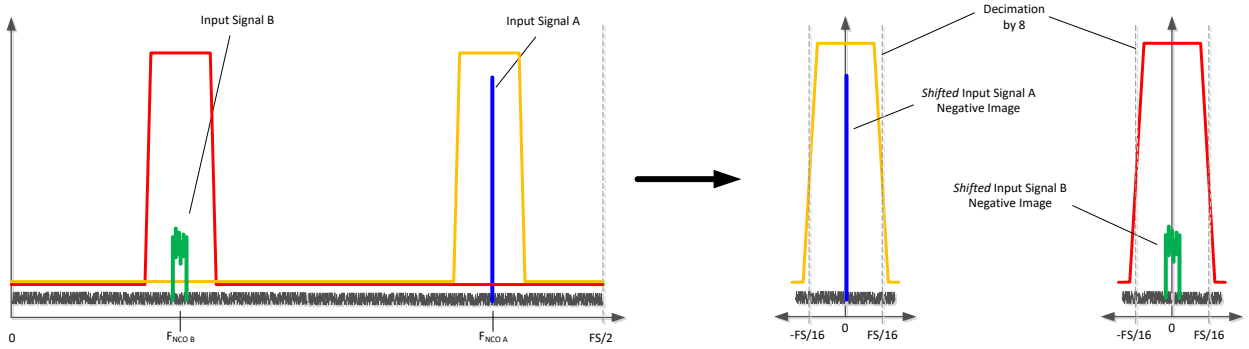

图 8-23. Complex Decimation (by 8) with dual band illustration

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8.3.4.2 Digital Filter Operation

The complex decimation operation is illustrated with an example in 图 8-24. First the input signal (and the negative image) are frequency shifted by the NCO frequency as shown on the left. Next a digital filter is applied (centered around 0 Hz) and the output data rate is decimated - in this example the output data rate $F_{S,OUT} = F_S/8$ with a Nyquist zone of $F_S/16$. During the complex mixing the spectrum (signal and noise) is split into real and complex parts and thus the amplitude is reduced by 6-dB. In order to compensate this loss, there is a 6-dB digital gain option in the decimation filter block that can be enabled via SPI write.

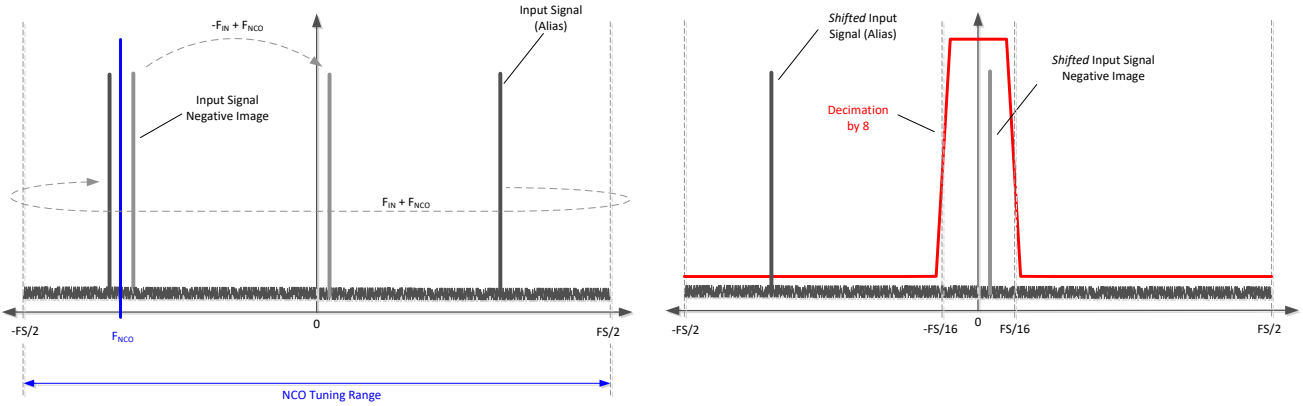

图 8-24. Complex decimation illustration

The real decimation operation is illustrated with an example in 图 8-25. There is no frequency shift happening and only the real portion of the complex digital filter is exercised. The output data rate is decimated - a decimation of 8 would result in an output data rate $F_{S,OUT} = F_S/8$ with a Nyquist zone of $F_S/16$.

During the real mixing the spectrum (signal and noise) amplitude is reduced by 3-dB. In order to compensate this loss, there is a 3-dB digital gain option in the decimation filter block that can be enabled via SPI write.

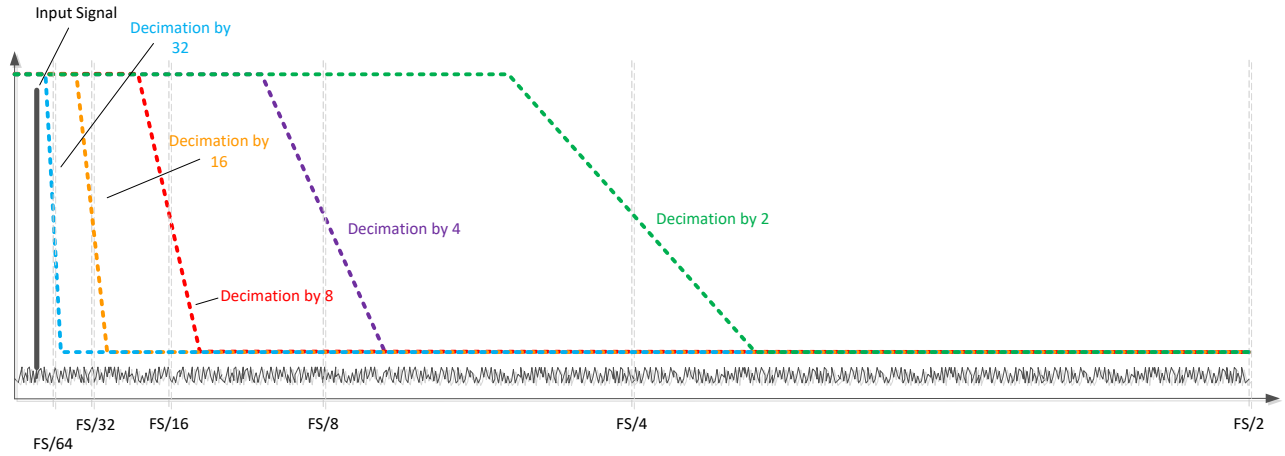

图 8-25. Real decimation illustration

8.3.4.3 FS/4 Mixing with Real Output

In this mode, the output after complex decimation gets mixed with FS/4 (FS = output data rate in this case). Instead of a complex output with the input signal centered around 0 Hz, the output is transmitted as a real output at twice the data rate and the signal is centered around FS/4 (Fout/4) as illustrated in 图 8-26.

In this example, complex decimation by 8 is used. The output data is transmitted as a real output with an output rate of Fout = FS'/4 (FS' = ADC sampling rate). The input signal is now centered around FS/4 (Fout/4) or FS'/16.

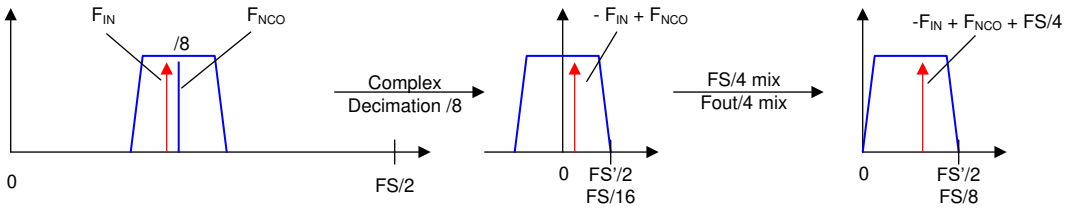

图 8-26. FS/4 Mixing with real output

8.3.4.4 Numerically Controlled Oscillator (NCO) and Digital Mixer

The decimation block is equipped with a 32-bit NCO and a digital mixer to fine tune the frequency placement prior to the digital filtering. The oscillator generates a complex exponential sequence of:

$$e^{j\omega n} \text{ (default) or } e^{-j\omega n} \quad (1)$$

where: frequency (ω) is specified as a signed number by the 32-bit register setting

The complex exponential sequence is multiplied with the real input from the ADC to mix the desired carrier to a frequency equal to f_{IN} + f_{NCO}. The NCO frequency can be tuned from $-F_S/2$ to $+F_S/2$ and is processed as a signed, 2s complement number. After programming a new NCO frequency, the MIXER RESTART register bit or SYNC pin has to be toggled for the new frequency to get active. Additionally the ADC356x provides the option via SPI to invert the mixer phase.

The NCO frequency setting is set by the 32-bit register value given and calculated as:

NCO frequency = 0 to + $F_S/2$: NCO = $f_{NCO} \times 2^{32} / F_S$

NCO frequency = $-F_S/2$ to 0: NCO = $(f_{NCO} + F_S) \times 2^{32} / F_S$

where:

- NCO = NCO register setting (decimal value)
- f_{NCO} = Desired NCO frequency (MHz)
- F_S = ADC sampling rate (MSPS)

The NCO programming is further illustrated with this example:

- ADC sampling rate F_S = 65 MSPS
- Input signal f_{IN} = 10 MHz
- Desired output frequency f_{OUT} = 0 MHz

For this example there are actually four ways to program the NCO and achieve the desired output frequency as shown in 表 8-2.

表 8-2. NCO value calculations example

Alias or negative image	f_{NCO}	NCO Value	Mixer Phase	Frequency translation for f_{OUT}
f_{IN} = – 10 MHz	f_{NCO} = 10 MHz	660764199	as is	$f_{OUT} = f_{IN} + f_{NCO}$ = – 10 MHz +10 MHz = 0 MHz
f_{IN} = 10 MHz	f_{NCO} = – 10 MHz	3634203097		$f_{OUT} = f_{IN} + f_{NCO}$ = 10 MHz + (– 10 MHz) = 0 MHz

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表 8-2. NCO value calculations example (continued)

Alias or negative image	f_{NCO}	NCO Value	Mixer Phase	Frequency translation for f_{OUT}
f_{IN} = 10 MHz	f_{NCO} = 10 MHz	660764199	inverted	$f_{OUT} = f_{IN} - f_{NCO}$ = 10 MHz – 10 MHz = 0 MHz
f_{IN} = – 10 MHz	f_{NCO} = – 10 MHz	3634203097		$f_{OUT} = f_{IN} - f_{NCO}$ = – 10 MHz – (– 10 MHz) = 0 MHz

8.3.4.5 Decimation Filter

The ADC356x supports complex decimation by 2, 4, 8, 16 and 32 with a pass-band bandwidth of ~ 80% and a stopband rejection of at least 85 dB. 表 8-3 gives an overview of the pass-band bandwidth of the different decimation settings with respect to ADC sampling rate F_S. In real decimation mode the output bandwidth is half of the complex bandwidth.

表 8-3. Decimation Filter Summary and Maximum Available Output Bandwidth

REAL/COMPLEX DECIMATION	DECIMATION SETTING N	OUTPUT RATE	OUTPUT BANDWIDTH	OUTPUT RATE (F_S = 65 MSPS)	OUTPUT BANDWIDTH (F_S = 65 MSPS)
Complex	2	F_S / 2 complex	0.8 × F_S / 2	32.5 MSPS complex	26 MHz
	4	F_S / 4 complex	0.8 × F_S / 4	16.25 MSPS complex	13 MHz
	8	F_S / 8 complex	0.8 × F_S / 8	8.125 MSPS complex	6.5 MHz
	16	F_S / 16 complex	0.8 × F_S / 16	4.0625 MSPS complex	3.25 MHz
	32	F_S / 32 complex	0.8 × F_S / 32	2.03125 MSPS complex	1.625 MHz
Real	2	F_S / 2 real	0.4 × F_S / 2	32.5 MSPS	13 MHz
	4	F_S / 4 real	0.4 × F_S / 4	16.25 MSPS	6.5 MHz
	8	F_S / 8 real	0.4 × F_S / 8	8.125 MSPS	3.25 MHz
	16	F_S / 16 real	0.4 × F_S / 16	4.0625 MSPS	1.625 MHz
	32	F_S / 32 real	0.4 × F_S / 32	2.03125 MSPS	0.8125 MHz

The decimation filter responses are normalized to the ADC sampling clock frequency F_S and illustrated in 图 8-28 to 图 8-37. They are interpreted as follows:

Each figure contains the filter pass-band, transition band(s) and alias or stop-band(s) as shown in 图 8-27. The x-axis shows the offset frequency (after the NCO frequency shift) normalized to the ADC sampling rate F_S.

For example, in the divide-by-4 complex setup, the output data rate is F_S / 4 complex with a Nyquist zone of F_S / 8 or 0.125 × F_S. The transition band (colored in blue) is centered around 0.125 × F_S and the alias transition band is centered at 0.375 × F_S. The stop-bands (colored in red), which alias on top of the pass-band, are centered at 0.25 × F_S and 0.5 × F_S. The stop-band attenuation is greater than 85 dB.

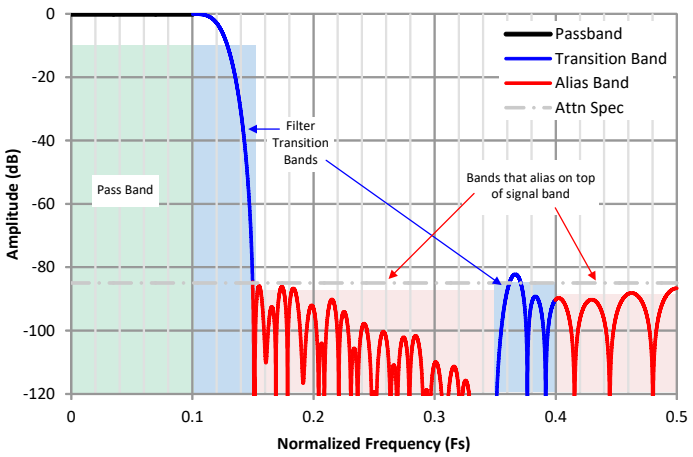

图 8-27. Interpretation of the Decimation Filter Plots

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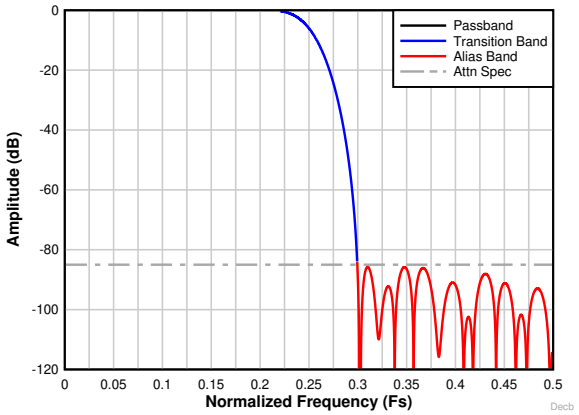

图 8-28. Decimation by 2 complex frequency response

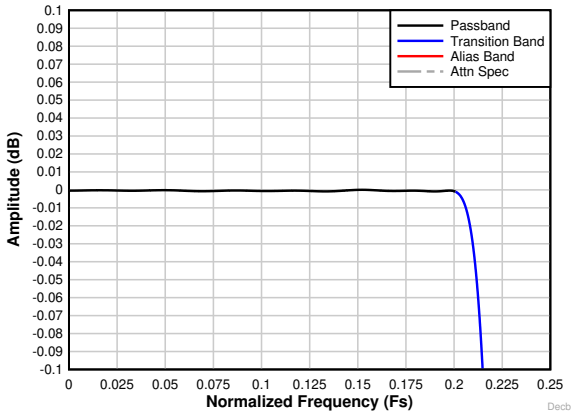

图 8-29. Decimation by 2 complex passband ripple response

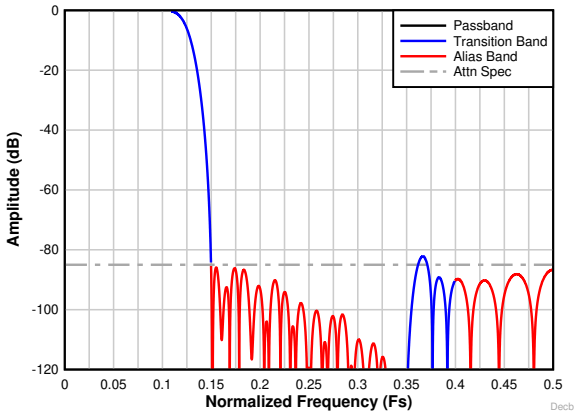

图 8-30. Decimation by 4 complex frequency response

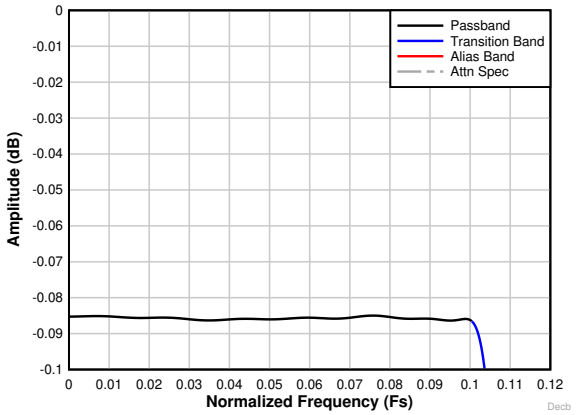

图 8-31. Decimation by 4 complex passband ripple response

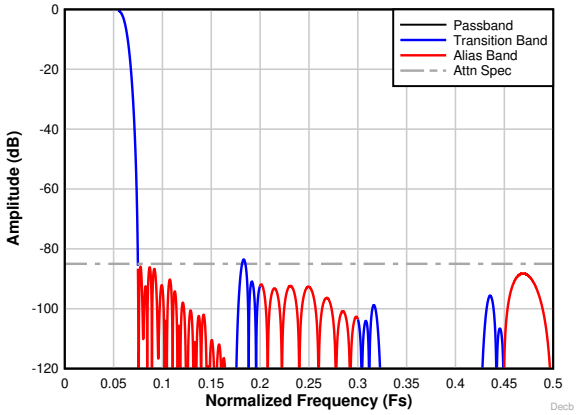

图 8-32. Decimation by 8 complex frequency response

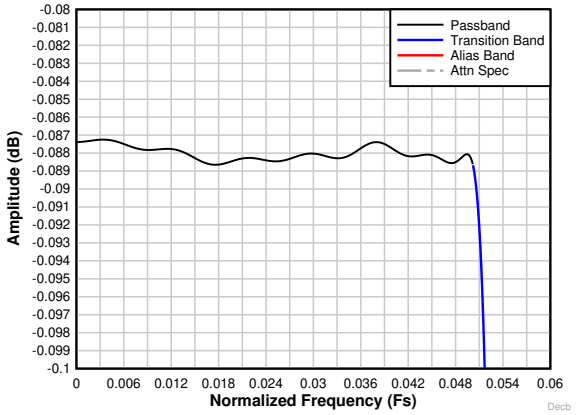

图 8-33. Decimation by 8 complex passband ripple response

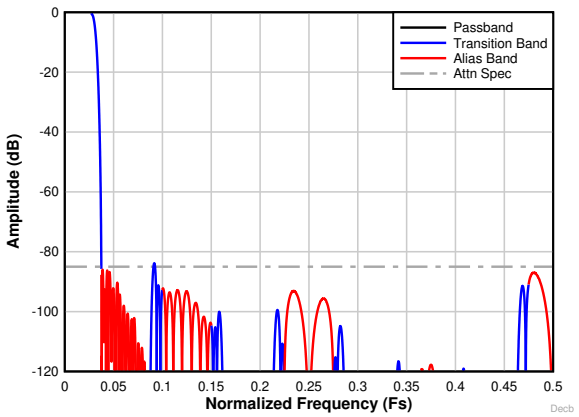

图 8-34. Decimation by 16 complex frequency response

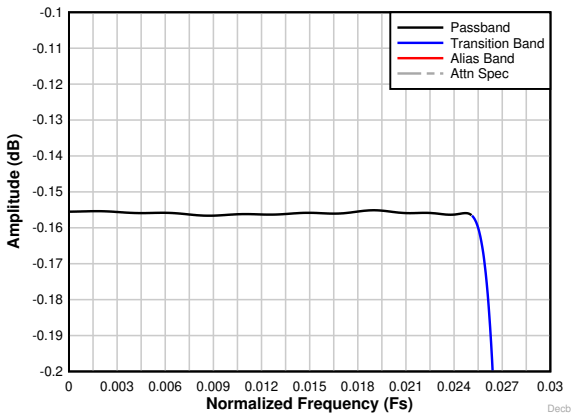

图 8-35. Decimation by 16 complex passband ripple response

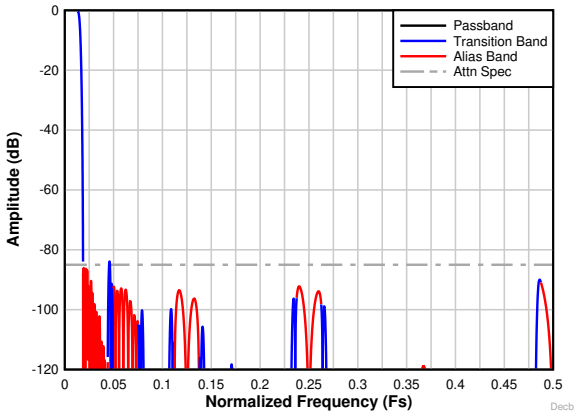

图 8-36. Decimation by 32 complex frequency response

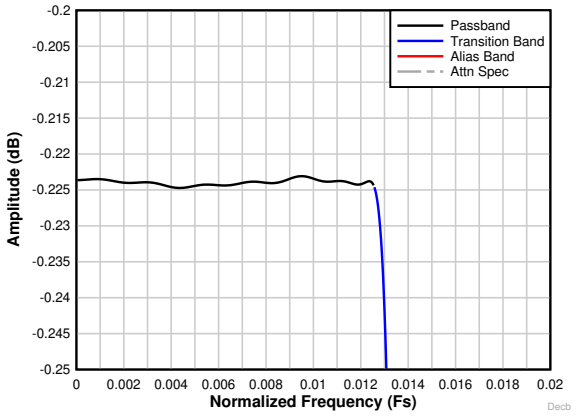

图 8-37. Decimation by 32 complex passband ripple response

8.3.4.6 SYNC

The PDN/SYNC pin can be used to synchronize multiple devices using an external SYNC signal. The PDN/SYNC pin can be configured via SPI (SYNC EN bit) from power down to synchronization functionality and is latched in by the rising edge of the sampling clock as shown in 图 8-38.

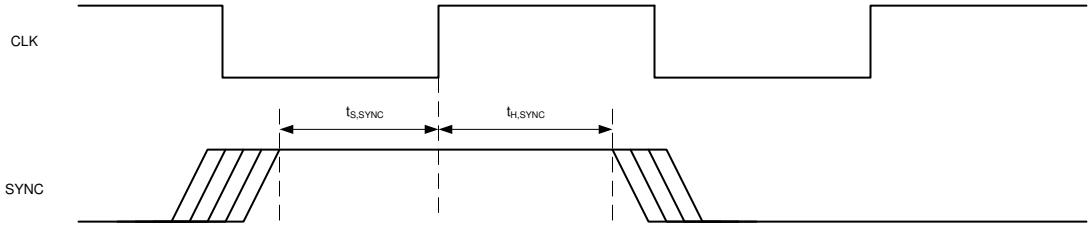

图 8-38. External SYNC timing diagram

The synchronization signal is only required when using the decimation filter - either using the SPI SYNC register or the PDN/SYNC pin. It resets internal clock dividers used in the decimation filter and aligns the internal clocks as well as I and Q data within the same sample. If no SYNC signal is given the internal clock dividers will not be synchronized, which can lead to a fractional delay across different devices. The SYNC signal also resets the NCO phase and loads the new NCO frequency (same as the MIXER RESTART bit).

When trying to resynchronize during operation, the SYNC toggle should occur at 64*K clock cycles, where K is an integer. This ensures phase continuity of the clock divider.

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8.3.4.7 Output Formatting with Decimation

When using decimation, the output data is formatted as shown in 图 8-39 (complex decimation) and 图 8-40 (real decimation).

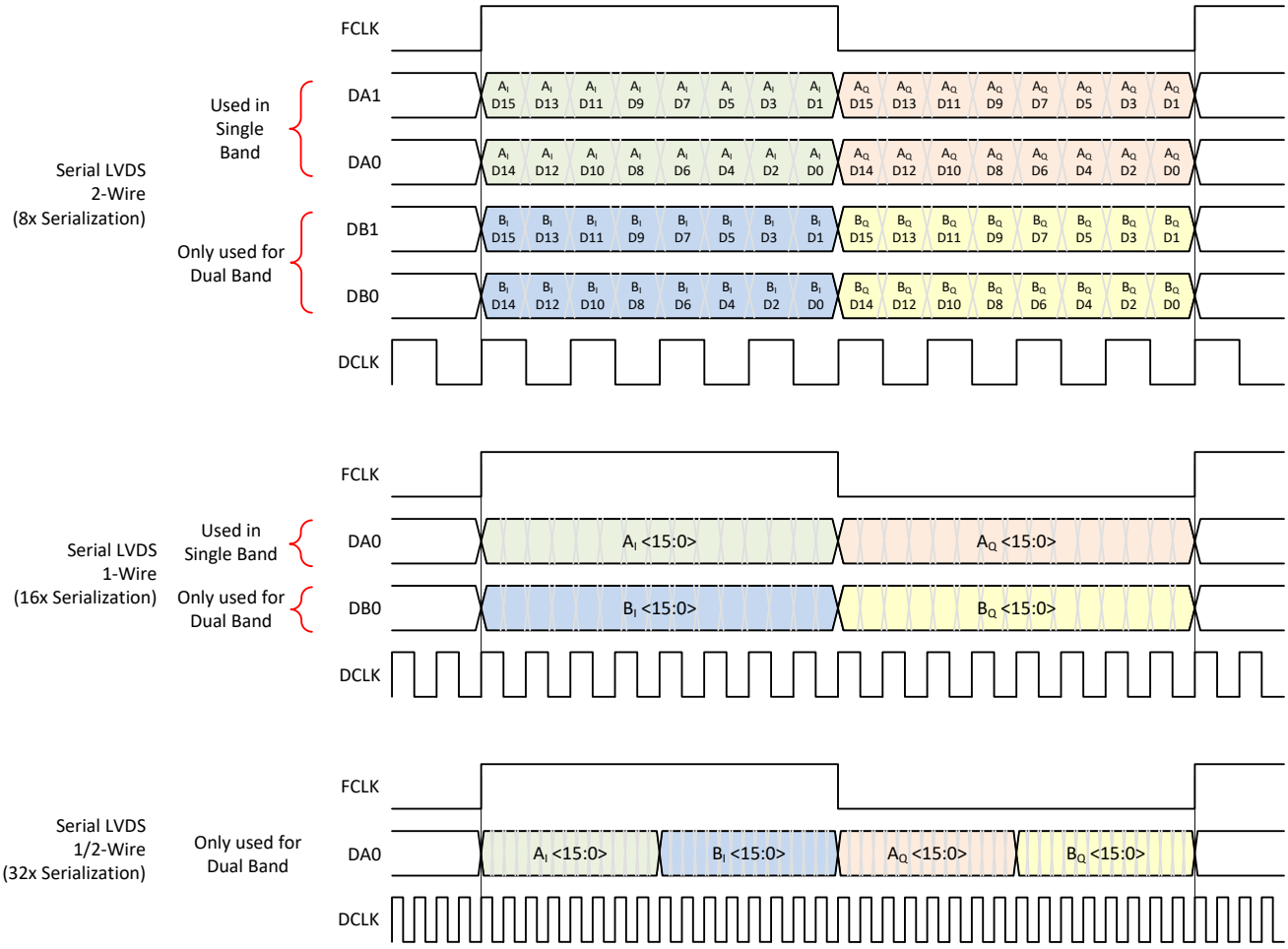

图 8-39. Output Data Format in Complex Decimation

表 8-4 illustrates the output interface data rate along with the corresponding DCLK/DCLKIN and FCLK frequencies based on output resolution (R), number of SLVDS lanes (L) and complex decimation setting (N).

Furthermore the table shows an actual lane rate example for the 2-, 1- and 1/2-wire interface, 16-bit output resolution and complex decimation by 4.

表 8-4. Serial LVDS Lane Rate Examples with Complex Decimation and 16-bit Output Resolution

DECIMATION SETTING	ADC SAMPLING RATE	OUTPUT RESOLUTION	# of WIRES	FCLK	DCLKIN, DCLK	DA/B0,1
N	F_S	R	L	F_S / N	[DA/B0,1] / 2	F_S x 2 x R / L / N
4	65 MSPS	16	2	16.25 MHz	130 MHz	260 MHz
			1		260 MHz	520 MHz
	62.5 MSPS		1/2	15.625 MHz	500 MHz	1000 MHz

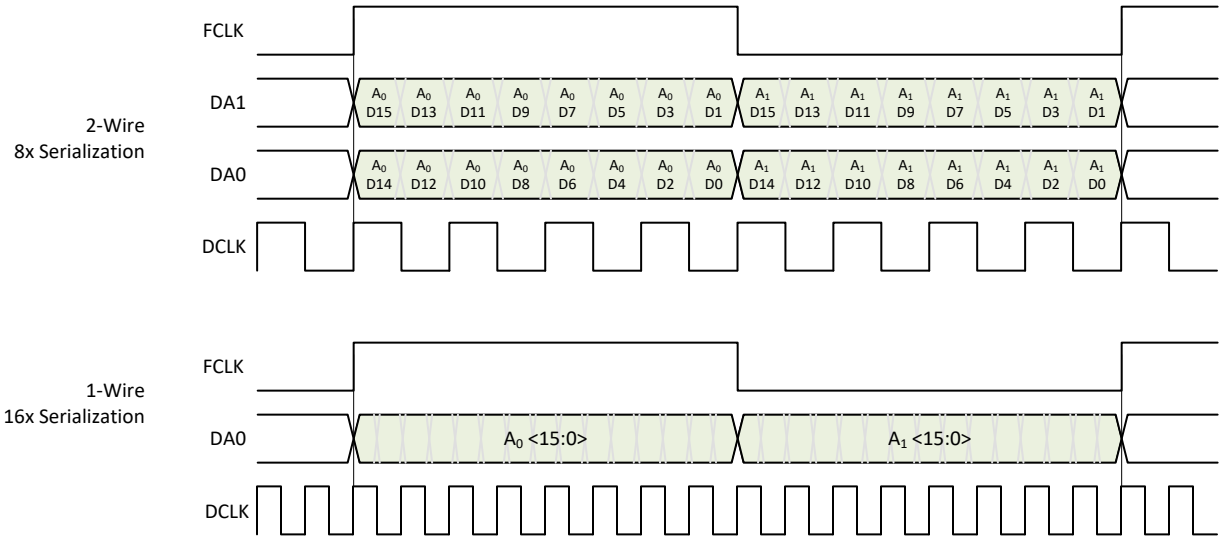

图 8-40. Output Data Format in Real Decimation

表 8-5 illustrates the output interface data rate along with the corresponding DCLK/DCLKIN and FCLK frequencies based on output resolution (R), number of SLVDS lanes (L) and real decimation setting (M).

Furthermore the table shows an actual lane rate example for the 2-, 1- and 1/2-wire interface, 16-bit output resolution and real decimation by 4.

表 8-5. Serial LVDS Lane Rate Examples with Real Decimation and 16-bit Output Resolution

DECIMATION SETTING	ADC SAMPLING RATE	OUTPUT RESOLUTION	# of WIRES	FCLK	DCLKIN, DCLK	DA/B0,1
M	F_S	R	L	F_S / M / 2 (L = 2) F_S / M (L = 1, 1/2)	[DA/B0,1] / 2	F_S x R / L / M
4	65 MSPS	16	2	8.125 MHz	65 MHz	130 MHz
			1	16.25 MHz	130 MHz	260 MHz

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8.3.5 Digital Interface

The serial LVDS interface supports the data output with 2-wire, 1-wire and 1/2-wire operation. The actual data output rate depends on the output resolution and number of lanes used.

The ADC356x requires an external serial LVDS clock input (DCLKIN), which is used to transmit the data out of the ADC along with the data clock (DCLK). The phase relationship between DCLKIN and the sampling clock is irrelevant but both clocks need to be frequency locked. The SLVDS interface is configured using SPI register writes.

8.3.5.1 Output Formatter

The digital output interface utilizes a flexible output bit mapper as shown in 图 8-41. The bit mapper takes the 16bit output directly from the ADC or from digital filter block and reformats it to a resolution of 14, 16, 18 or 20-bit. With parallel output format the maximum output resolution supported is 16-bit. With serial LVDS output the output serialization factor gets adjusted accordingly for 2-, 1- and 1/2-wire interface mode. The maximum output data rate can not be exceeded independently of output resolution and serialization factor.

With 14-bit output resolution the 2 LSBs are truncated.

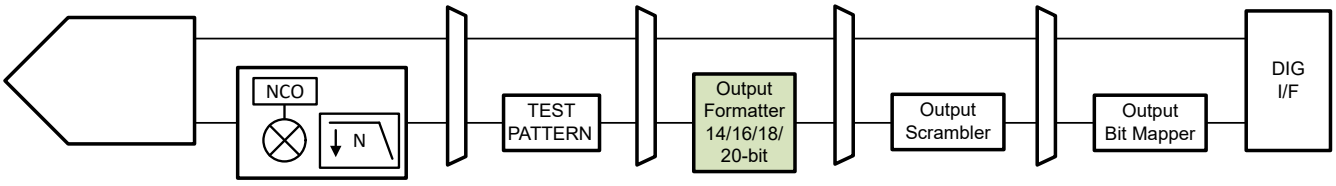

图 8-41. Interface output bit mapper

表 8-6 provides an overview for the resulting serialization factor depending on output resolution and output modes. Note that the DCLKIN frequency needs to be adjusted accordingly as well. Changing the output resolution to 14-bit, 2-wire mode for example would result in DCLKIN = F_S * 3.5 instead of * 4.

The output bit mapper can be used for bypass and decimation filter.

表 8-6. Serialization Factor vs Output Resolution for Different Output Modes

OUTPUT RESOLUTION	Interface	SERIALIZATION	FCLK	DCLKIN	DCLK	D0/D1
14-bit	2-Wire	7x	F_S/2	F_S* 3.5	F_S* 3.5	F_S* 7
	1-Wire	14x	F_S	F_S* 7	F_S* 7	F_S* 14
	1/2-Wire	28x	F_S	F_S* 14	F_S* 14	F_S* 28
16-bit (default)	2-Wire	8x	F_S/2	F_S* 4	F_S* 4	F_S* 8
	1-Wire	16x	F_S	F_S* 8	F_S* 8	F_S* 16
	1/2-Wire	32x	F_S	F_S* 16	F_S* 16	F_S* 32
18-bit	2-Wire	9x	F_S/2	F_S* 4.5	F_S* 4.5	F_S* 9
	1-Wire	18x	F_S	F_S* 9	F_S* 9	F_S* 18
	1/2-Wire	36x	F_S	F_S* 18	F_S* 18	F_S* 36
20-bit	2-Wire	10x	F_S/2	F_S* 5	F_S* 5	F_S* 10
	1-Wire	20x	F_S	F_S* 10	F_S* 10	F_S* 20
	1/2-Wire	40x	F_S	F_S* 20	F_S* 20	F_S* 40

The programming sequence to change the output interface and/or resolution from default settings is shown in Output Interface/Mode Configuration.

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8.3.5.2 Output Bit Mapper

The output bit mapper allows change to the output bit order for any selected interface mode.

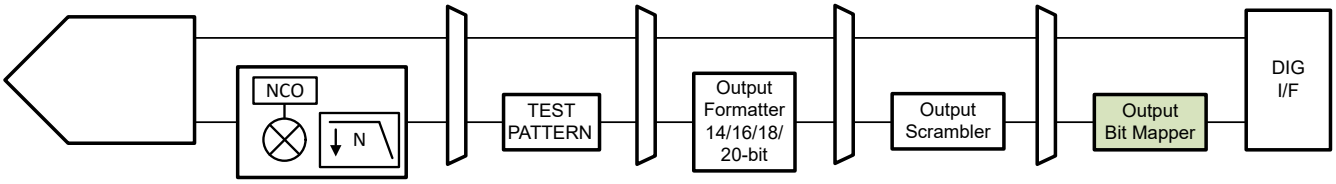

图 8-42. Output Bit Mapper

There is a two step process to change the output bit mapping and assemble the output data bus:

1. Both channel A and B can have up to 20-bit output. Each output bit of either channel has a unique identifier bit as shown in 表 8-7. The MSB starts with bit D19 – depending on output resolution chosen the LSB would be D6 (14-bit) to D0 (20-bit). The ‘previous sample’ is only needed in 2-w mode.
2. The bit mapper is then used to assemble the output sample. The following sections detail how to remap the serial output format.

表 8-7. Unique identifier of each data bit

Bit	Channel A		Channel B	
	Previous sample (2w only)	Current sample	Previous sample (2w only)	Current sample
D19 (MSB)	0x2D	0x6D	0x29	0x69
D18	0x2C	0x6C	0x28	0x68
D17	0x27	0x67	0x23	0x63
D16	0x26	0x66	0x22	0x62
D15	0x25	0x65	0x21	0x61
D14	0x24	0x64	0x20	0x60
D13	0x1F	0x5F	0x1B	0x5B
D12	0x1E	0x5E	0x1A	0x5A
D11	0x1D	0x5D	0x19	0x59
D10	0x1C	0x5C	0x18	0x58
D9	0x17	0x57	0x13	0x53
D8	0x16	0x56	0x12	0x52
D7	0x15	0x55	0x11	0x51
D6	0x14	0x54	0x10	0x50
D5	0x0F	0x4F	0x0B	0x4B
D4	0x0E	0x4E	0x0A	0x4A
D3	0x0D	0x4D	0x09	0x49
D2	0x0C	0x4C	0x08	0x48
D1	0x07	0x47	0x03	0x43
D0 (LSB)	0x06	0x46	0x02	0x42

In the serial output mode, a data bit (with unique identifier) needs to be assigned to each location within the serial output stream. There are a total of 40 addresses available per channel. Channel A spans from address 0x39 to 0x60 and channel B from address 0x61 to 0x88. When using complex decimation, the output bit mapper is applied to both the “I” and the “Q” sample.

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2-wire mode: in this mode both the current and the previous sample have to be used in the address space as shown in 图 8-43. The address order is different for 14/18-bit and 16/20-bit. Note: there are unused addresses between samples for resolution less than 20-bit (gray back ground), which can be ignored if not used.

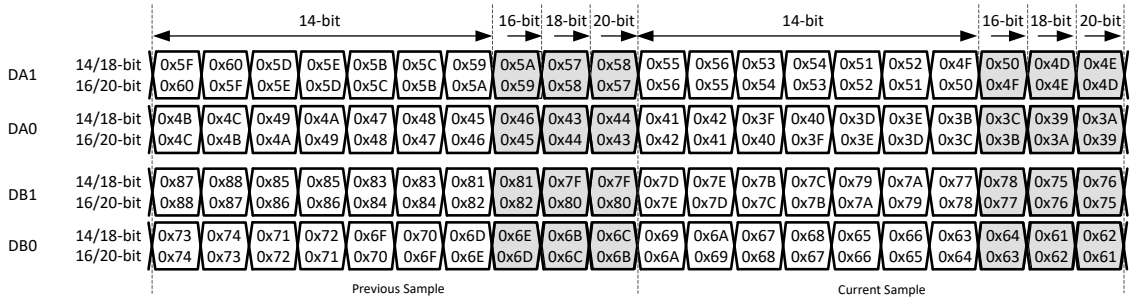

图 8-43. 2-wire output bit mapper

In the following example (图 8-44), the 16-bit 2-wire serial output is reordered to where lane DA1/DB1 carries the 8 MSB and lane DA0/DB0 carries 8 LSBs.

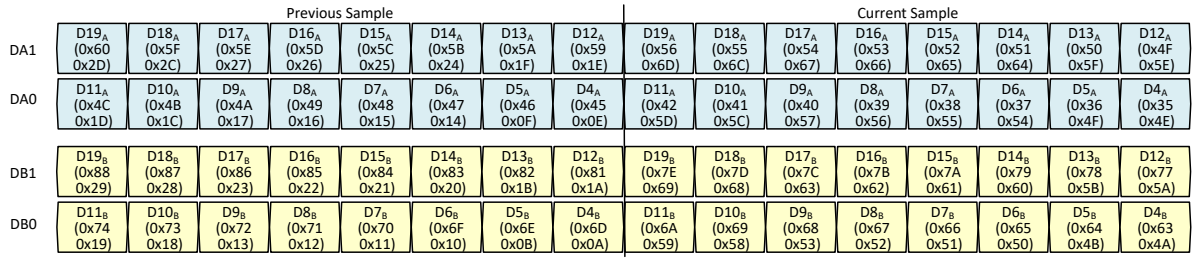

图 8-44. Example: 2-wire output bit mapping

1-wire mode: Only the ‘current’ sample needs to programmed in the address space. If desired, it can be duplicated on DA1/DB1 as well (using addresses shown below) in order to have a redundant output. Lane DA1/DB1 needs to be powered up in that case.

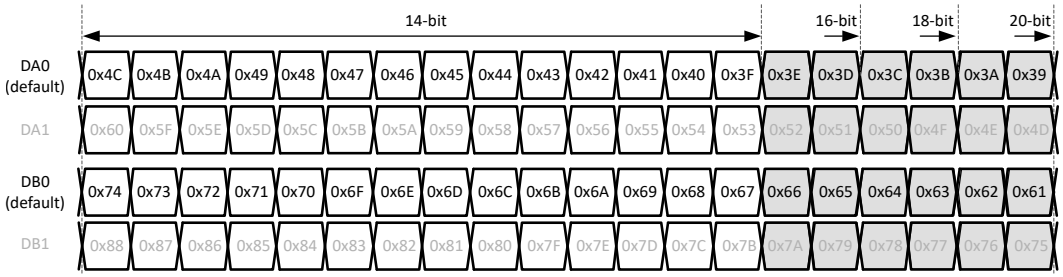

图 8-45. 1-wire output bit mapping

½-wire mode: The output is only lane DA0 and the sample order is programmed into the 40 addresses of chA (from 0x39 to 0x60). It covers 2 samples (one for chA, one for chB) as shown below. If desired, it can be duplicated on DB0 as well (using addresses shown 图 8-46) in order to have a redundant output. Lane DB0 needs to be powered up in that case.

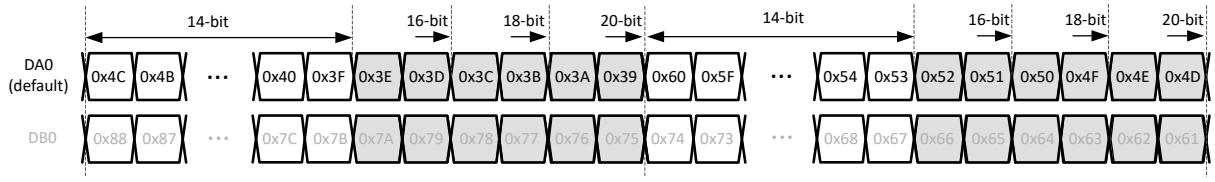

图 8-46. 1/2-wire output bit mapping

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8.3.5.3 Output Scrambler

The device includes an optional output scrambler feature. Scrambling is performed on each serial output lane independently. When enabled, the serial output bit stream is scrambled where each output bit is XOR-ed with 2 previous bits (k-14 and k-15) as shown in 图 8-47. For descrambling, note that the output bit mapper is located after the scrambler.

On the external receiver, the incoming serial data stream can be descrambled by XOR-ing each incoming bit with 2 previous bits (k-14 and k-15).

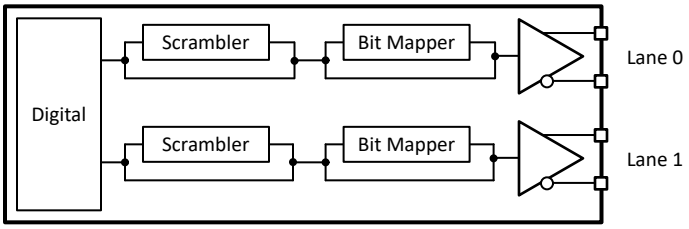

图 8-47. Output scrambling per lane

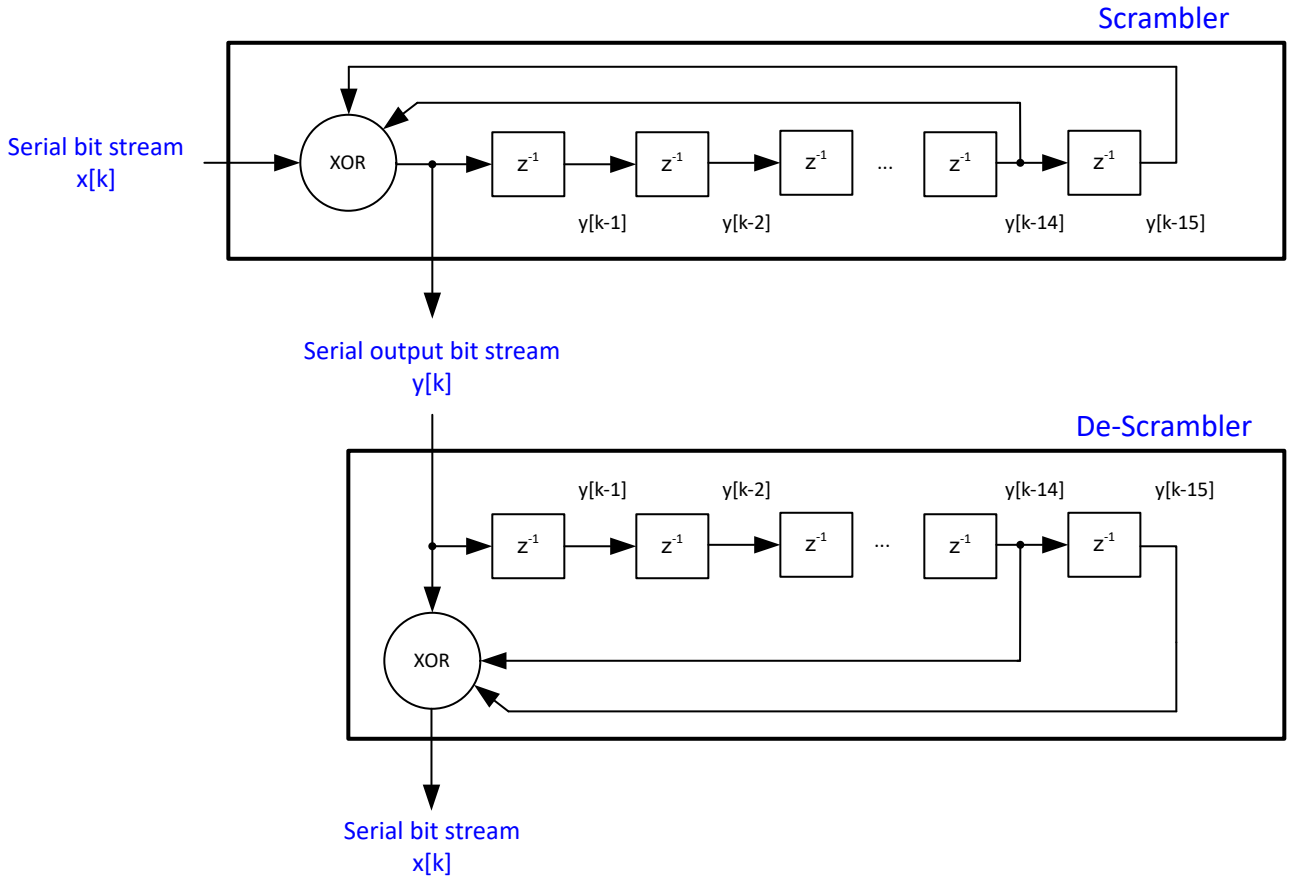

图 8-48. Output scrambler and descrambler operation

Scrambling is enabled by disabling digital bypass (register 0x24, D2) and enabling scrambling (register 0x22, D6).

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8.3.5.4 Output Interface/Mode Configuration

The following sequence summarizes all the relevant registers for changing the output interface and/or enabling the decimation filter. Steps 1 and 2 must come first since the E-Fuse load reset the SPI writes, the remaining steps can come in any order.

表 8-8. Configuration steps for changing interface or decimation

STEP	FEATURE	ADDRESS	DESCRIPTION
1	Output Interface	0x07	Select the output interface bit mapping depending on resolution and output interface. Output Resolution / 2-wire / 1-wire / 1/2-wire 14-bit / 0x2B / 0x6C / 0x8D 16-bit / 0x4B 18-bit / 0x2B 20-bit / 0x4B
2		0x13	Load the output interface bit mapping using the E-fuse loader (0x13, D0). Program register 0x13 to 0x01, wait ~ 1ms so that bit mapping is loaded properly followed by 0x13 0x00
3		0x19	Configure the FCLK frequency based on bypass/decimation and number of lanes used. Bypass/Dec / SLVDS / FCLK SRC (D7) / FCLK DIV (D4) / TOG FCLK (D0) Bypass/ Real Decimation / 2-wire / 0 / 1 / 0 1-wire / 0 / 0 / 0 1/2-wire / 0 / 0 / 0 Complex Decimation / 2-wire / 1 / 0 / 0 1-wire / 1 / 0 / 0 1/2-wire / 0 / 0 / 1
4		0x1B	Select the output interface resolution using the bit mapper (D5-D3).
5		0x20 0x21 0x22	Select the FCLK pattern for decimation for proper duty cycle output of the frame clock. Output Resolution / 2-wire / 1-wire / 1/2-wire Real Decimation: 14-bit / 0xFE000; 16-bit / 0xFF000; 18-bit / 0xFF800; 20-bit / 0xFFC00 — 2-wire: use default — 1/2-wire: use default Complex Decimation: 14-bit; 16-bit; 18-bit; 20-bit — 2-wire: use default — 1-wire: 0xFFFFF — 1/2-wire: 0xFFFFF
6		0x39..0x60 0x61..0x88	Change output bit mapping for chA and chB if desired. This works also with the default interface selection.
7		0x24 0x22	Enable scrambling
8	Decimation Filter	0x24	Enable the decimation filter
9		0x25	Configure the decimation filter
10		0x2A/B/C/D 0x31/2/3/4	Program the NCO frequency for complex decimation (can be skipped for real decimation)
11		0x27 0x2E	Configure the complex output data stream (set both bits to 0 for real decimation) SLVDS / OP-Order (D4) / Q-Delay (D3) 2-wire / 1 / 0 1-wire / 0 / 1 1/2-wire / 1 / 1
12		0x26	Set the mixer gain and toggle the mixer reset bit to update the NCO frequency.

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8.3.5.4.1 Configuration Example

The following is a step by step programming example to configure the ADC356x to complex decimation by 8 with 1-wire SLVDS and 16-bit output.

1. 0x07 (address) 0x6C (load bit mapper configuration for 16-bit output with 1-wire SLVDS)
2. 0x13 0x01, wait 1 ms, 0x13 0x00 (load e-fuse)
3. 0x19 0x80 (configure FCLK)
4. 0x1B 0x88 (select 16-bit output resolution)
5. 0x20 0xFF, 0x21 0xFF, 0x22 0x0F (configure FCLK pattern)
6. 0x24 0x06 (enable decimation filter)
7. 0x25 0x30 (configure complex decimation by 8)
8. 0x2A/B/C/D and 0x31/32/33/34 (program NCO frequency)
9. 0x27/0x2E 0x08 (configure Q-delay register bit)
10. 0x26 0xAA, 0x26 0x88 (set digital mixer gain to 6-dB and toggle the mixer update)

8.3.5.5 Output Data Format

The output data can be configured to two's complement (default) or offset binary formatting using SPI register writes (register 0x8F and 0x92). 表 8-9 provides an overview for minimum and maximum output codes for the two formatting options. The actual output resolution is set by the output bit mapper.

表 8-9. Overview of minimum and maximum output codes vs output resolution for different formatting

	Two's Complement (default)				Offset Binary			
RESOLUTION (BIT)	**14**	**16**	**18**	**20**	**14**	**16**	**18**	**20**
$V_{IN,MAX}$	0x1FFF	0x7FFF	0x1FFFF	0x7FFFF	0x3FFF	0xFFFF	0x3FFFF	0xFFFFF
0	0x0000		0x00000		0x2000	0x8000	0x20000	0x80000
$V_{IN,MIN}$	0x2000	0x8000	0x20000	0x80000	0x0000		0x00000	

8.3.6 Test Pattern

In order to enable in-circuit testing of the digital interface, the following test patterns are supported and enabled via SPI register writes (0x14/0x15/0x16). The test pattern generator is located after the decimation filter as shown in 图 8-49. In decimation mode (real and complex), the test patterns replace the output data of the DDC - however channel A controls the test patterns for both channels.

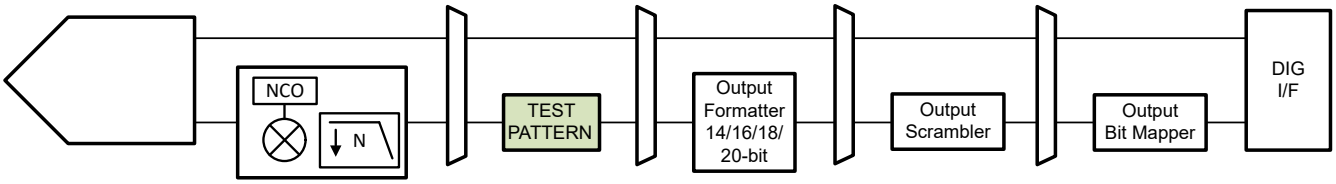

图 8-49. Test Pattern Generator

- RAMP Pattern: The step size needs to be configured in the CUSTOM PAT register according to the native resolution of the ADC. When selecting a higher output resolution then the additional LSBs will still be 0 in RAMP pattern mode.
  - 00001: 18-bit output resolution
  - 00100: 16-bit output resolution
  - 10000: 14-bit output resolution
- Custom Pattern: Configured in the CUSTOM PAT register

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8.4 Device Functional Modes

8.4.1 Normal operation

In normal operating mode, the entire ADC full scale range gets converted to a digital output with 16-bit resolution. The output is available in as little as 1 clock cycle on the digital SLVDS outputs.

8.4.2 Power Down Options

A global power down mode can be enabled via SPI as well as using the power down pin (PDN/SYNC). There is an internal pull-down 21kΩ resistor on the PDN/SYNC input pin and the pin is active high - so the pin needs to be pulled high externally to enter global power down mode.

The SPI register map provides the capability to enable/disable individual blocks directly or via PDN pin mask in order to trade off power consumption vs wake up time.

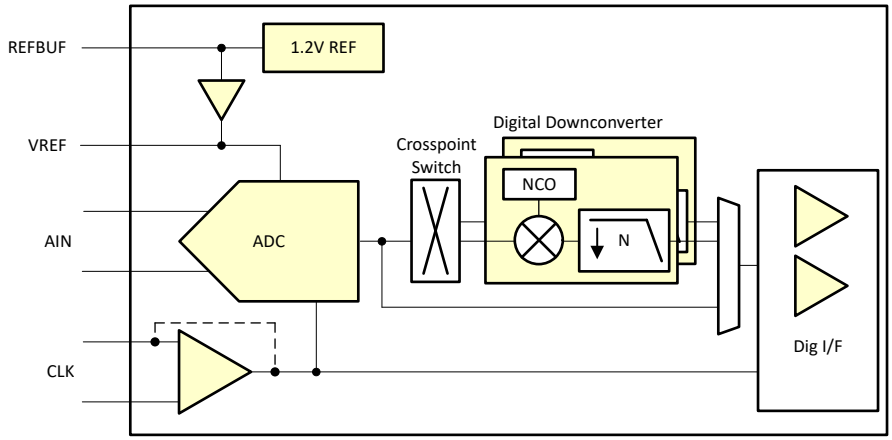

图 8-50. Power Down Configurations

表 8-10. Overview of Power Down Options

Function/ Register	PDN via SPI	Mask for Global PDN	Feature - Default	Power Impact	Wake-up time	Comment
ADC	Yes	-	Enabled			ADC is included in Global PDN automatically
Reference gain amplifier	Yes	Yes	Enabled	~ 0.4 mA	~3 us	
Internal 1.2V reference	Yes		External ref	~ 1-3.5 mA	~3 ms	Internal/external reference selection is available through SPI and REFBUF pin.
Clock buffer	Yes		Differential clock	~ 1 mA	n/a	Single ended clock input saves ~ 1mA compared to differential. Some programmability is available through the REFBUF pin.
Output interface drivers	Yes	-	Enabled	varies	n/a	Depending on output interface mode, unused output drivers can be powered down for maximum power savings
Decimation filter	Yes	-	Disabled	see electrical table	n/a	

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8.5 Programming

The device is primarily configured and controlled using the serial programming interface (SPI) however it can operate in a default configuration without requiring the SPI interface. Furthermore the power down function as well as internal/external reference configuration is possible via pin control (PDN/SYNC and REFBUF pin).

备注

The power down command (via PIN or SPI) only goes in effect with the ADC sampling clock present.

After initial power up, the default operating configuration for each device is shown in 表 8-11.

表 8-11. Default device configuration after power up

FEATURE	ADC3561	ADC3562	ADC3563
Signal Input	Differential		
Auto-Zero	Enabled	Enabled	Disabled
Clock Input	Differential		
Reference	External		
Decimation	DDC bypass		
Interface	1-wire	1-wire	2-wire
Output Format	2s complement		

8.5.1 Configuration using PINs only

The ADC voltage reference can be selected using the REFBUF pin. Even though there is an internal 100 kΩ pull-up resistor to AVDD, the REFBUF pin should be set to a voltage externally and not left floating. When using a voltage divider to set the REFBUF voltage (R1 and R2 in 图 8-51), resistor values < 5 kΩ should be used.

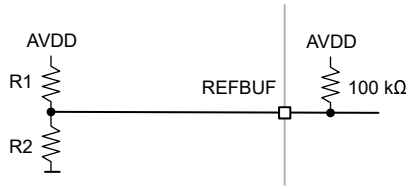

图 8-51. Configuration of external voltage on REFBUF pin

表 8-12. REFBUF voltage levels control voltage reference selection

REFBUF VOLTAGE	VOLTAGE REFERENCE OPTION	CLOCKING OPTION
> 1.7 V (Default)	External reference	Differential clock input
1.2 V (1.15-1.25V)	External 1.2V input on REFBUF pin using internal gain buffer	Differential clock input
0.5 - 0.7V	Internal reference	Differential clock input
< 0.1V	Internal reference	Single ended clock input

8.5.2 Configuration using the SPI interface

The device has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock) and SDIO (serial interface data input/output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data input are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The interface can function with SCLK frequencies from 12 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

8.5.2.1 Register Write

The internal registers can be programmed following these steps:

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1. Drive the SEN pin low
2. Set the R/W bit to 0 (bit A15 of the 16-bit address) and bits A[14:12] in address field to 0.
3. Initiate a serial interface cycle by specifying the address of the register (A[11:0]) whose content is written and
4. Write the 8-bit data that are latched in on the SCLK rising edges

图 8-52 show the timing requirements for the serial register write operation.

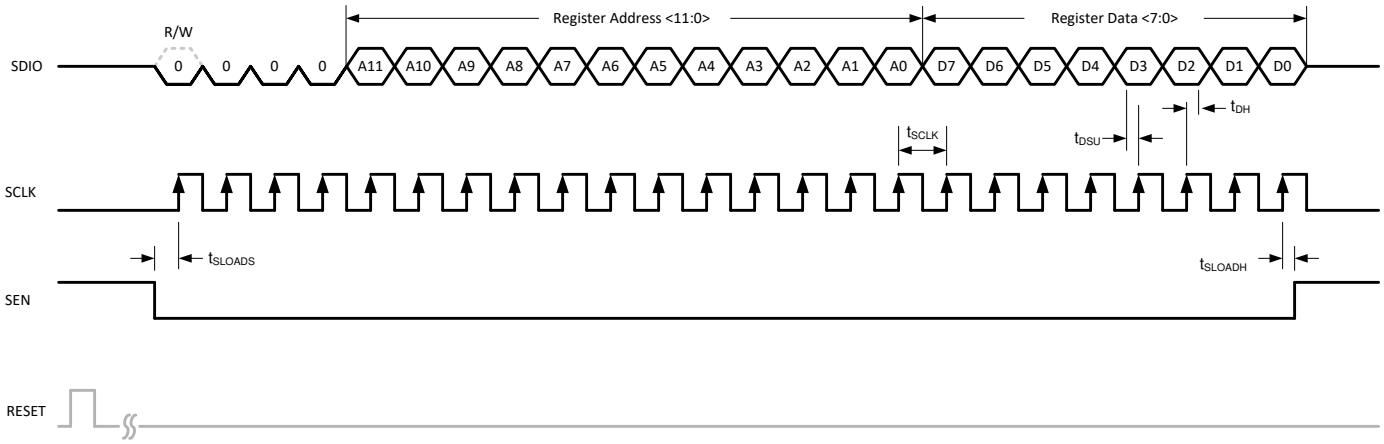

图 8-52. Serial Register Write Timing Diagram

8.5.2.2 Register Read

The device includes a mode where the contents of the internal registers can be read back using the SDIO pin. This readback mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

1. Drive the SEN pin low
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers. Set A[14:12] in address field to 0.
3. Initiate a serial interface cycle specifying the address of the register (A[11:0]) whose content must be read
4. The device launches the contents (D[7:0]) of the selected register on the SDIO pin on SCLK falling edge
5. The external controller can capture the contents on the SCLK rising edge

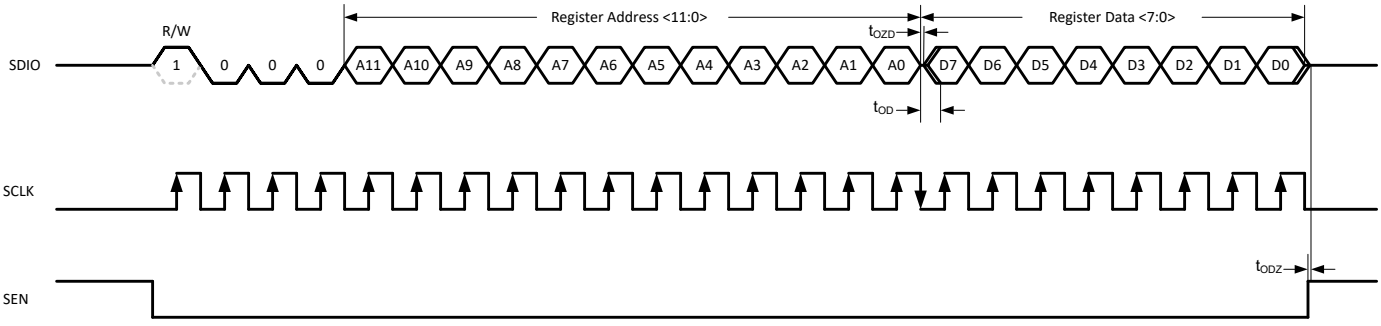

图 8-53. Serial Register Read Timing Diagram

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8.6 Register Maps

表 8-13. Register Map Summary

REGISTER ADDRESS	REGISTER DATA							
A[11:0]	D7	D6	D5	D4	D3	D2	D1	D0
0x00	0	0	0	0	0	0	0	RESET
0x07	OP IF MAPPER			0	OP IF EN	OP IF SEL		
0x08	0	0	PDN CLKBUF	PDN REFAMP	0	PDN A	1	PDN GLOBAL
0x09	0	0	PDN FCLKOUT	PDN DCLKOUT	PDN DA1	PDN DA0	PDN DB1	PDN DB0
0x0D	0	0	0	0	MASK CLKBUF	MASK REFAMP	MASK BG DIS	0
0x0E	SYNC PIN EN	SPI SYNC	SPI SYNC EN	0	REF CTRL	REF SEL		SE CLK EN
0x11	0	0	SE A	0	0	DLL PDN	0	AZ EN
0x13	0	0	0	0	0	0	0	E-FUSE LD
0x14	CUSTOM PAT [7:0]							
0x15	CUSTOM PAT [15:8]							
0x16	TEST PAT B			TEST PAT A			CUSTOM PAT [17:16]	
0x19	FCLK SRC	0	0	FCLK DIV	0	0	0	TOG FCLK
0x1A	0	LVDS ½ SWING	0	0	0	0	0	0
0x1B	MAPPER EN	20B EN	BIT MAPPER RES			0	0	0
0x1E	0	0	0	0	LVDS DATA DEL		LVDS DCLK DEL	
0x20	FCLK PAT [7:0]							
0x21	FCLK PAT [15:8]							
0x22	0	SCR EN	0	0	FCLK PAT [19:16]			
0x24	0	0	0	DDC MUX		DIG BYP	DDC EN	0
0x25	DDC MUX EN	DECIMATION			REAL OUT	0	0	MIX PHASE
0x26	MIX GAIN A		MIX RES A	FS/4 MIX A	MIX GAIN B		MIX RES B	FS/4 MIX B
0x27	0	0	0	OP ORDER A	Q-DEL A	FS/4 MIX PH A	0	0
0x2A	NCO A [7:0]							
0x2B	NCO A [15:8]							
0x2C	NCO A [23:16]							
0x2D	NCO A [31:24]							
0x2E	0	0	0	OP ORDER B	Q-DEL B	FS/4 MIX PH B	0	0
0x31	NCO B [7:0]							
0x32	NCO B [15:8]							
0x33	NCO B [23:16]							
0x34	NCO B [31:24]							
0x39..0x60	OUTPUT BIT MAPPER CHA							
0x61..0x88	OUTPUT BIT MAPPER CHB							
0x8F	0	0	0	0	0	0	FORMAT A	0
0x92	0	0	0	0	0	0	FORMAT B	0

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8.6.1 Detailed Register Description

图 8-54. Register 0x00

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	RESET
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-14. Register 0x00 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0	Must write 0
0	RESET	R/W	0	This bit resets all internal registers to the default values and self clears to 0.

图 8-55. Register 0x07

7	6	5	4	3	2	1	0
OP IF VAR			0	OP IF EN	OP IF SEL		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-15. Register 0x07 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	OP IF MAPPER	R/W	000	Output interface mapper. This register contains the proper output interface bit mapping for the different interfaces. The interface bit mapping is internally loaded from e-fuses and also requires a fuse load command to go into effect (0x13, D0). Register 0x07 along with the E-Fuse Load (0x13, D0) needs to be loaded first in the programming sequence since the E-Fuse load resets the SPI writes. After initial reset the default output interface variant is loaded automatically from fuse internally. However when reading back this register reads 000 until a value is written using SPI. 001: 2-wire, 18 and 14-bit 010: 2-wire, 16-bit 011: 1-wire 100: 0.5-wire others: not used
4	0	R/W	0	Must write 0
3	OP IF EN	R/W	0	Enables changing the default output interface mode (D2-D0).
2-0	OP IF SEL	R/W	000	Selection of the output interface mode. OP IF EN (D3) needs to be enabled also. After initial reset the default output interface is loaded automatically from fuse internally. However when reading back this register reads 000 until a value is written using SPI. 011: 2-wire 100: 1-wire 101: 0.5-wire others: not used

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图 8-56. Register 0x08

7	6	5	4	3	2	1	0
0	0	PDN CLKBUF	PDN REFAMP	0	PDN A	1	PDN GLOBAL
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-16. Register 0x08 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0
5	PDN CLKBUF	R/W	0	Powers down sampling clock buffer 0: Clock buffer enabled 1: Clock buffer powered down
4	PDN REFAMP	R/W	0	Powers down internal reference gain amplifier 0: REFAMP enabled 1: REFAMP powered down
3	0	R/W	0	Must write 0
2	PDN A	R/W	0	Powers down ADC channel A 0: ADC channel A enabled 1: ADC channel A powered down
1	1	R/W	1	Must write 1
0	PDN GLOBAL	R/W	0	Global power down via SPI 0: Global power disabled 1: Global power down enabled. Power down mask (register 0x0D) determines which internal blocks are powered down.

图 8-57. Register 0x09

7	6	5	4	3	2	1	0
0	0	PDN FCLKOUT	PDN DCLKOUT	PDN DA0	PDN DA1	PDN DB0	PDN DB1
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-17. Register 0x09 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0
5	PDN FCLKOUT	R/W	0	Powers down frame clock (FCLK) LVDS output buffer 0: FCLK output buffer enabled 1: FCLK output buffer powered down
4	PDN DCLKOUT	R/W	0	Powers down DCLK LVDS output buffer 0: DCLK output buffer enabled 1: DCLK output buffer powered down
3	PDN DA1	R/W	1	Powers down LVDS output buffer for channel A, lane 1. Powered down automatically in 1-wire and 1/2-wire mode. 0: DA1 LVDS output buffer enabled 1: DA1 LVDS output buffer powered down
2	PDN DA0	R/W	1	Powers down LVDS output buffer for channel A, lane 0. 0: DA0 LVDS output buffer enabled 1: DA0 LVDS output buffer powered down.
1	PDN DB1	R/W	0	Powers down LVDS output buffer for channel B, lane 1. Powered down by default. Powered down automatically in 1-wire and 1/2-wire mode. 0: DB1 LVDS output buffer enabled 1: DB1 LVDS output buffer powered down
0	PDN DB0	R/W	0	Powers down LVDS output buffer for channel B, lane 0. Powered down by default. Powered down automatically in 1/2-wire mode. 0: DB0 LVDS output buffer enabled 1: DB0 LVDS output buffer powered down

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图 8-58. Register 0x0D (PDN GLOBAL MASK)

7	6	5	4	3	2	1	0
0	0	0	0	MASK CLKBUF	MASK REFAMP	MASK BG DIS	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-18. Register 0x0D Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0	Must write 0
3	MASK CLKBUF	R/W	0	Global power down mask control for sampling clock input buffer. 0: Clock buffer will get powered down when global power down is exercised. 1: Clock buffer will NOT get powered down when global power down is exercised.
2	MASK REFAMP	R/W	0	Global power down mask control for reference amplifier. 0: Reference amplifier will get powered down when global power down is exercised. 1: Reference amplifier will NOT get powered down when global power down is exercised.
1	MASK BG DIS	R/W	0	Global power down mask control for internal 1.2V bandgap voltage reference. Setting this bit reduces power consumption in global power down mode but increases the wake up time. See the power down option overview. 0: Internal 1.2V bandgap voltage reference will NOT get powered down when global power down is exercised. 1: Internal 1.2V bandgap voltage reference will get powered down when global power down is exercised.
0	0	R/W	0	Must write 0

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图 8-59. Register 0x0E

7	6	5	4	3	2	1	0
SYNC PIN EN	SPI SYNC	SPI SYNC EN	0	REF CTL	REF SEL		SE CLK EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-19. Register 0x0E Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC PIN EN	R/W	0	This bit controls the functionality of the SYNC/PDN pin. 0: SYNC/PDN pin exercises global power down mode when pin is pulled high. 1: SYNC/PDN pin issues the SYNC command when pin is pulled high.
6	SPI SYNC	R/W	0	Toggling this bit issues the SYNC command using the SPI register write. SYNC using SPI must be enabled as well (D5). This bit doesn't self reset to 0. 0: Normal operation 1: SYNC command issued.
5	SPI SYNC EN	R/W	0	This bit enables synchronization using SPI instead of the SYNC/PDN pin. 0: Synchronization using SPI register bit disabled. 1: Synchronization using SPI register bit enabled.
4	0	R/W	0	Must write 0
3	REF CTL	R/W	0	This bit determines if the REFBUF pin controls the voltage reference selection or the SPI register (D2-D1). 0: The REFBUF pin selects the voltage reference option. 1: Voltage reference is selected using SPI (D2-D1) and single ended clock using D0.
2-1	REF SEL	R/W	00	Selects of the voltage reference option. REF CTRL (D3) must be set to 1. 00: Internal reference 01: External voltage reference (1.2V) using internal reference buffer (REFBUF) 10: External voltage reference 11: not used
0	SE CLK EN	R/W	0	Selects single ended clock input and powers down the differential sampling clock input buffer. REF CRTL (D3) must be set to 1. 0: Differential clock input 1: Single ended clock input

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图 8-60. Register 0x11

7	6	5	4	3	2	1	0
0	0	SE A	0	0	DLL PDN	0	AZ EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-20. Register 0x11 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0
5	SE A	R/W	0	This bit enables single ended analog input, channel A. In this mode the SNR reduces by 3-dB. 0: Differential input 1: Single ended input
4-3	0	R/W	0	Must write 0
2	DLL PDN	R/W	0	This register applies ONLY to the ADC3563. It powers down the internal DLL, which is used to adjust the sampling time. This register must only be enabled when operating at sampling rates below 40 MSPS. When DLL PDN bit is enabled the sampling time is directly dependent on sampling clock duty cycle (with a 50/50 duty the sampling time is $T_S/2$). 0: Sampling time is $T_S/4$ 1: Sampling time is $T_S/2$ (only for sampling rates below 40 MSPS).
1	0	R/W	0	Must write 0
0	AZ EN	R/W	0	This bit enables the internal auto-zero circuitry. It is enabled by default for the ADC3561/62 and disabled for the ADC3563. ADC3561/62: 0: Auto-zero enabled 1: Auto-zero disabled ADC3563: 0: Auto-zero disabled 1: Auto-zero enabled

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图 8-61. Register 0x13

7	6	5	4	3	2	1	0
0	0	0	0	0	0		E-FUSE LD
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-21. Register 0x13 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0	Must write 0
0	E-FUSE LD	R/W	0	This register bit loads the internal bit mapping for different interfaces. After setting the interface in register 0x07, this E-FUSE LD bit needs to be set to 1 and reset to 0 for loading to go into effect. Register 0x07 along with the E-Fuse Load (0x13, D0) needs to be loaded first in the programming sequence since the E-Fuse load resets the SPI writes. 0: E-FUSE LOAD set 1: E-FUSE LOAD reset

图 8-62. Register 0x14/15/16

7	6	5	4	3	2	1	0
CUSTOM PAT [7:0]							
CUSTOM PAT [15:8]							
TEST PAT B			TEST PAT A			CUSTOM PAT [17:16]	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-22. Register 0x14/15/16 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CUSTOM PAT [17:0]	R/W	00000000	This register is used for two purposes: • It sets the constant custom pattern starting from MSB • It sets the RAMP pattern increment step size. 00001: Ramp pattern for 18-bit ADC 00100: Ramp pattern for 16-bit ADC 10000: Ramp pattern for 14-bit ADC
7-5	TEST PAT B	R/W	000	Enables test pattern output mode for channel B (NOTE: The test pattern is set prior to the bit mapper and is based on native resolution of the ADC starting from the MSB). These work in either output format. 000: Normal output mode (test pattern output disabled) 010: Ramp pattern: need to set proper increment using CUSTOM PAT register 011: Constant Pattern using CUSTOM PAT [17:0] in register 0x14/15/16. others: not used
4-2	TEST PAT A	R/W	000	Enables test pattern output mode for channel A (NOTE: The test pattern is set prior to the bit mapper and is based on native resolution of the ADC starting from the MSB). These work in either output format. 000: Normal output mode (test pattern output disabled) 010: Ramp pattern: need to set proper increment using CUSTOM PAT register 011: Constant Pattern using CUSTOM PAT [17:0] in register 0x14/15/16. others: not used

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图 8-63. Register 0x19

7	6	5	4	3	2	1	0
FCLK SRC	0	0	FCLK DIV	0	0	0	TOG FCLK
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-23. Register 0x19 Field Descriptions

Bit	Field	Type	Reset	Description
7	FCLK SRC	R/W	0	User has to select if FCLK signal comes from ADC or from DDC block. Here real decimation is treated same as bypass mode 0: FCLK generated from ADC. FCLK SRC set to 0 for DDC bypass, real decimation mode and 1/2-w complex decimation mode. 1: FCLK generated from DDC block. In complex decimation mode only this bit needs to be set for 2-w and 1-w output interface mode but NOT for 1/2-w mode.
6-5	0	R/W	0	Must write 0
4	FCLK DIV	R/W	0	This bit needs to be set to 1 for 2-w output mode in bypass mode only (non decimation). 0: All output interface modes except 2-w bypass mode. 1: 2-w output interface mode.
3-1	0	R/W	0	Must write 0
0	TOG FCLK	R/W	0	This bit adjusts the FCLK signal appropriately for 1/2-wire mode where FCLK is stretched to cover channel A and channel B. This bit ONLY needs to be set in 1/2-wire mode with complex decimation mode. 0: all other modes. 1: FCLK for 1/2-wire complex decimation mode.

表 8-24. Configuration of FCLK SRC and FCLK DIV Register Bits vs Serial Interface

BYPASS/DECIMATION	SERIAL INTERFACE	FCLK SRC	FCLK DIV	TOG FCLK
Decimation Bypass/ Real Decimation	2-wire	0	1	0
	1-wire	0	0	0
	1/2-wire	0	0	0
Complex Decimation	2-wire	1	0	0
	1-wire	1	0	0
	1/2-wire	0	0	1

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图 8-64. Register 0x1A

7	6	5	4	3	2	1	0
0	LVDS ½ SWING	0	0	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-25. Register 0x1A Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0
6	LVDS ½ SWING	R/W	0	This bit reduces the LVDS output current from 3.5 mA to 1.75 mA which reduces power consumption. 0: Normal output current 3.5 mA 1: Reduced LVDS output current 1.75 mA
5-0	0	R/W	0	Must write 0

图 8-65. Register 0x1B

7	6	5	4	3	2	1	0
MAPPER EN	20B EN	BIT MAPPER RES			0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-26. Register 0x1B Field Descriptions

Bit	Field	Type	Reset	Description
7	MAPPER EN	R/W	0	This bit enables changing the resolution of the output (including output serialization factor) in bypass mode only. This bit doesn't need to be set for 20-bit resolution output. 0: Output bit mapper disabled. 1: Output bit mapper enabled.
6	20B EN	R/W	0	This bit enables 20-bit output resolution which can be useful for very high decimation settings so that quantization noise doesn't impact the ADC performance. 0: 20-bit output resolution disabled. 1: 20-bit output resolution enabled.
5-3	BIT MAPPER RES	R/W	001	Sets the output resolution using the bit mapper. MAPPER EN bit (D6) needs to be enabled when operating in bypass mode.. 000: 18 bit 001: 16 bit 010: 14 bit all others, n/a
2-0	0	R/W	0	Must write 0

表 8-27. Register Settings for Output Bit Mapper vs Operating Mode

BYPASS/DECIMATION	OUTPUT RESOLUTION	MAPPER EN (D7)	BIT MAPPER RES (D5-D3)
Decimation Bypass	Resolution Change	1	000: 18-bit 001: 16-bit 010: 14-bit
Real Decimation	Resolution Change (default 18-bit)	0	
Complex Decimation		0	

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图 8-66. Register 0x1E

7	6	5	4	3	2	1	0
0	0	0	0	LVDS DATA DEL		LVDS DCLK DEL	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-28. Register 0x1E Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0	Must write 0
3-2	LVDS DATA DEL	R/W	00	These bits adjust the output timing of the SLVDS output data. 00: no delay 01: Data advanced by 50 ps 10: Data delayed by 50 ps 11: Data delayed by 100 ps
1-0	LVDS DCLK DEL	R/W	00	These bits adjust the output timing of the SLVDS DCLK output. 00: no delay 01: DCLK advanced by 50 ps 10: DCLK delayed by 50 ps 11: DCLK delayed by 100 ps

图 8-67. Register 0x20/21/22

7	6	5	4	3	2	1	0
FCLK PAT [7:0]							
FCLK PAT [15:8]							
0	SCR EN	0	0	FCLK PAT [19:16]			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-29. Register 0x20/21/22 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FCLK PAT [19:0]	R/W	0xFFC00	These bits can adjust the duty cycle of the FCLK. In decimation bypass mode the FCLK pattern gets adjusted automatically for the different output resolutions. 表 8-30 shows the proper FCLK pattern values for 1-wire and 1/2-wire in real/complex decimation.
6	SCR EN	R/W	0	This bit enables the output data scrambler. Digital bypass (0x24, D2) needs to be set as well. 0: Output scrambling disabled 1: Output scrambling enabled

表 8-30. FCLK Pattern for different resolution based on interface

DECIMATION	OUTPUT RESOLUTION	2-WIRE	1-WIRE	1/2-WIRE
REAL DECIMATION	14-bit	Use Default	0xFE000	Use Default
	16-bit		0xFF000	
	18-bit		0xFF800	
	20-bit		0xFFC00	
COMPLEX DECIMATION	14-bit		0xFFFFF	0xFFFFF
	16-bit			
	18-bit			
	20-bit			

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图 8-68. Register 0x24

7	6	5	4	3	2	1	0
0	0	0	DDC MUX		DIG BYP	DDC EN	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-31. Register 0x24 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0	Must write 0
4-3	DDC MUX	R/W	0	Configures DDC MUX in front of the decimation filter. 00: ADC channel A connected to DDC A 01: ADC channel A connected to DDC A and DDC B. others: not used
2	DIG BYP	R/W	0	This bit needs to be set to enable digital features block which includes decimation and scrambling. 0: Digital feature block bypassed - lowest latency 1: Data path includes digital features
1	DDC EN	R/W	0	Enables internal decimation filter for both channels 0: DDC disabled. 1: DDC enabled.
0	0	R/W	0	Must write 0

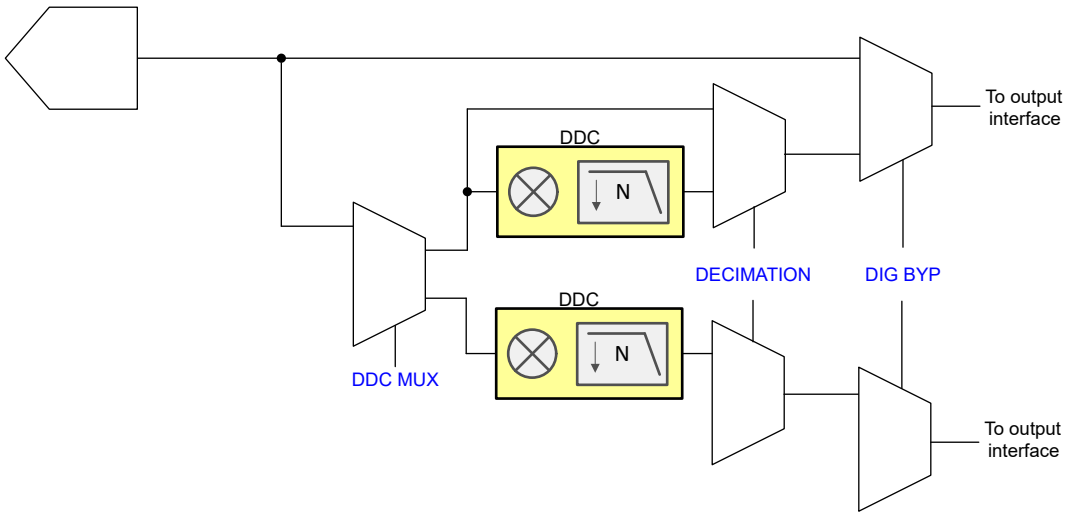

图 8-69. Register control for digital features

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图 8-70. Register 0x25

7	6	5	4	3	2	1	0
DDC MUX EN	DECIMATION			REAL OUT	0	0	MIX PHASE
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-32. Register 0x25 Field Descriptions

Bit	Field	Type	Reset	Description
7	DDC MUX EN	R/W	0	Enables the digital mux between ADCs and decimation filters. This bit is required for DDC mux settings in register 0x24 (D4, D3) to go into effect. 0: DDC mux disabled 1: DDC mux enabled
6-4	DECIMATION	R/W	000	Complex decimation setting. This applies to both channels. 000: Bypass mode (no decimation) 001: Decimation by 2 010: Decimation by 4 011: Decimation by 8 100: Decimation by 16 101: Decimation by 32 others: not used
3	REAL OUT	R/W	0	This bit selects real output decimation. This mode applies to both channels. In this mode, the decimation filter is a low pass filter and no complex mixing is performed to reduce power consumption. For maximum power savings the NCO in this case should be set to 0. 0: Complex decimation 1: Real decimation
2-1	0	R/W	0	Must write 0
0	MIX PHASE	R/W	0	This bit used to invert the NCO phase 0: NCO phase as is. 1: NCO phase inverted.

图 8-71. Register 0x26

7	6	5	4	3	2	1	0
MIX GAIN A		MIX RES A	FS/4 MIX A	MIX GAIN B		MIX RES B	FS/4 MIX B
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-33. Register 0x26 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	MIX GAIN A	R/W	00	This bit applies a 0, 3 or 6-dB digital gain to the output of digital mixer to compensate for the mixing loss for channel A. 00: no digital gain added 01: 3-dB digital gain added 10: 6-dB digital gain added 11: not used
5	MIX RES A	R/W	0	Toggling this bit resets the NCO phase of channel A and loads the new NCO frequency. This bit does not self reset.
4	FS/4 MIX A	R/W	0	Enables FS/4 mixing for DDC A (complex decimation only). 0: FS/4 mixing disabled. 1: FS/4 mixing enabled.
3-2	MIX GAIN B	R/W	00	This bit applies a 0, 3 or 6-dB digital gain to the output of digital mixer to compensate for the mixing loss for channel B. 00: no digital gain added 01: 3-dB digital gain added 10: 6-dB digital gain added 11: not used
1	MIX RES B	R/W	0	Toggling this bit resets the NCO phase of channel B and loads the new NCO frequency. This bit does not self reset.

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表 8-33. Register 0x26 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FS/4 MIX B	R/W	0	Enables FS/4 mixing for DDC B (complex decimation only). 0: FS/4 mixing disabled. 1: FS/4 mixing enabled.

图 8-72. Register 0x27

7	6	5	4	3	2	1	0
0	0	0	OP ORDER A	Q-DEL A	FS/4 MIX PH A	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-34. Register 0x27 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0	Must write 0
4	OP ORDER A	R/W	0	Swaps the I and Q output order for channel A 0: Output order is I[n], Q[n] 1: Output order is swapped: Q[n], I[n]
3	Q-DEL A	R/W	0	This delays the Q-sample output of channel A by one. 0: Output order is I[n], Q[n] 1: Q-sample is delayed by 1 sample: I[n], Q[n+1], I[n+1], Q[n+2]
2	FS/4 MIX PH A	R/W	0	Inverts the mixer phase for channel A when using FS/4 mixer 0: Mixer phase is non-inverted 1: Mixer phase is inverted
1-0	0	R/W	0	Must write 0

图 8-73. Register 0x2A/B/C/D

7	6	5	4	3	2	1	0
NCO A [7:0]							
NCO A [15:8]							
NCO A [23:16]							
NCO A [31:24]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-35. Register 0x2A/2B/2C/2D Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NCO A [31:0]	R/W	0	Sets the 32 bit NCO value for decimation filter channel A. The NCO value is $f_{NCO} \times 2^{32}/F_S$ In real decimation mode these registers are automatically set to 0.

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图 8-74. Register 0x2E

7	6	5	4	3	2	1	0
0	0	0	OP ORDER B	Q-DEL B	FS/4 MIX PH B	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-36. Register 0x2E Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0	Must write 0
4	OP ORDER B	R/W	0	Swaps the I and Q output order for channel B 0: Output order is I[n], Q[n] 1: Output order is swapped: Q[n], I[n]
3	Q-DEL B	R/W	0	This delays the Q-sample output of channel B by one. 0: Output order is I[n], Q[n] 1: Q-sample is delayed by 1 sample: I[n], Q[n+1], I[n+1], Q[n+2]
2	FS/4 MIX PH B	R/W	0	Inverts the mixer phase for channel B when using FS/4 mixer 0: Mixer phase is non-inverted 1: Mixer phase is inverted
1-0	0	R/W	0	Must write 0

图 8-75. Register 0x31/32/33/34

7	6	5	4	3	2	1	0
NCO B [7:0]							
NCO B [15:8]							
NCO B [23:16]							
NCO B [31:24]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-37. Register 0x31/32/33/34 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NCO B [31:0]	R/W	0	Sets the 32 bit NCO value for decimation filter channel B. The NCO value is $f_{NCO} \times 2^{32}/F_S$ In real decimation mode these registers are automatically set to 0.

图 8-76. Register 0x39..0x60

7	6	5	4	3	2	1	0
OUTPUT BIT MAPPER CHA							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-38. Register 0x39..0x60 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUTPUT BIT MAPPER CHA	R/W	0	These registers are used to reorder the output data bus. See the 节 8.3.5.2 on how to program it.

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图 8-77. Register 0x61..0x88

7	6	5	4	3	2	1	0
OUTPUT BIT MAPPER CHB							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-39. Register 0x61..0x88 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUTPUT BIT MAPPER CHB	R/W	0	These registers are used to reorder the output data bus. See the 节 8.3.5.2 on how to program it.

图 8-78. Register 0x8F

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FORMAT A	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-40. Register 0x8F Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0	Must write 0
1	FORMAT A	R/W	0	This bit sets the output data format for channel A. Digital bypass register bit (0x24, D2) needs to be enabled as well. 0: 2s complement 1: Offset binary
0	0	R/W	0	Must write 0

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图 8-79. Register 0x92

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FORMAT B	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 8-41. Register 0x92 Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0	Must write 0
1	FORMAT B	R/W	0	This bit sets the output data format for channel B. Digital bypass register bit (0x24, D2) needs to be enabled as well. 0: 2s complement 1: Offset binary
0	0	R/W	0	Must write 0

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9 Application Information Disclaimer

备注

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9.1 Typical Application

A spectrum analyzer is a typical frequency domain application for the ADC356x and its front end circuitry is very similar to several other systems such as software defined radio (SDR), sonar, radar or communications. Some applications require frequency coverage including DC or near DC (such as. sonar), so it is included in this example.

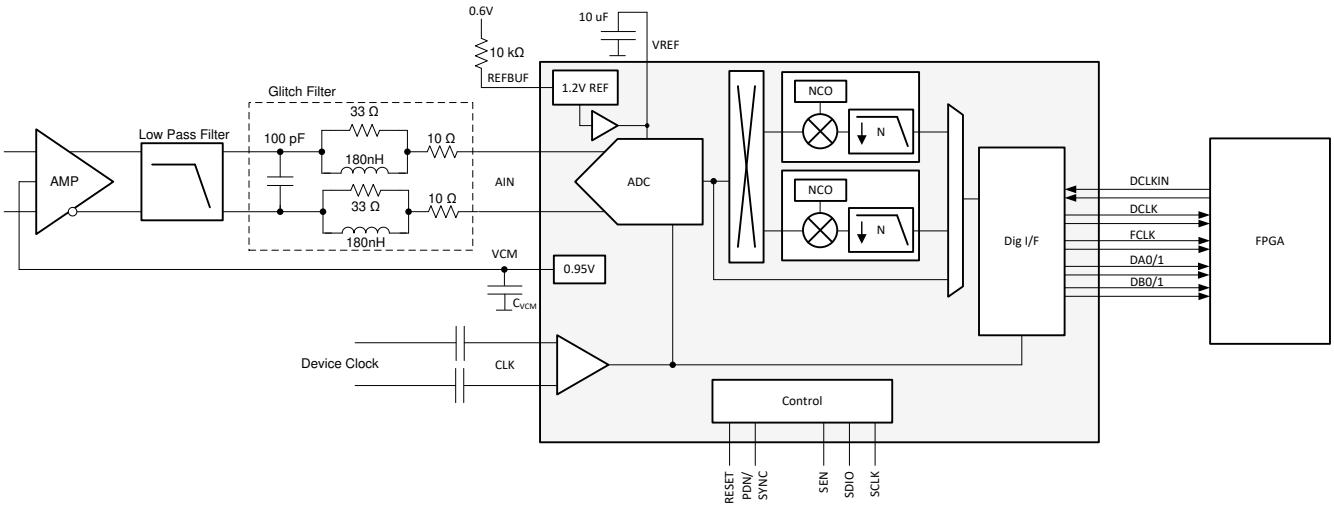

图 9-1. Typical configuration for a spectrum analyzer with DC support

9.1.1 Design Requirements

Frequency domain applications cover a wide range of frequencies from low input frequencies at or near DC in the 1st Nyquist zone to under sampling in higher Nyquist zones. If very low input frequency is supported then the input has to be DC coupled and the ADC driven by a fully differential amplifier (FDA). If low frequency support is not needed, then AC coupling and use of a balun may be more suitable.

The internal reference is used since DC precision is not needed. However the ADC AC performance is highly dependent on the quality of the external clock source. If in-band interferes can be present, then the ADC SFDR performance will be a key care about as well. A higher ADC sampling rate is desirable in order to relax the external anti-aliasing filter – an internal decimation filter can be used to reduce the digital output rate afterwards.

表 9-1. Design key care-abouts

FEATURE	DESCRIPTION
Signal Bandwidth	DC to 20 MHz
Input Driver	Single ended to differential signal conversion and DC coupling
Clock Source	External clock with low jitter

When designing the amplifier/filter driving circuit, the ADC input full-scale voltage needs to be taken into consideration. For example, the ADC356x input full-scale is 3.2 Vpp. When factoring in ~ 1 dB for insertion loss of the filter, then the amplifier needs to deliver close to 3.6 Vpp. The amplifier distortion performance will degrade with a larger output swing and considering the ADC common mode input voltage the amplifier may not be able to deliver the full swing. The ADC356x provides an output common mode voltage of 0.95 V and the THS4541 for

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example can only swing within 250 mV of its negative supply. A unipolar 3.3 V amplifier power supply will thus limit the maximum voltage swing to ~ 2.8 Vpp. Hence if a larger output swing is required (factoring in filter insertion loss) then a negative supply for the amplifier is needed in order to eliminate that limitation. Additionally input voltage protection diodes may be needed to protect the ADC from over-voltage events.

表 9-2. Output voltage swing of THS4541 vs power supply

DEVICE	MIN OUTPUT VOLTAGE	MAX SWING WITH 3.3 V/ 0 V SUPPLY	MAX SWING WITH 3.3 V/ -1 V SUPPLY
THS4541	VS- + 250 mV	2.8 Vpp	6.8 Vpp

9.1.2 Detailed Design Procedure

9.1.2.1 Input Signal Path

Depending on desired input signal frequency range the THS4551 and THS4541 provide very good low power options to drive the ADC inputs. 表 9-3 provides a comparison between the THS4551 and THS4541 and the power consumption vs usable frequency trade off.

表 9-3. Fully Differential Amplifier Options

DEVICE	CURRENT (IQ) PER CHANNEL	USABLE FREQUENCY RANGE
THS4561	0.8 mA	< 3 MHz
THS4551	1.4 mA	< 10 MHz
THS4541	10 mA	< 70 MHz

The low pass filter design (topology, filter order) is driven by the application itself. However, when designing the low pass filter, the optimum load impedance for the amplifier should be taken into consideration as well. Between the low pass filter and the ADC input the sampling glitch filter needs to added as well as shown in Sampling Glitch Filter Design. In this example, the DC - 30 MHz glitch filter is selected.

9.1.2.2 Sampling Clock

Applications operating with low input frequencies (such as DC to 20 MHz) typically are less sensitive to performance degradation due to clock jitter. The internal ADC aperture jitter improves with faster rise and fall times (i.e. square wave vs sine wave). 表 9-4 provides an overview of the estimated SNR performance of the ADC356x based on different amounts of jitter of the external clock source. The SNR is estimated based on ADC356x thermal noise of 84.5dBFS and input signal at -1dBFS.

表 9-4. ADC SNR performance across vs input frequency for different amounts of external clock jitter

INPUT FREQUENCY	$T_{J,EXT}$ = 100 fs	$T_{J,EXT}$ = 250 fs	$T_{J,EXT}$ = 500 fs	$T_{J,EXT}$ = 1 ps
5 MHz	82.0	81.9	81.8	81.5
10 MHz	81.9	81.8	81.4	80.2
20 MHz	81.6	81.2	80.1	77.2

Termination of the clock input should be considered for long clock traces.

9.1.2.3 Voltage Reference

The ADC356x is configured to internal reference operation by applying 0.6 V to the REFBUF pin.

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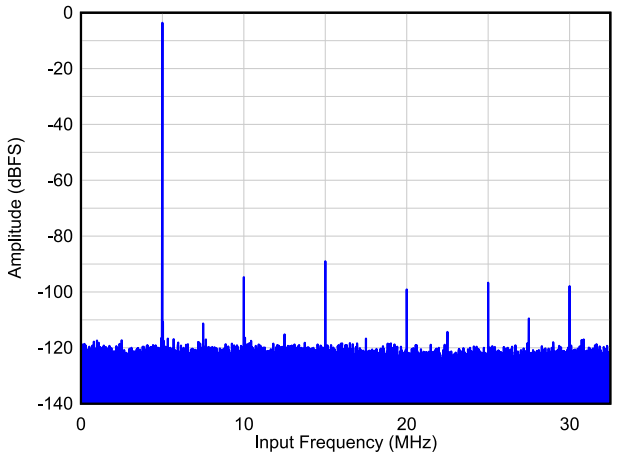
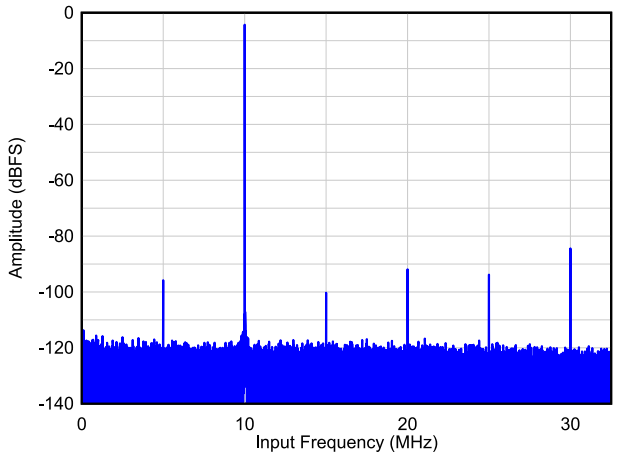
9.1.3 Application Curves

The following FFT plots show the performance of THS4541 driving the ADC3563 operated at 65 MSPS with a full-scale input at -1 dBFS and input frequencies of 5, 10 and 20 MHz.



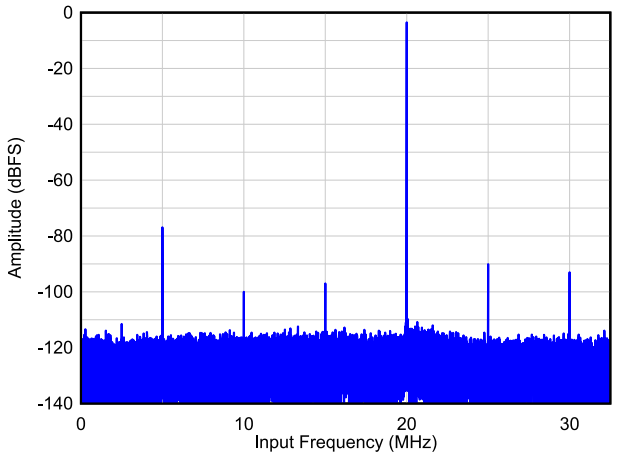
SNR = 81.0 dBFS, SFDR = 88 dBc, Non HD23 = 95 dBFS

图 9-2. Single Tone FFT at F_{IN} = 5 MHz



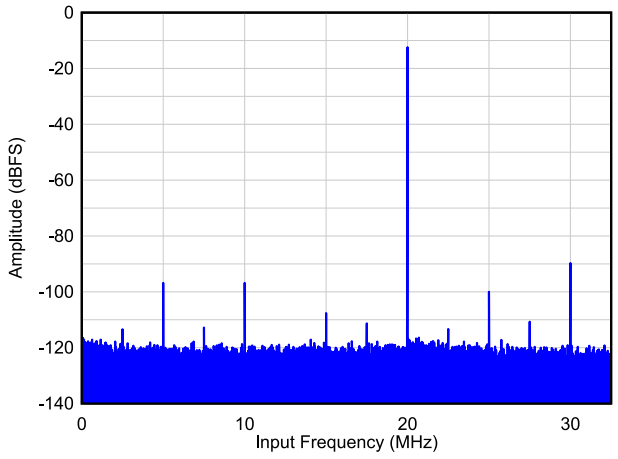
SNR = 80.4 dBFS, SFDR = 91 dBc, Non HD23 = 83 dBFS

图 9-3. Single Tone FFT at F_{IN} = 10 MHz



SNR = 77.2 dBFS, SFDR = 76 dBc, Non HD23 = 93 dBFS

图 9-4. Single Tone FFT at F_{IN} = 20 MHz



A_{IN} = -10 dBFS, SNR = 81.0 dBFS, SFDR = 87 dBc, Non HD23 = 90 dBFS

图 9-5. Single Tone FFT at F_{IN} = 20 MHz

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9.2 Initialization Set Up

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin, as shown in 图 9-6.

1. Apply AVDD and IOVDD (no specific sequence required). After AVDD is applied the internal bandgap reference will power up and settle out in ~ 2ms.
2. Configure REFBUF pin (pull high or low even if configured via SPI later on) and apply the sampling clock.
3. Apply hardware reset. After hardware reset is released, the default registers are loaded from internal fuses and the internal power up capacitor calibration is initiated. The calibration takes approximately 200000 clock cycles.
4. Begin programming using SPI interface.

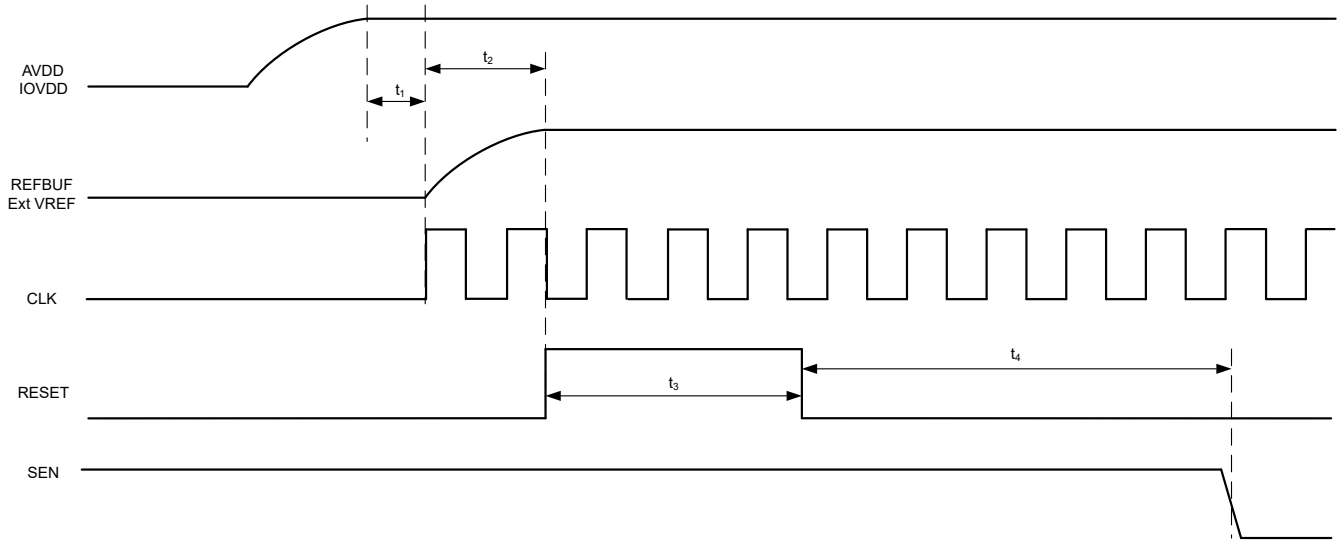

图 9-6. Initialization of serial registers after power up

表 9-5. Power-up timing

		MIN	TYP	MAX	UNIT
t_1	Power-on delay: delay from power up to logic level of REFBUF pin	2			ms
t_2	Delay from REFBUF pin logic level to RESET rising edge	100			ns
t_3	RESET pulse width	1			us
t_4	Delay from RESET disable to SEN active	~ 200000			clock cycles

9.2.1 Register Initialization During Operation

If required, the serial interface registers can be cleared and reset to default settings during operation either:

- through a hardware reset or
- by applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 0x00) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

After hardware or software reset the wait time is also ~ 200000 clock cycles before the SPI registers can be programmed.

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9.3 Power Supply Recommendations

The ADC356x requires two different power-supplies. The AVDD rail provides power for the internal analog circuits and the ADC itself while the IOVDD rail powers the digital interface and the internal digital circuits like decimation filter or output interface mapper. Power sequencing is not required.

The AVDD power supply must be low noise in order to achieve data sheet performance. In applications operating near DC, the 1/f noise contribution of the power supply needs to be considered as well. The ADC is designed for very good PSRR which aides with the power supply filter design.

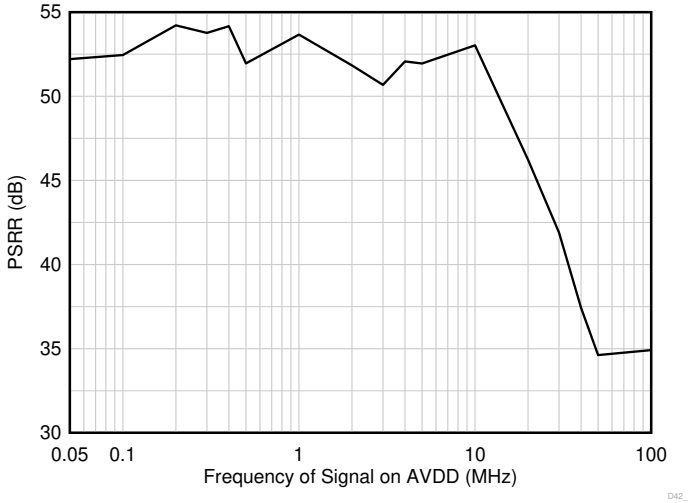

图 9-7. Power supply rejection ratio (PSRR) vs frequency

There are two recommended power-supply architectures:

1. 1. Step down using high-efficiency switching converters, followed by a second stage of regulation using a low noise LDO to provide switching noise reduction and improved voltage accuracy.
2. 2. Directly step down the final ADC supply voltage using high-efficiency switching converters. This approach provides the best efficiency, but care must be taken to ensure switching noise is minimized to prevent degraded ADC performance.

TI WEBENCH® Power Designer can be used to select and design the individual power-supply elements needed: see the WEBENCH® Power Designer

Recommended switching regulators for the first stage include the TPS62821, and similar devices.

Recommended low dropout (LDO) linear regulators include the TPS7A4701, TPS7A90, LP5901, and similar devices.

For the switch regulator only approach, the ripple filter must be designed with a notch frequency that aligns with the switching ripple frequency of the DC/DC converter. Note the switching frequency reported from WEBENCH® and design the EMI filter and capacitor combination to have the notch frequency centered as needed. 图 9-8 and 图 9-9 illustrate the two approaches.

AVDD and IOVDD supply voltages should not be shared in order to prevent digital switching noise from coupling into the analog signal chain.

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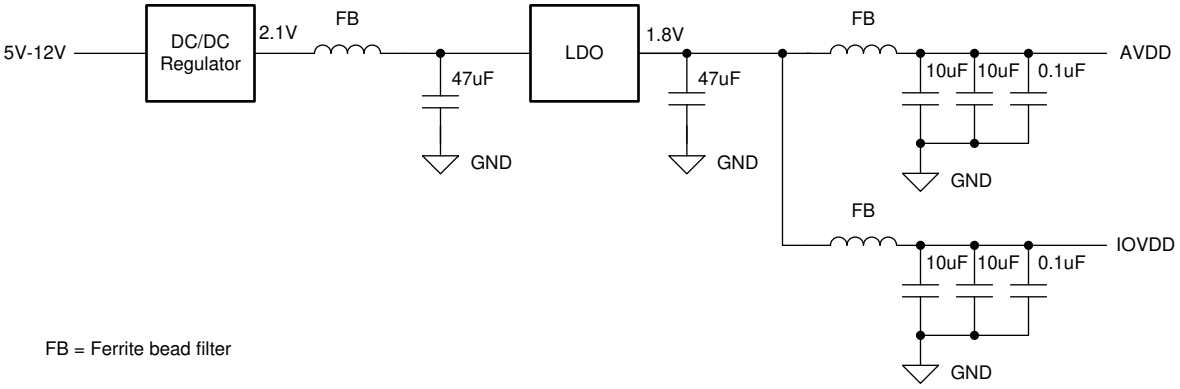

图 9-8. Example: LDO Linear Regulator Approach

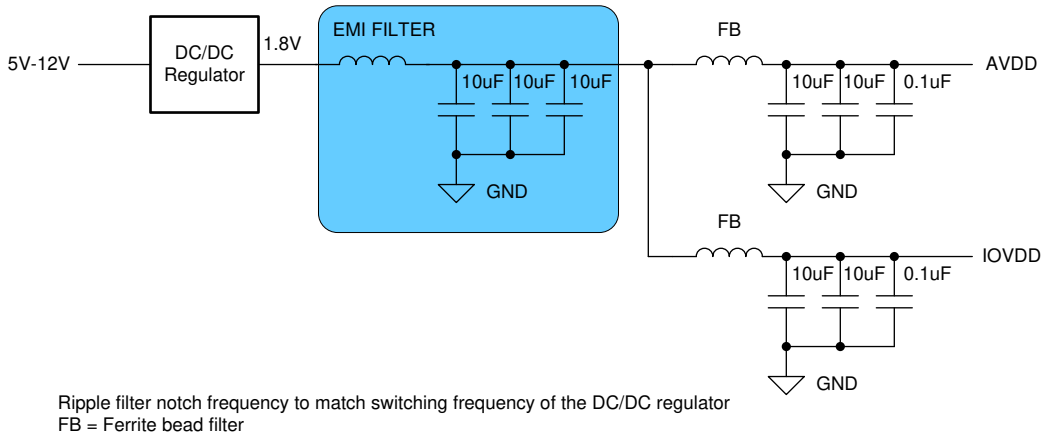

图 9-9. Example Switcher-Only Approach

9.4 Layout

9.4.1 Layout Guidelines

There are several critical signals which require specific care during board design:

1. Analog input and clock signals
   - Traces should be as short as possible and vias should be avoided where possible to minimize impedance discontinuities.
   - Traces should be routed using loosely coupled 100-Ω differential traces.
   - Differential trace lengths should be matched as close as possible to minimize phase imbalance and HD2 degradation.
2. Digital output interface
   - Traces should be routed using tightly coupled 100-Ω differential traces.
3. Voltage reference
   - The bypass capacitor should be placed as close to the device pins as possible and connected between VREF and REFGND – on top layer avoiding vias.
   - Depending on configuration an additional bypass capacitor between REFBUF and REFGND may be recommended and should also be placed as close to pins as possible on top layer.
4. Power and ground connections
   - Provide low resistance connection paths to all power and ground pins.
   - Use power and ground planes instead of traces.
   - Avoid narrow, isolated paths which increase the connection resistance.

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- Use a signal/ground/power circuit board stackup to maximize coupling between the ground and power plane.

9.4.2 Layout Example

The following screen shot shows the top layer of the ADC356x/368x EVM.

- Signal and clock inputs are routed as differential signals on the top layer avoiding vias.
- SLVDS output interface lanes are routed differential and length matched
- Bypass caps are close to the VREF pin on the top layer avoiding vias.

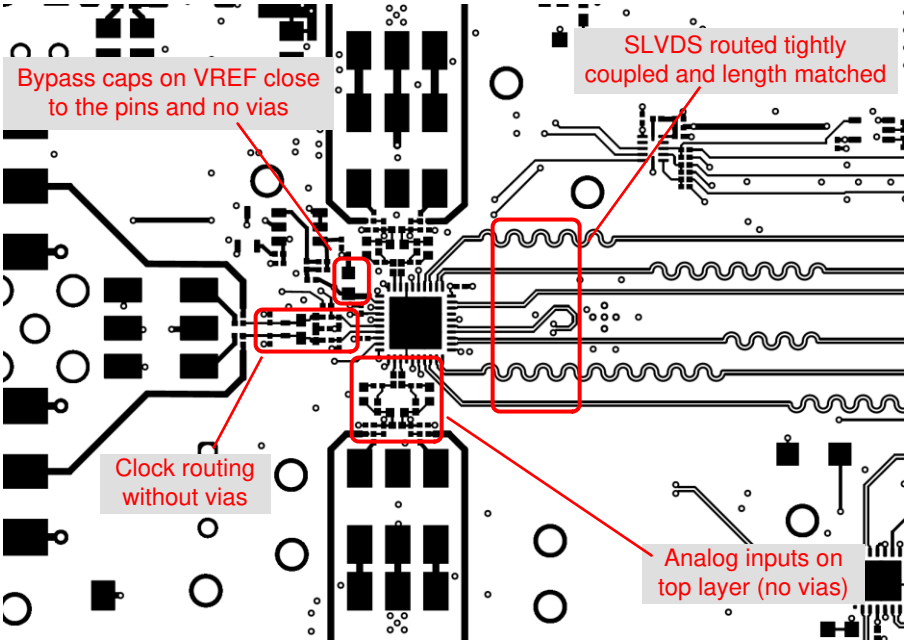

图 9-10. Layout example: top layer of ADC356x/368x EVM

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10 Device and Documentation Support

10.1 Device Support

10.2 Documentation Support

10.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC3561IRSBR	ACTIVE	WQFN	RSB	40	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	AZ3561	Samples
ADC3561IRSBT	ACTIVE	WQFN	RSB	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	AZ3561	Samples
ADC3562IRSBR	ACTIVE	WQFN	RSB	40	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	AZ3562	Samples
ADC3562IRSBT	ACTIVE	WQFN	RSB	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	AZ3562	Samples
ADC3563IRSBR	ACTIVE	WQFN	RSB	40	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	AZ3563	Samples
ADC3563IRSBT	ACTIVE	WQFN	RSB	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	AZ3563	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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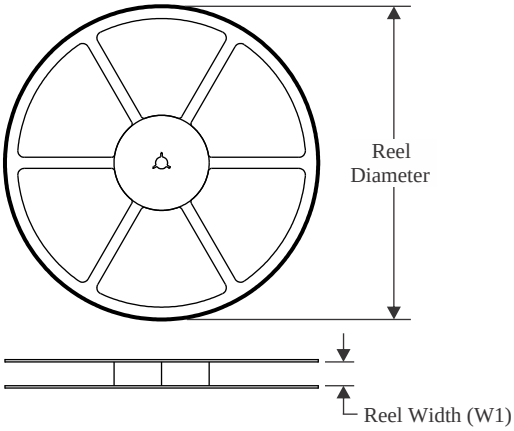
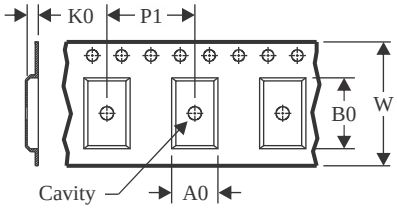
TAPE AND REEL INFORMATION

REEL DIMENSIONS

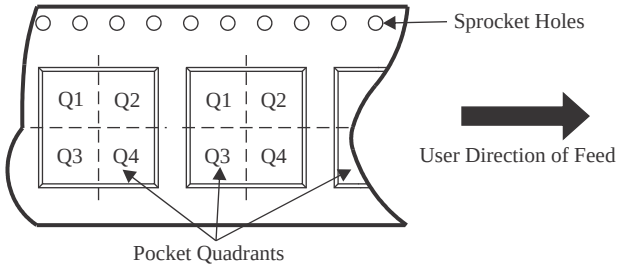


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

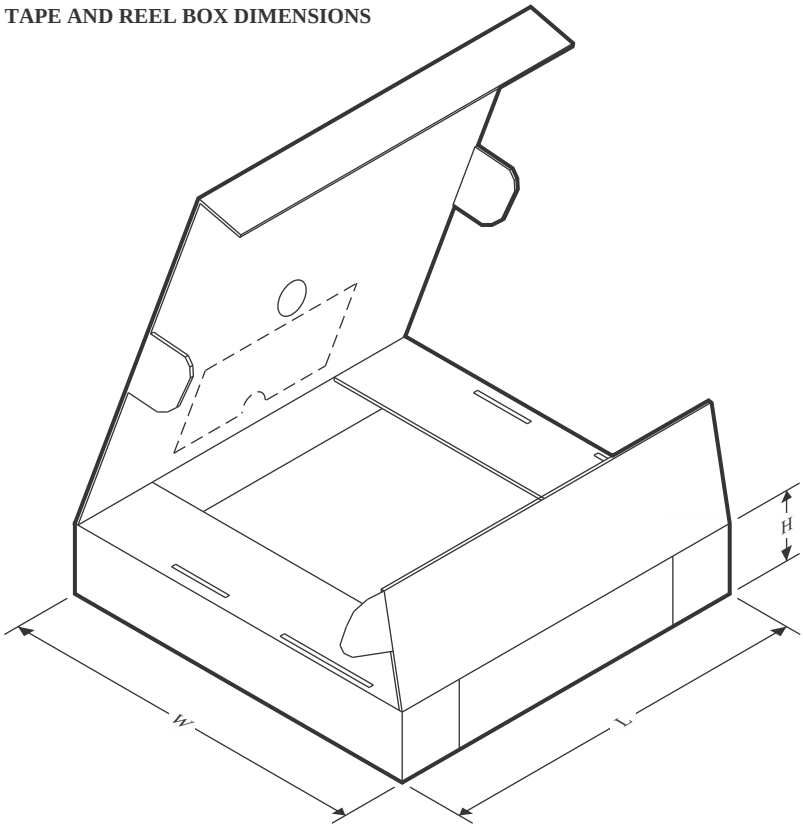
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC3561IRSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADC3562IRSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADC3563IRSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC3561IRSBR	WQFN	RSB	40	3000	350.0	350.0	43.0
ADC3562IRSBR	WQFN	RSB	40	3000	350.0	350.0	43.0
ADC3563IRSBR	WQFN	RSB	40	3000	350.0	350.0	43.0

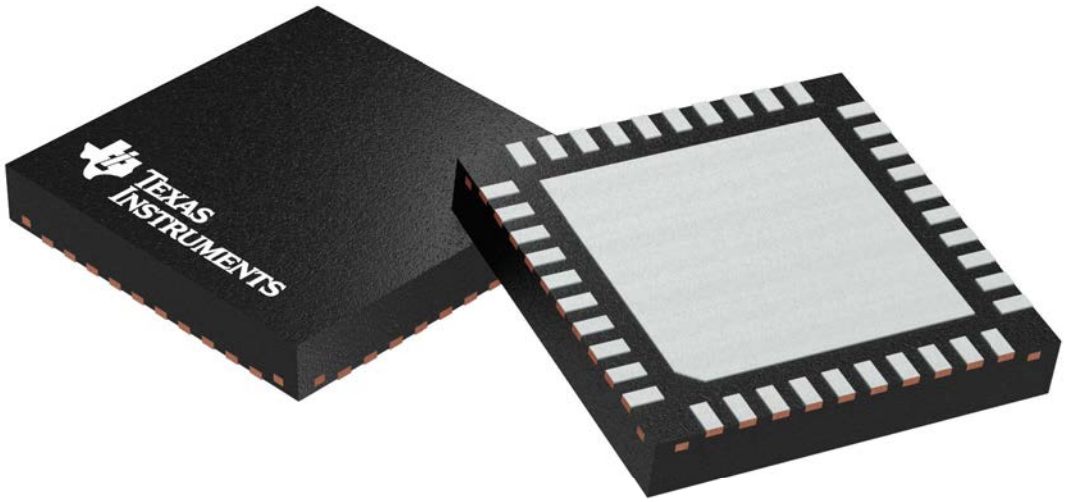
GENERIC PACKAGE VIEW

RSB 40

WQFN - 0.8 mm max height

5 x 5 mm, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



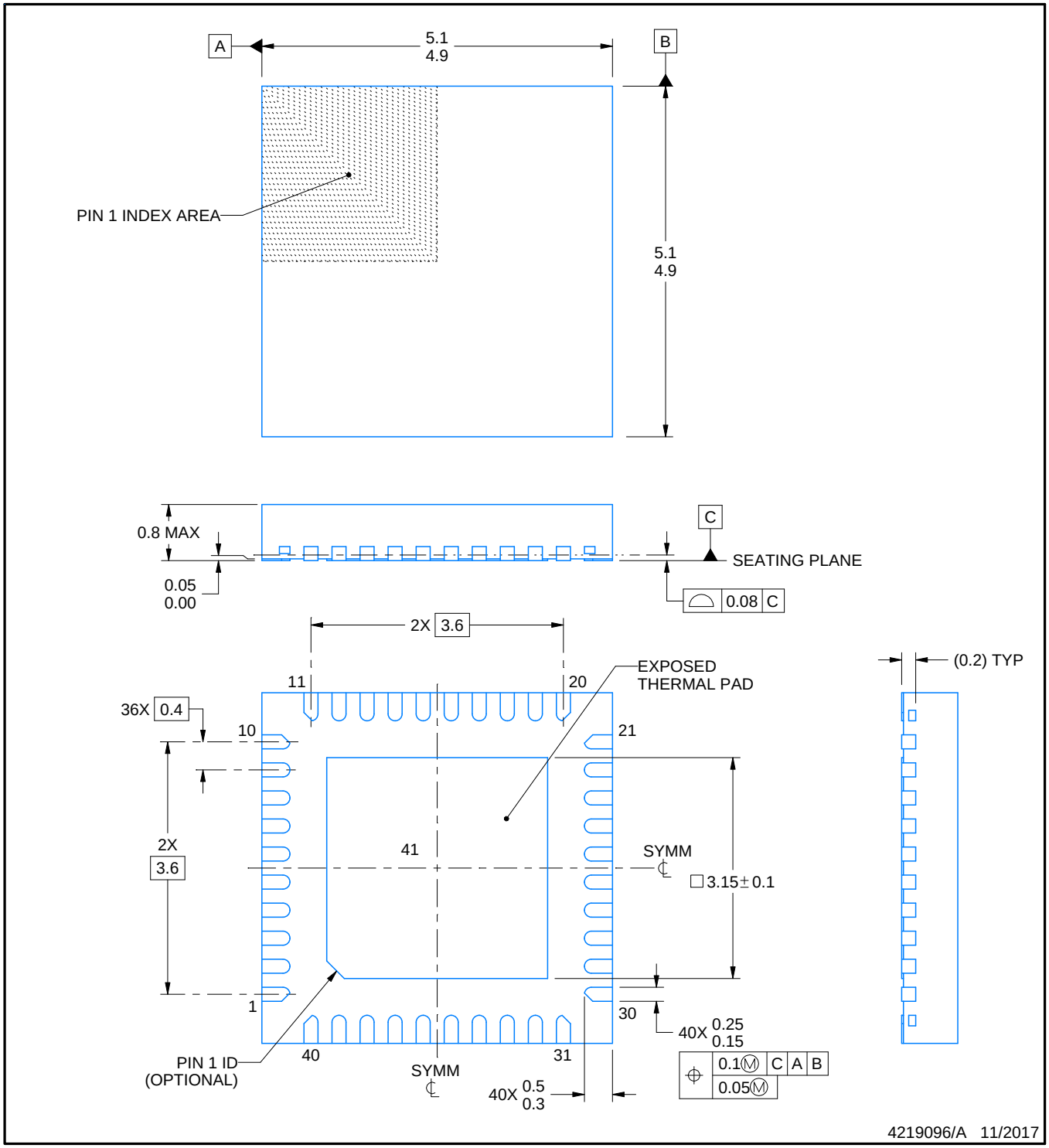
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RSB0040E

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

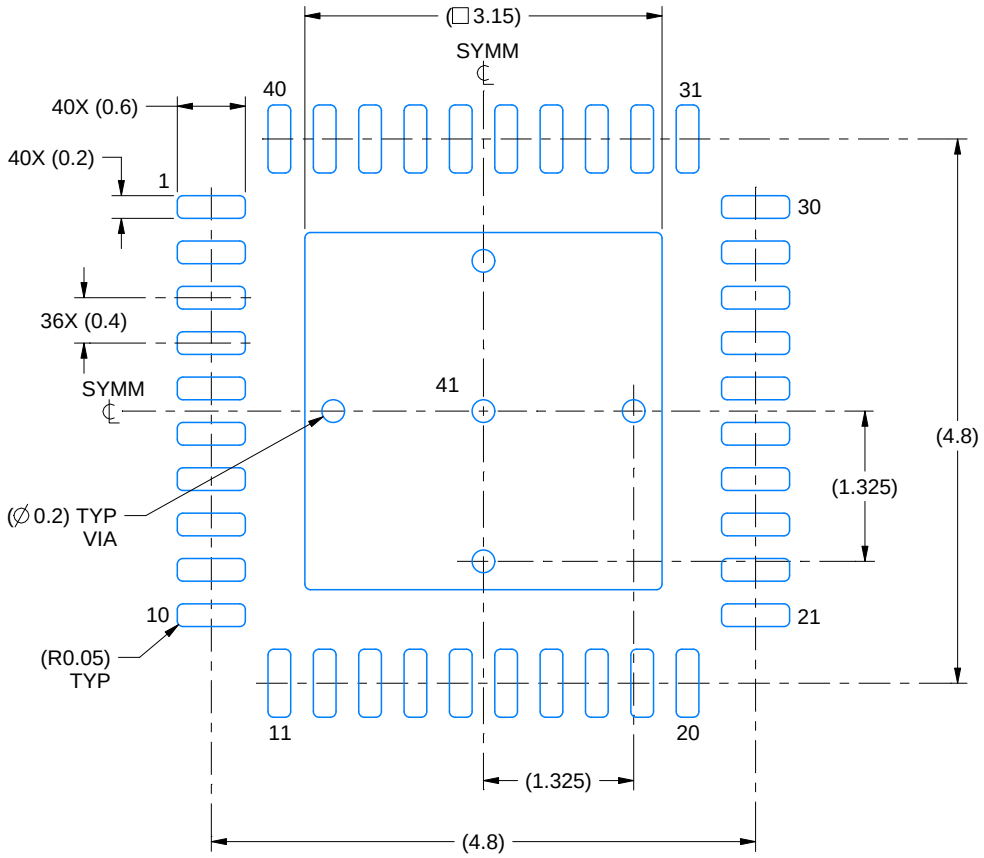
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

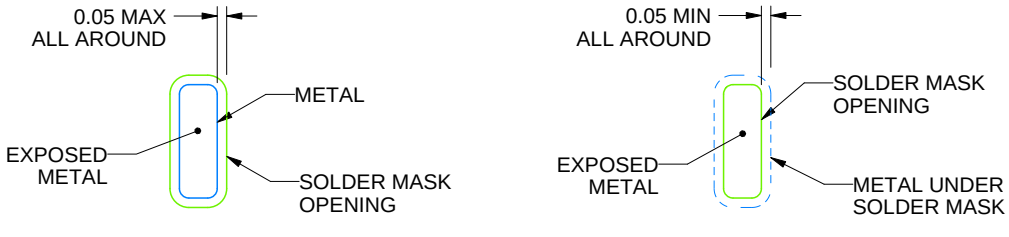
RSB0040E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

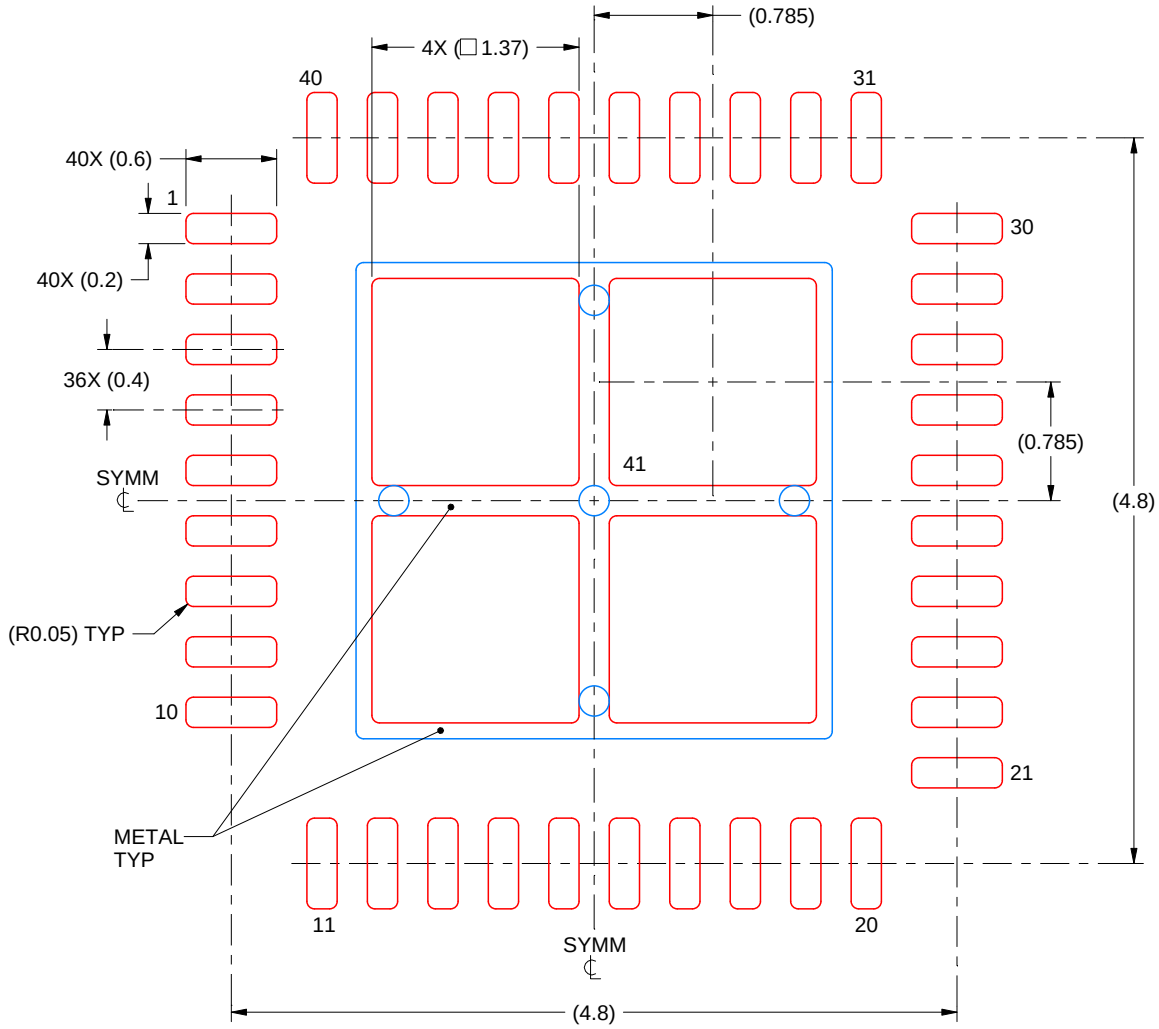
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219096/A 11/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219096/A 11/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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