ULN2803A

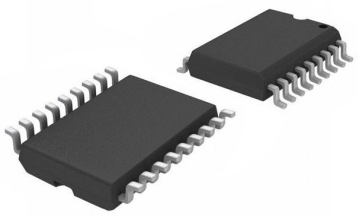
Darlington Transistor Arrays

Features

- 500-mA-Rated Collector Current(Single Output)
- High-Voltage Outputs: 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic

Package

SOP-18



Applications

- Relay Drivers
- Hammer Drivers
- Lamp Drivers
- Display Drivers (LED and Gas Discharge)
- Line Drivers

Applications

- Logic Buffers
- Stepper Motors
- IP Camera
- HVAC Valve and LED Dot Matrix

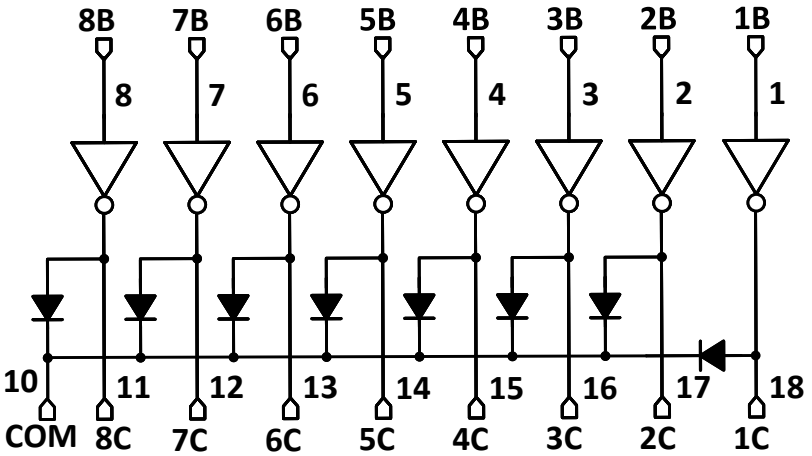
General Description

The ULN2803A device is a 50 V, 500 mA Darlington transistor array. The device consists of eight NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be connected in parallel for higher current capability.

Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULN2803A device has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

Connection Diagram

Logical Diagram



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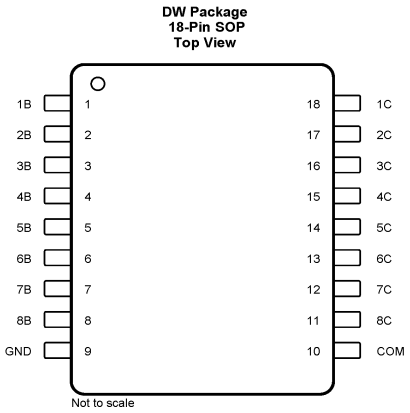
ULN2803A

Darlington Transistor Arrays

Marking



Pin Description



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 through 8 Darlington base input
2B	2		
3B	3		
4B	4		
5B	5		
6B	6		
7B	7		
8B	8		
1C	18	O	Channel 1 through 8 Darlington collector output
2C	17		
3C	16		
4C	15		
5C	14		
6C	13		
7C	12		
8C	11		
GND	9	–	Common emitter shared by all channels (typically tied to ground)
COM	10	I/O	Common cathode node for flyback diodes (required for inductive loads)

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ULN2803A

Darlington Transistor Arrays

Absolute Maximum Ratings (At 25°C free-air temperature unless otherwise noted)(1)

Symbol	Parameter	Min	Max	Units
V_{CE}	Collector to emitter voltage	–	50	V
V_{IN}	Input voltage(2)	-0.3	30	V
$V_{IN(on)}$	Input open voltage	2.4(3)	30	V
$V_{IN(off)}$	Input turn-off voltage(4)	-0.3	0.7	V
I_C	Peak collector current	–	500	mA
I_{CP}	Output clamp current	–	500	mA
I_E	Total substrate-terminal current	–	-2.5	A
T_J	Operating virtual junction temperature	-55	150	°C
T_{STG}	Storage temperature range	-55	150	°C

Notes:(1) Stresses beyond those listed under ”absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ”recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

(3) V_{CE}=2V,I_{out}=200mA.

(4) Input voltage below -0.3V is not recommended. If input overshoot occurs, ensure the overshoot voltage is greater than -0.7V and the pulse width is less than 10ms.

ESD Ratings

Symbol	Parameter	VALUE	UNIT
$V_{(ESD)}$	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	MIN.	MAX.	UNIT
V_{CE}	Collector-emitter voltage	0	50	V
T_A	Ambient temperature	-40	85	°C

Thermal Information

Symbol	Parameter	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

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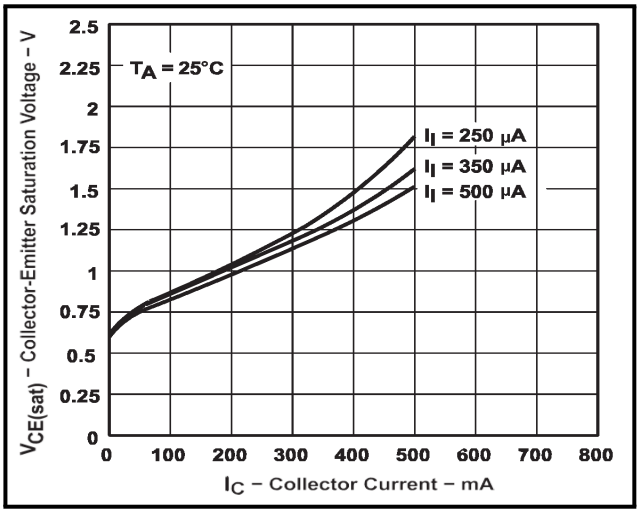
ULN2803A

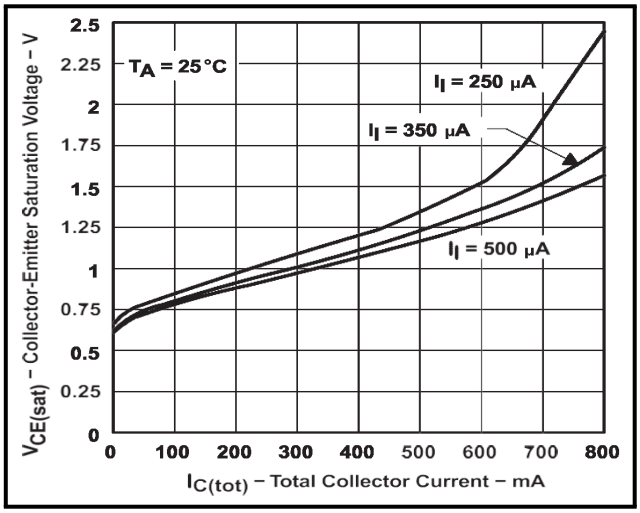
Darlington Transistor Arrays

Electrical Characteristics (T_A=+25°C, unless otherwise specified)

Parameter		Test Figure	Test Conditions		BE2803A			Unit
					MIN.	TYP.	MAX.	
$V_{I(on)}$	Input current- on condition	Figure 6	V_{CE} = 2V	I_C = 200 mA	–	–	2.4	V
				I_C = 250 mA	–	–	2.7	
				I_C = 300 mA	–	–	3.0	
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 7	I_I = 250μA	I_C = 100 mA	–	0.9	1.1	V
			I_I = 350μA	I_C = 200 mA	–	1.0	1.3	
			I_I = 500μA	I_C = 350 mA	–	1.3	1.6	
I_{CEX}	Collector cutoff current	Figure 3	V_{CE} = 50V	I_I = 0	–	–	50	μA
$I_{I(off)}$	Off-state input current	Figure 4	V_{CE} = 50V, T_A=70°C	I_C = 500μA	50	65	–	μA
$I_{I(on)}$	On-state input voltage	Figure 5	V_I = 3.85V	–	–	0.93	1.35	mA
I_R	Clamp diode reverse current	Figure 8	V_R = 50V	–	–	–	50	μA
V_F	Clamp diode forward Voltage	Figure 9	I_F = 350 mA	–	–	1.6	2.0	V
C_i	Input capacitance	–	V_I = 0	f = 1 MHz	–	15	25	pF
t_{PLH}	Propagation delay time, low - to high-level output	Figure 10	V_S = 50V,C_L = 15PF , R_L = 163Ω		–	130	–	ns
t_{PHL}	Propagation delay time, high- to low -level output				–	20	–	
V_{OH}	High-level output voltage after switching	Figure 11	V_S = 50V	I_O = 300mA	V_S-20	–	–	mV

Typical Characteristics





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Parameter Measurement Information

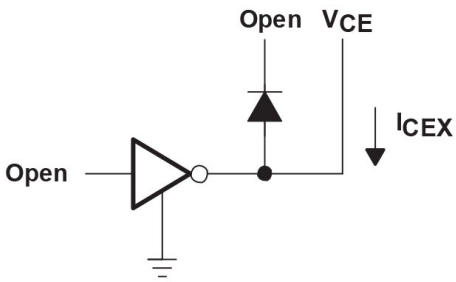


Figure 3. I_{CEX} Test Circuit

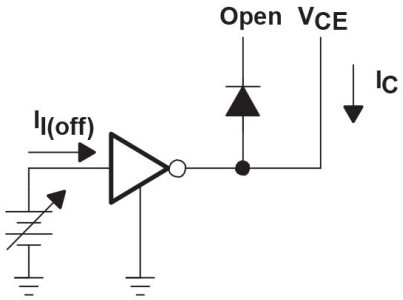


Figure 4. $I_{I(off)}$ Test Circuit

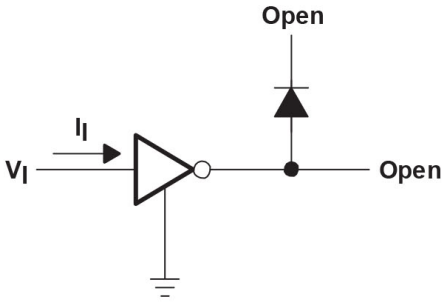


Figure 5. $I_{I(on)}$ Test Circuit

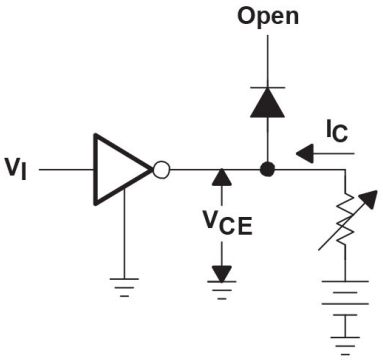


Figure 6. $V_{I(on)}$ Test Circuit

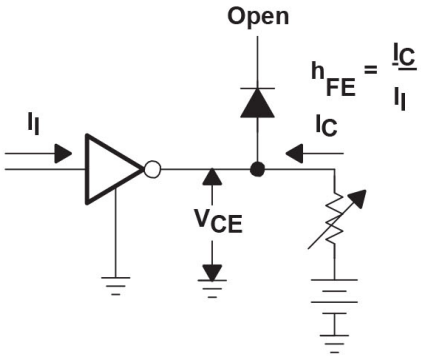


Figure 7. h_{FE}, $V_{CE(sat)}$ Test Circuit

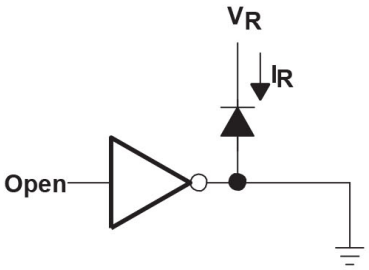


Figure 8. I_R Test Circuit

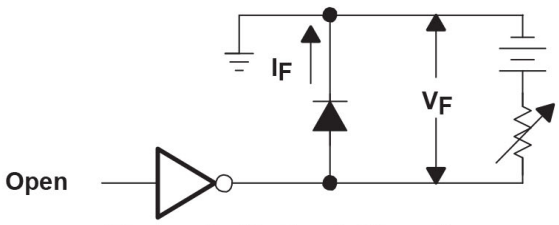


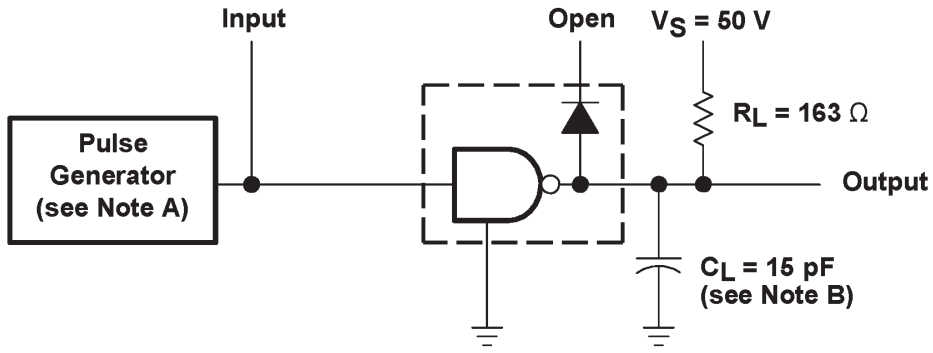
Figure 9. V_F Test Circuit

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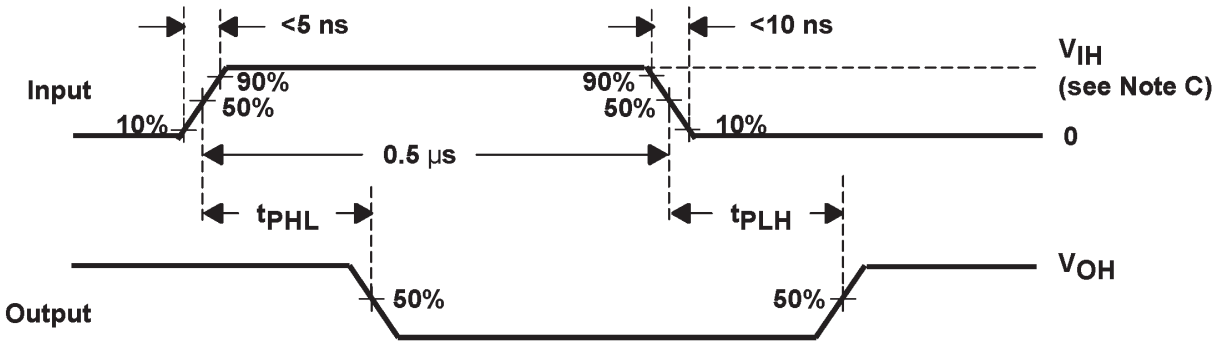
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Parameter Measurement Information

Parameter Measurement Information (continued)



Test Circuit



Voltage Waveforms

A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

C. V_{IH} = 3 V

Figure 10. Propagation Delay Times

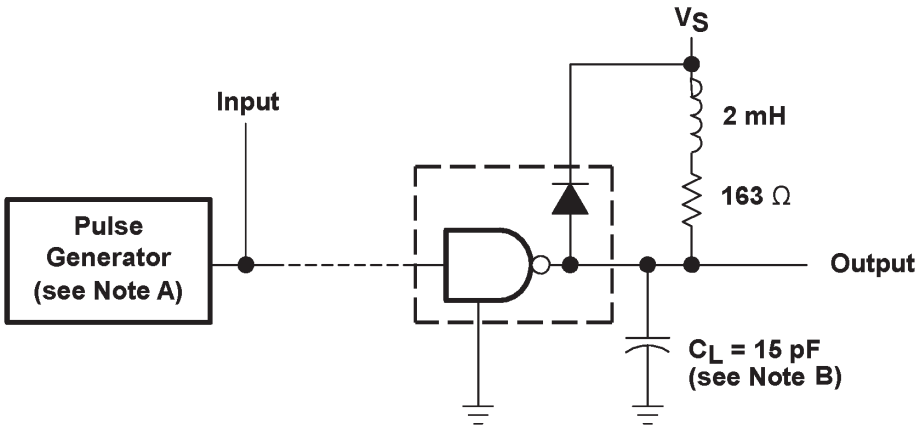
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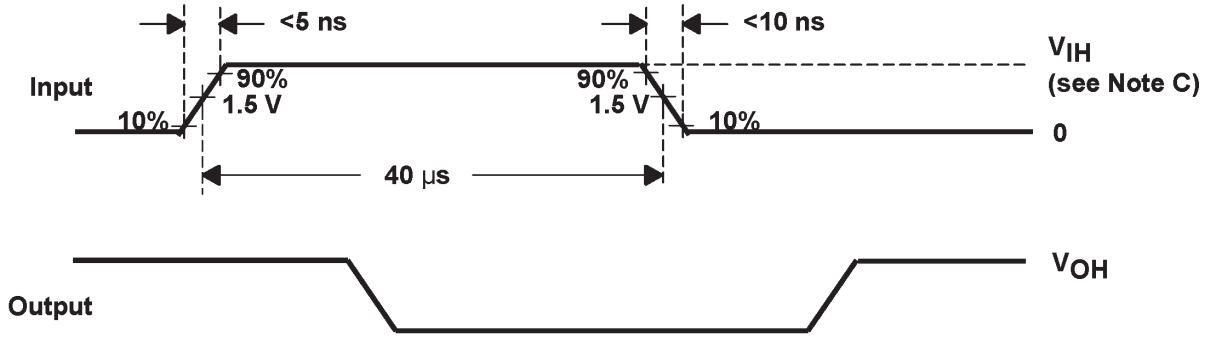
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Parameter Measurement Information

Parameter Measurement Information (continued)



Test Circuit



Voltage Waveforms

A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

C. V_{IH} = 3 V

Figure 11. Latch-Up Test

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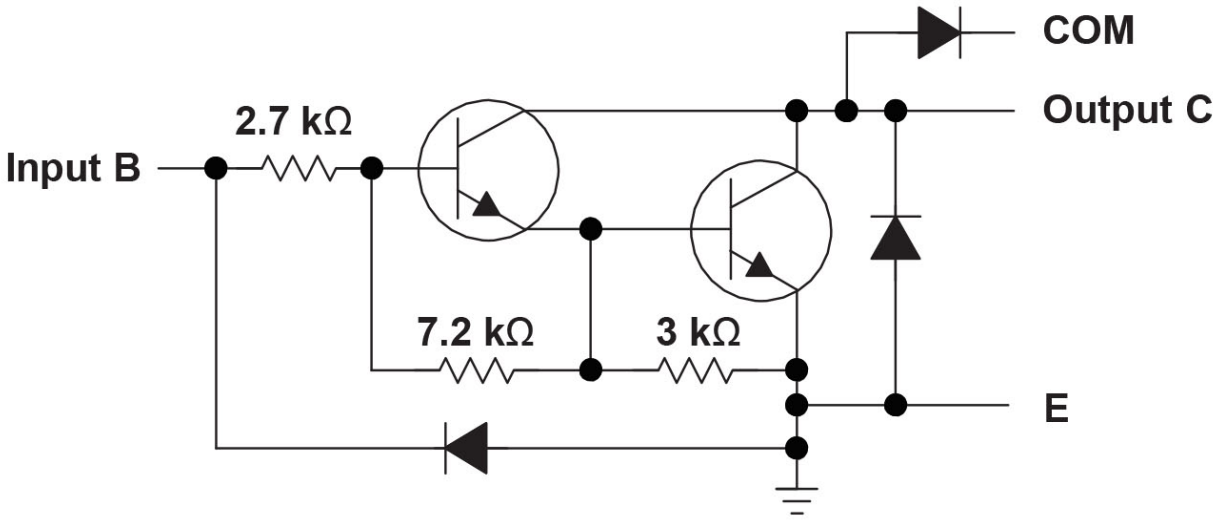
Detailed Description

Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This is due to its integration of 8 Darlington transistors that are capable of sinking up to 500 mA and wide GPIO range capability.

The ULN2803A is comprised of eight high voltage, high current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The ULN2803A has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V or 3.3 V. The ULN2803A offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

Functional Block Diagram



Feature Description

Each channel of ULN2803A consists of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very-high current gain. The very high β allows for high output current drive with a very-low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current through the 2.7-kΩ resistor connected between the input and base of the predriver Darlington NPN.

The diodes connected between the output and COM pin are used to suppress the kick-back voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply through the kick-back diode.

In normal operation, the diodes on base and collector pins to emitter will be reverse biased. If these diode are forward biased, internal parasitic NPN transistors will draw (a nearly equal) current from other (nearby) device pins.

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Device Functional Modes

Inductive Load Drive

When the COM pin is tied to the coil supply voltage, ULN2803A is able to drive inductive loads and suppress the kick-back voltage through the internal free wheeling diodes.

Resistive Load Drive

When driving resistive loads, COM can be left unconnected or connected to the load voltage supply. If multiple supplies are used, connect to the highest voltage supply.

Application and Implementation

Application Information

ULN2803A will typically be used to drive a high voltage and/or current peripheral from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of ULN2803A, driving inductive loads. This includes motors, solenoids, and relays. Each load type can be modeled by what is seen in Figure 12.

Typical Application

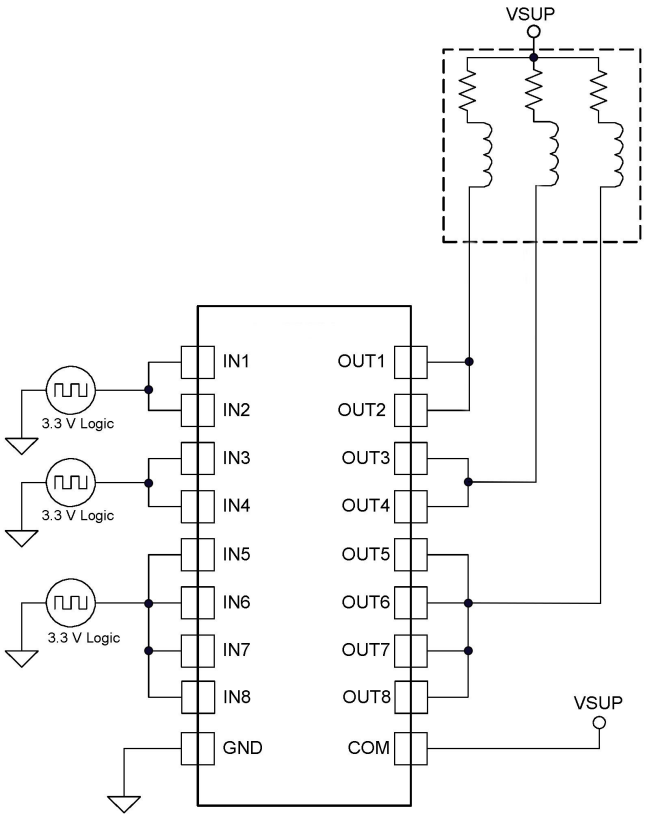


Figure 12. ULN2803A as Inductive Load Driver

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Typical Application (continued)

Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

DESIGN PARAMETER	EXAMPLE VALUE
GPIO voltage	3.3 or 5 V
Coil supply voltage	12 to 50 V
Number of channels	8
Output current (RCOIL)	20 to 300 mA per channel
Duty cycle	100%

Detailed Design Procedure

When using ULN2803A in a coil driving application, determine the following:

- Input voltage range
- Temperature range
- Output and drive current
- Power dissipation

Drive Current

The coil current is determined by the coil voltage (V_{SUP}), coil resistance, and output low voltage (V_{OL} or $V_{CE(SAT)}$).

$I_{COIL} = (V_{SUP} - V_{CE(SAT)}) / R_{COIL}$

Output Low Voltage

The output low voltage (V_{OL}) is the same thing as $V_{CE(SAT)}$ and can be determined by Figure 1, Figure 2, or Electrical Characteristics.

Power Dissipation and Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. To determine the number of coils possible, use Equation 2 to calculate ULN2803A on-chip power dissipation P_D. $P_D=\sum_{i=1}^{N}(V_{OLi})xI_{Li}$

where:

- N is the number of channels active together.
- VOLi is the OUTi pin voltage for the load current ILi. This is the same as $V_{CE(SAT)}$

To ensure the reliability of ULN2803A and the system, the on-chip power dissipation must be lower that or equal to the maximum allowable power dissipation (PD) dictated by Equation 3. $P_{D(MAX)}=(T_{J(MAX)}-T_A)/\theta_{JA}$.

where:

- $T_{J(MAX)}$ is the target maximum junction temperature.
- T_A is the operating ambient temperature.
- θ_{JA} is the package junction to ambient thermal resistance.

TI recommends to limit ULN2803A IC's die junction temperature to <125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

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Application Curves

The following curves were generated with ULN2803A driving an OMRON G5NB relay - Vin = 5.0 V; Vsup= 12 V and R_{COIL} =2.8 kΩ

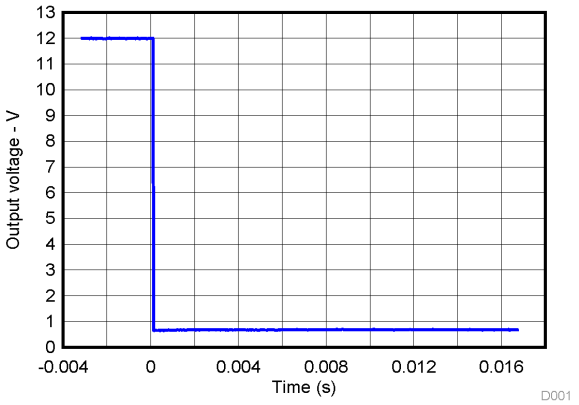


Figure 13. Output Response With Activation of Coil (Turn On)

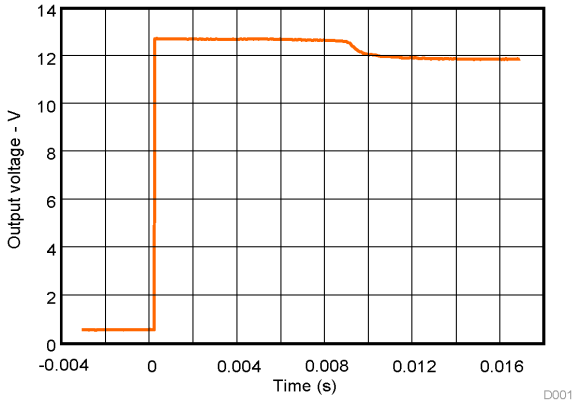


Figure 14. Output Response With De-Activation of Coil (Turn Off)

Power Supply Recommendations

This part does not need a power supply; however, the COM pin is typically tied to the system power supply. When this is the case, make sure that the output voltage does not heavily exceed the COM pin voltage. This will heavily forward bias the flyback diodes and cause a large current to flow into COM, potentially damaging the on- chip metal or overheating the part.

Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive ULN2803A. Take care to separate the input channels as much as possible, as to eliminate crosstalk. TI recommends thick traces for the output, in order to drive high currents as desired. Wire thickness can be determined by the trace material's current density and desired drive current.

Because all of the channels currents return to a common emitter, it is best to size that trace width to be very wide. Some applications require up to 2.5 A.

Layout Example

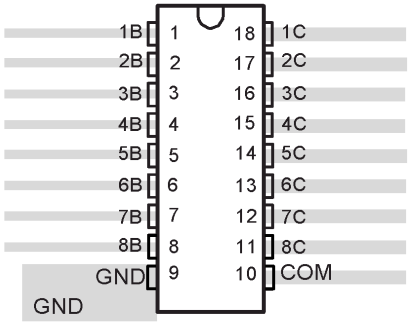


Figure 15. Package Layout

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Device and Documentation Support

Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

Glossary

SLYZ022— Glossary .

This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation..

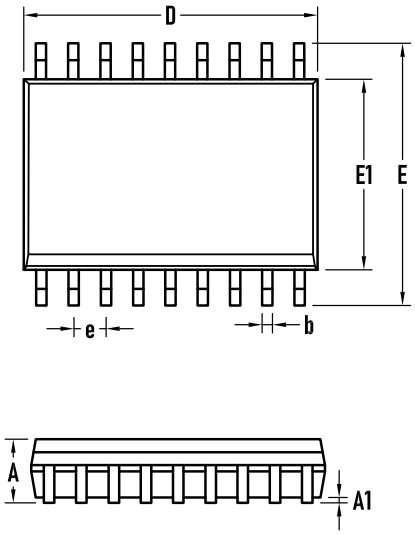
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ULN2803A

Darlington Transistor Arrays

SOP18 Package Specifications



SYMBOL	MIN.	TYP.	MAX.
A	–	–	2.65
A1	0.10	–	0.30
b	0.31	–	0.51
D	11.35	–	11.75
E	9.97	–	10.63
E1	7.40	–	7.60
e	1.27BSC		
L	0.40	–	1.27
θ	0	–	8°

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