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PRODUCT SPECIFICATION

Customer : _____

Product Name : Real Time Clock

Part NO : FRTC4100S

Issue Date : _____

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Prepared	Checked	Customer Check
ChenTT	Zelig	

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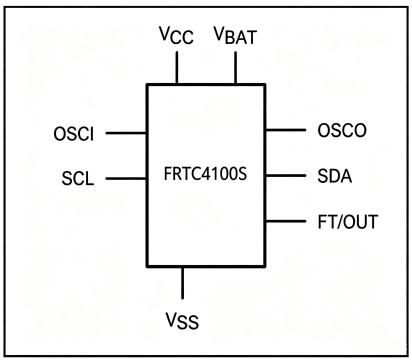
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1 Features

- 2.0 to 5.5 V clock operating voltage
- Counters for seconds, minutes, hours, day, date, month, years and century
- Year 2000 COMPLIANT
- Software clock calibration to
- compensate crystal deviation duetotemperature
- Automatic switchover and deselect circuitry
- Serial interface supports I2C bus (400 kHz protocol)
- Ultra-low battery supply current of 0.4 µA (typ. at 3 V)
- Low operating current of 150uA
- Battery of Super-cap back-up
- 32 KHz crystal oscillator integrating load capacitance (12.5 pF) providing
- exceptional oscillator stability and
- high crystal series
- Special software programmable output
- Automatic leap year compensation
- Operating temperature of -40 to 85° C

2 Logic Diagram



3 Description

The FRTC4100S is a low-power serial real-time clock (RTC). It features a built-in 32.768kHz oscillator (controlled by an external crystal), and the first 8 bytes of its RAM are allocated for the clock/calendar function, configured in binary-coded decimal (BCD) format. Address and data transfers are carried out serially through a two-line bidirectional bus. The internal address register is automatically incremented following each data byte write or read.

The FRTC4100S clock incorporates an internal power detection circuit that identifies power loss and seamlessly transitions to battery backup when a power failure occurs. The energy required to maintain clock operation can be provided by a compact lithium coin cell.

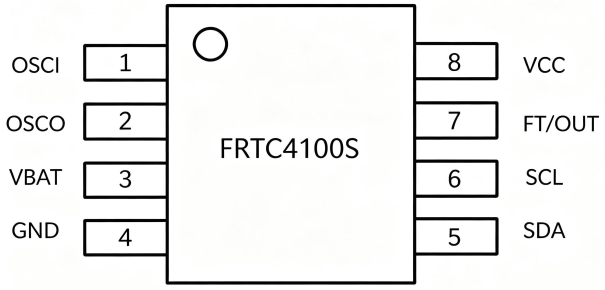
With a 3V lithium cell rated at 50 mA/h, typical data retention duration exceeds 5 years.

4 Ordering Information

Ordering Code	Package	Package Description
FRTC4100S	SOP8	pitch 1.27mm

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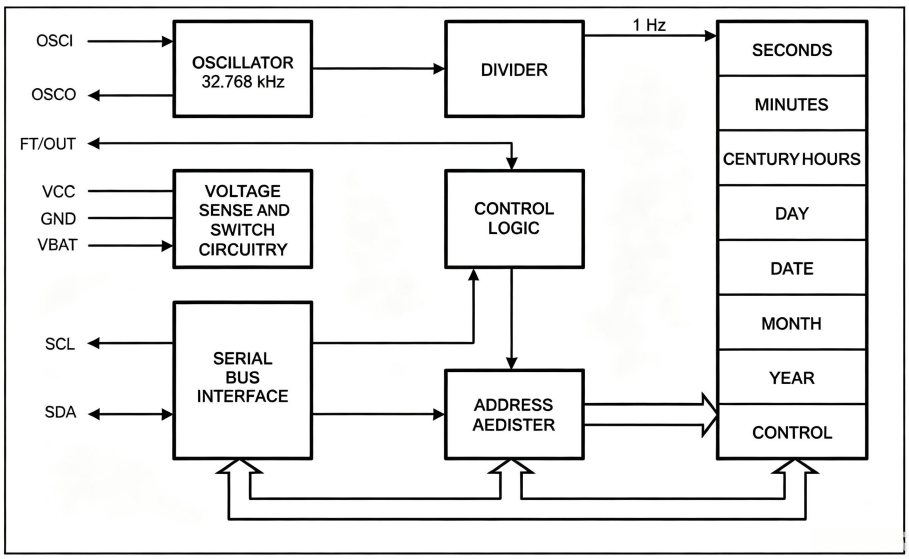
5 Pin Configuration



SOP8 (Top view)

Pin Name	Pin No.	Type	Description
OSCI	1	Input	Oscillator input
OSCO	2	Output	Oscillator output
VBAT	3	Power	Battery supply voltage
GND	4	GND	Ground
SDA	5	I/O	Serial data address input/output
SCL	6	Input	Serial clock.
FT/OUT	7	Output	Frequency test/output driver (open drain)
VCC	8	Power	Supply voltage

6 Block Diagram



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6.1 Maximum Ratings

Symbol	Parameter	Min	TYP	Max	Unit
T_{store}	Storage Temperature	-55	_	+150	° C
V_{CC}	DC Supply Voltage	-0.3	_	6.0	V
V_{IO}	Input / Output Voltage	-0.3	_	6.0	V
IO	Output Current			20	mA

Notes:
Applying stress levels beyond those specified in the MAXIMUM RATINGS table may result in permanent damage to the device. These values are stress limits only, and proper functional operation of the device at these or any other conditions exceeding those stated in the operational sections of this specification is not guaranteed. Prolonged exposure to absolute maximum rating conditions may degrade device reliability.

6.2 Recommended operation conditions

Symbol	Parameter	Min	TYP	Max	Unit
V_{CC}	V_{CCA} Positive DC Supply Voltage	2.0	_	5.5	V
V_{IO}	I/O Pin Voltage	GND	_	5.5	V
T_A	Operating Temperature Range	-40	_	+85	° C

7 DC Electrical Characteristics

7.1 DC characteristics

Symbol	Parameter	Test Condition* 1	Min	Typ	Max	Unit
I_{LI}	Input leakage current	$0V \leqslant VIN \leqslant V_{CC}$			±1	μA
I_{LO}	Output leakage current	$0V \leqslant VOUT \leqslant V_{CC}$			±1	μA
I_{CC}	Supply current	Switch frequency = 400 kHz			150	μA
V_{IL}	Input low voltage		-0.3		$0.3*V_{CC}$	V
V_{IH}	Input high voltage		$0.7*V_{CC}$		V_{CC} + 0.5	V
V_{OL}	Output low voltage	I_{OL} = 3 mA			0.4	V
V_{PU}	Pull-up supply voltage (open drain)	FT/OUT			5.5	V
V_{BAT}	Battery supply voltage		2.5*2	3	3.5*3	V
I_{BAT}	Battery supply current	TA = 25 ° C, V_{CC} = 0 V, oscillator ON, V_{BAT} = 3 V		0.4	1	μA

Note:
1. Applies within the ambient operating temperature range of TA = -40 to 85° C and VCC = 2.0 to 5.5 V (unless otherwise specified).
2. Following switchover (VSO), VBAT(min) may be as low as 2.0 V when using a crystal with RS = 40 KΩ.
3. For rechargeable backup configurations, VBAT(max) may be treated as equivalent to VCC..

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7.2 Capacitance

Symbol	Parameter*1*2	Min	Max	Unit
C_{IN}	Input capacitance (SCL)		7	pF
C_{OUT}	Output capacitance (SDA, FT/OUT)		10	pF

7.3 Crystal electrical characteristics

Symbol	Parameter* 1*2	Min	Typ	Max	Unit
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance			100	kΩ
C_L	Load capacitance		12.5		pF

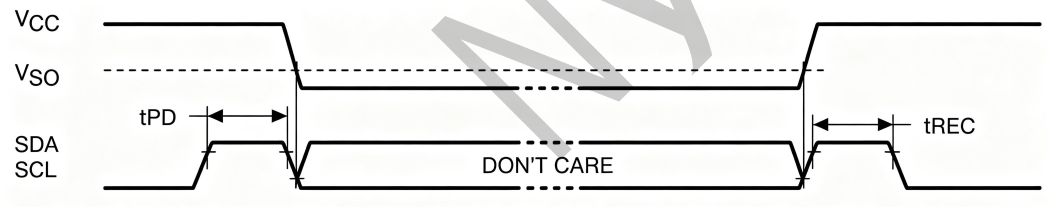
Note:

1. When the SOIC8 package is used, these values must be provided externally.
2. The load capacitors are built into the FRTC4100S. When laying out the circuit board for the 32.768 kHz crystal, careful attention should be given to keeping trace lengths to a minimum and isolating the crystal from signals that generate RF interference.

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7.4 AC Electrical characteristics

Power down/up mode AC waveforms



7.5 Power down/up AC characteristics

Symbol	Parameter*1*2	Min	Max	Unit
t_{PD}	SCL and SDA at VIH before power down	0		ns
t_{REC}	SCL and SDA at VIH after power up	10		μs

Note

1. Valid for ambient operating temperature: TA = -40 to 85° C; VCC = 2.0 to 5.5 V (except where noted).
2. VCC fall time should not exceed 5 mV/μs.

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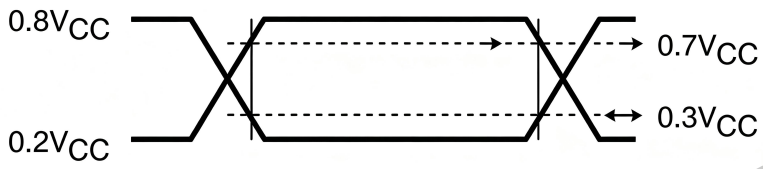
7.6 Power down/up trip points DC characteristics

Symbol	Parameter*1*2		Min	Typ	3 Max*	Unit
V_{SO}	Battery backup switchover voltage		V_{BAT} - 0.80	V_{BAT} - 0.50	V_{BAT} - 0.30	V

Note

1. Valid for ambient operating temperature: TA = -40 to +85° C; VCC = 2.0 to 5.5 V (except where noted).
2. All voltages referenced to GND.
3. In 3.3 V application, if initial battery voltage is 3.4 V, it may be necessary to reduce battery voltage (i.e.,through wave soldering the battery) in order to avoid inadvertent switchover/deselection for VCC - 10% operation.
4. Switchover and deselect point.

7.7 AC testing input/output waveform



Parameter	FRTC4100S	Unit
Input rise and fall times	⩽ 50	ns
Input pulse voltages	0.2Vcc to 0.8V cc	V
Input and output timing ref. voltages	0.3Vcc to 0.7Vcc	V

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7.8 I2C AC Characteristics

(TA = -40 ° C to +85 ° C) *1

Symbol	Parameter	Test Conditions*1	MIN	TYP	MAX	Unit
f_{SCL}	SCL Clock Frequency	Fast mode	100		400	kHz
		Standard mode			100	kHz
t_{BUF}	Bus Free Time Between STOP and START Condition	Fast mode	1.3			μs
		Standard mode	4.7			
$t_{HD:STA}$	Hold Time (Repeated) START Condition*2	Fast mode	0.6			μs
		Standard mode	4.0			
t_{LOW}	LOW Period of SCL Clock	Fast mode	1.3			μs
		Standard mode	4.7			

t_{HIGH}	HIGH Period of SCL Clock	Fast mode	0.6			μs
		Standard mode	4.0			
$t_{SU:STA}$	Setup Time for Repeated START Condition	Fast mode	0.6			μs
		Standard mode	4.7			
$t_{HD:DAT}$	Data Hold Time* 3/4	Fast mode	0		0.9	μs
		Standard mode	0			
$t_{SU:DAT}$	Data Setup Time*5	Fast mode	100			ns
		Standard mode	250			
t_R	Rise Time of Both SDA and SCL Signals *6	Fast mode	20 + 0.1CB		300	ns
		Standard mode	20 + 0.1CB		1000	
t_F	Fall Time of Both SDA and SCL Signals *6	Fast mode	20 + 0.1CB		300	ns
		Standard mode	20 + 0.1CB		300	
$t_{SU:STO}$	Setup Time for STOP Condition	Fast mode	0.6			μs
		Standard mode	4.0			
C_B	Capacitive Load for Each Bus Line*6				400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL) *7				10	pF
t_{OSF}	Oscillator Stop Flag (OSF) Delay* 8			100		ms

Note:

1. The limits at -40° C are ensured by design and are not verified through production testing.
2. Following this interval, the first clock pulse is produced.
3. A device must internally maintain a hold time of at least 300ns for the SDA signal (referenced to VIHMIN of the SCL signal) in order to bridge the undefined region of the SCL falling edge.
4. The maximum tHD:DAT requirement only needs to be satisfied if the device does not extend the LOW period (tLOW) of the SCL signal.
5. A fast-mode device may be employed in a standard-mode system, provided that the requirement tSU:DAT ≥ 250ns is met. This condition is automatically satisfied if the device does not extend the LOW period of the SCL signal. If such a device does extend the LOW period of the SCL signal, it must deliver the next data bit to the SDA line tR MAX + tSU:DAT = 1000 + 250 = 1250ns prior to the SCL line being released.
6. CB—represents the total capacitance of a single bus line in pF.
7. Ensured by design. Not verified through production testing.
8. The parameter tOSF refers to the duration for which the oscillator must be halted in order for the OSF flag to be set, across the voltage range of 0.0V ≤ VCC ≤ VCC MAX and 2.5V ≤ VBAT ≤ 3.5V.

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8 Application Information

8.1 Operation

The FRTC4100S clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 64 bytes contained in the device can then be accessed sequentially in the following order:

1st byte: seconds register
2nd byte: minutes register
3rd byte: century/ hours register
4th byte: day register
5th byte: date register
6th byte: month register
7th byte: years register
8th byte: control register

The FRTC4100S clock continuously monitors VCC for any out-of-tolerance condition. If VCC drops below VSO, the device immediately halts any access in progress and resets the device address counter.
During this period, inputs to the device will not be acknowledged, thereby preventing erroneous data from being written to the device by an out-of-tolerance system.
When VCC drops below VSO, the device automatically transitions to the battery supply and enters an ultra-low current mode to preserve battery life.
At power-up, the device switches from the battery back to VCC at VSO and resumes recognizing inputs.

8.2 2-wire bus characteristics

This bus is designed for communication between different ICs. It comprises two lines: one bidirectional line for data signals (SDA) and one line for clock signals (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage through a pull-up resistor.
The following protocol has been established:

- Data transfer may only be initiated when the bus is not busy.
- While data is being transferred, the data line must remain stable whenever the clock line is high.
- Any change in the data line while the clock line is high will be treated as a control signal. Based on this, the following bus conditions have been defined:

8.2.1 Bus not busy

Both data and clock lines remain high.

8.2.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition .

8.2.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition .

8.3 Data valid

The data line is considered to carry valid data when, following a start condition, it remains stable throughout the high period of the clock signal. The data on the line may be altered during the low period of the clock signal. One clock pulse is provided for each bit of data.
Every data transfer begins with a start condition and ends with a stop condition. The number of data bytes transferred between the start and stop conditions is not restricted. Information is transmitted in byte-wide units, and each receiver acknowledges with a ninth bit.
By definition, a device that sends out a message is referred to as a ″transmitter,″ while the receiving device that accepts the message is called a ″receiver.″ The device that manages the message is termed a ″master,″ and the devices governed by the master are known as ″slaves.″ ″ .

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8.4 Acknowledge

Every byte of eight bits is followed by a single acknowledge bit. This acknowledge bit is a low level placed on the bus by the receiver, while the master generates an additional acknowledge-related clock pulse.

A slave receiver that has been addressed is required to generate an acknowledge after receiving each byte. Likewise, a master receiver must generate an acknowledge after receiving each byte that has been clocked out of the slave transmitter.

The acknowledging device must pull the SDA line low during the acknowledge clock pulse so that the SDA line remains a stable low throughout the high period of the acknowledge-related clock pulse. Naturally, setup and hold times must be taken into account. A master receiver must indicate end-of-data to the slave transmitter by not generating an acknowledge on the final byte that has been clocked out of the slave. In this situation, the transmitter must keep the data line high so that the master can generate the STOP condition.

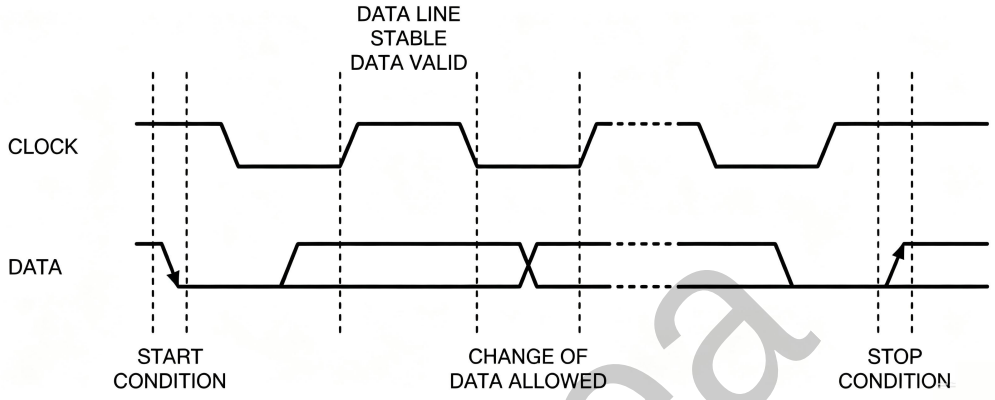
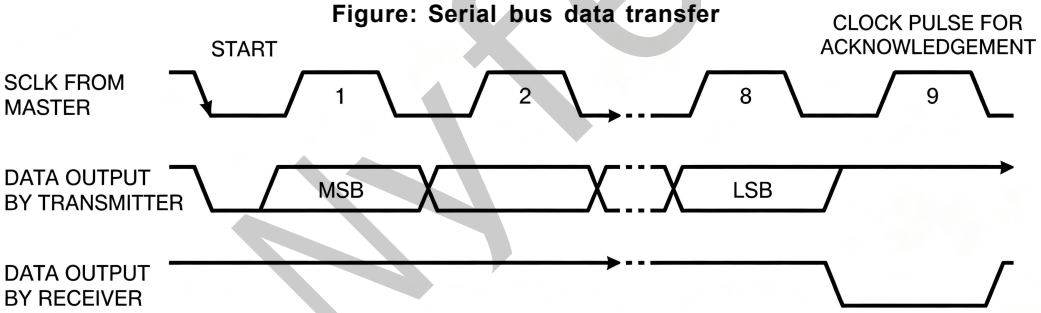
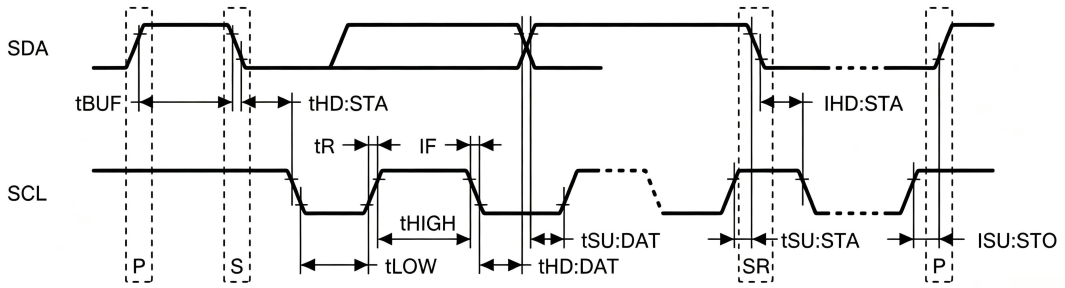


Figure: Serial bus data transfer



sequence **Figure: Acknowledgement**



sequenc

Figure: Bus timing requirements sequence

8.5 Read mode

In this mode, the master reads from the FRTC4100S slave after first setting the slave address. Following the write-mode control bit (R/W = 0) and the acknowledge bit, the word address An is written into the on-chip address pointer. The START condition and slave address are then repeated, followed by the READ-mode control bit (R/W = 1). At this point, the master transmitter transitions into the master receiver. The data byte at the addressed location will be transmitted, and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is incremented only upon reception of an acknowledge bit. The FRTC4100S slave transmitter will then place the data byte at address An + 1 onto the bus. The master receiver reads and acknowledges the new byte, and the address pointer is incremented to An + 2.

This sequence of reading consecutive addresses continues until the master receiver issues a STOP condition to the slave transmitter.

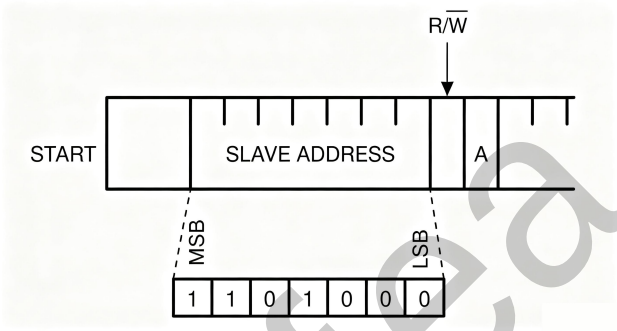


Figure: Slave address location

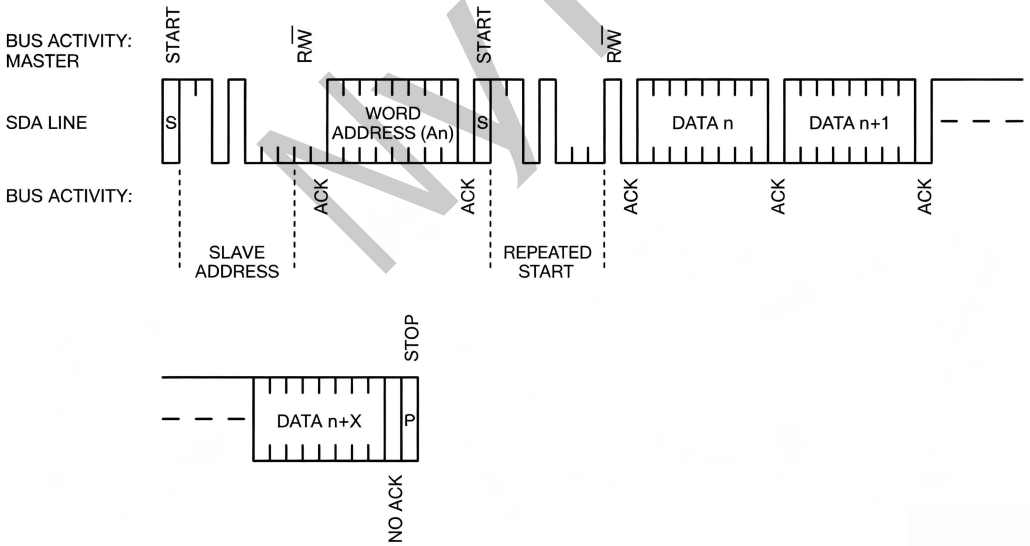


Figure: Read Mode Sequence

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8.6 Write mode

In this mode, the master transmitter sends data to the FRTC4100S slave receiver. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus, indicating to the addressed device that word address An will follow and is to be written into the on-chip address pointer. The data word to be written to memory is strobed in next, and the internal address pointer is incremented to the next memory location within the RAM upon reception of an acknowledge clock. The FRTC4100S slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address, and again after it has received the word address and each data byte.

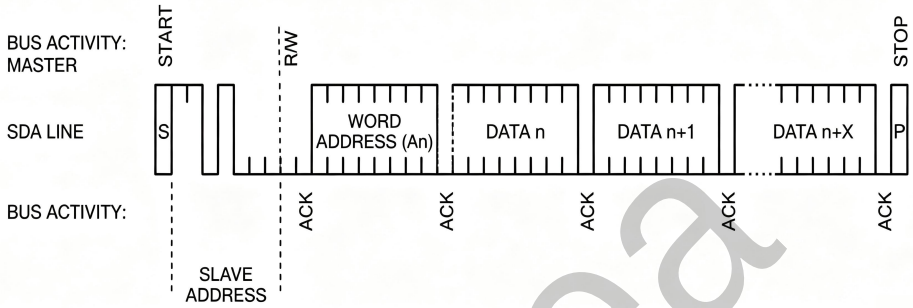


Figure: Write mode sequence

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8.7 Clock Operation

The eight-byte clock register (refer to Table 3) is used both to set the clock and to read the date and time from the clock in binary-coded decimal format. Seconds, minutes, and hours are held within the first three registers. Bits D6 and D7 of clock register 2 (the hours register) contain the CENTURY ENABLE bit (CEB) and the CENTURY bit (CB). Setting CEB to a '1' will cause CB to toggle—either from '0' to '1' or from '1' to '0'—at the turn of the century, depending on its initial state. If CEB is set to a '0', CB will not toggle. Bits D0 through D2 of register 3 hold the day (day of week). Registers 4, 5, and 6 contain the date (day of month), month, and years. The final register is the control register (described in the clock calibration section). Bit D7 of register 0 contains the STOP bit (ST). Setting this bit to a '1' causes the oscillator to stop. If the device is expected to remain on the shelf for a significant period, the oscillator may be halted to reduce current drain. When reset to a '0', the oscillator restarts within one second.

Note: To guarantee oscillator startup after the initial power-up, set the ST bit to a '1,' then reset it to a '0.' This sequence activates a "kick start" circuit that assists oscillator startup under worst-case voltage and temperature conditions.

The seven clock registers may be read one byte at a time or as a sequential block. The control register (address location 7) can be accessed independently. Provisions have been made to ensure that a clock update does not occur while any of the seven clock addresses are being read. If a clock address is being read, an update of the clock registers will be delayed by 250 ms to allow the read to complete before the update takes place. This prevents data from transitioning during the read.

Note: This 250 ms delay affects only the clock register update and does not alter the actual clock time.

Address	Data*1								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
0	ST	10 seconds			Seconds				Seconds	00-59
1	X	10 minutes			Minutes				Minutes	00-59
2	CEB*2	CB	10 hours		Hours				Century/hours	0-1/00-23
3	X	X	X	X	X	Day			Day	01-07
4	X	X	10 date		Date				Date	01-31
5	X	X	X	10 M.	Month				Month	01-12
6	10 years				Years				Year	00-99
7	OUT	FT	S	Calibration					Control	

Note

1. Keys:
   S = SIGN bit
   FT = FREQUENCY TEST bit
   ST = STOP bit
   OUT = Output level
   X = Don' t care
   CEB = Century enable bit CB = Century bit
2. When CEB is set to '1', CB will toggle from '0' to '1' or from '1' to '0' every 100 years (depending on the initial value that was set). When CEB is set to '0', CB will not toggle.

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8.8 Clock Calibration

The FRTC4100S is driven by a quartz-controlled oscillator operating at a nominal frequency of 32,768 Hz. These devices are tested to exhibit no more than 35 ppm (parts per million) of oscillator frequency error at 25° C, which corresponds to roughly ±1.53 minutes per month. When the calibration bits are properly configured, the accuracy of each FRTC4100S improves to better than ±2 ppm at 25° C.

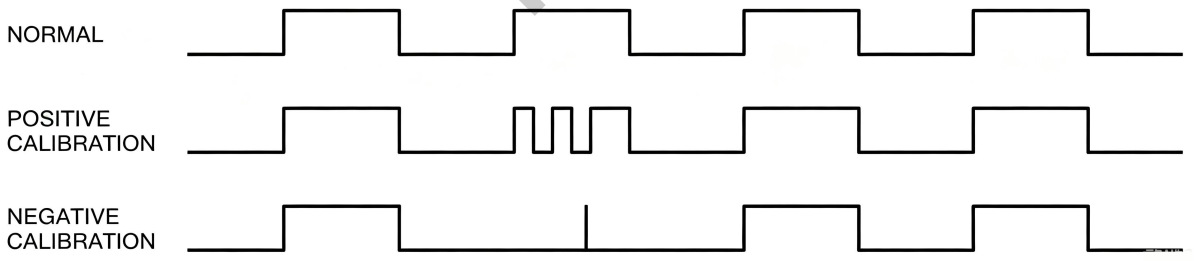
The oscillation rate of any crystal varies with temperature. Most clock chips attempt to compensate for crystal frequency and temperature drift using cumbersome trim capacitors. The FRTC4100S design, however, relies on periodic counter correction. The calibration circuit adds to or subtracts from the oscillator divider circuit at the divide-by-256 stage. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends on the value loaded into the five-bit calibration byte located in the control register. Adding counts speeds the clock up, while subtracting counts slows the clock down.

The calibration byte occupies the five lower-order bits (D4 - D0) in the control register (address 7). This byte can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit: '1' indicates positive calibration, while '0' indicates negative calibration. Calibration takes place within a 64-minute cycle. During the first 62 minutes of the cycle, one second may be either shortened by 128 or lengthened by 256 oscillator cycles, once per minute. If a binary '1' is loaded into the register, only the first 2 minutes of the 64-minute cycle will be modified; if a binary 6 is loaded, the first 12 minutes will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles—that is, +4.068 or -2.034 ppm of adjustment per calibration step in the calibration register. Assuming the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or -5.35 seconds per month, which corresponds to a total range of +5.5 or -2.75 minutes per month.

Two methods are available for determining how much calibration a given FRTC4100S may require. The first involves simply setting the clock, letting it run for a month, and comparing it to a known accurate reference (such as WWV broadcasts). While this may seem crude, it allows the designer to give the end user the ability to calibrate the clock as their environment may require, even after the final product is packaged in a non-user-serviceable enclosure. All the designer has to do is provide a simple utility that accesses the calibration byte.

The second approach is better suited to a manufacturing environment and involves the use of test equipment. When the frequency test (FT) bit, the seventh-most significant bit in the control register, is set to a '1', and the oscillator is running at 32,768 Hz, the FT/OUT pin of the device will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 ppm oscillator frequency error, requiring a -10 (XX001010) to be loaded into the calibration byte for correction. Note that setting or changing the calibration byte does not affect the frequency test output frequency..



8.9 Output driver pin

When the FT bit is not set, the FT/OUT pin functions as an output driver that reflects the contents of D7 of the control register. In other words, when D6 of location 7 is a zero and D7 of location 7 is a zero, the FT/OUT pin will be driven low.

Note:

The FT/OUT pin is open drain which requires an external pull-up resistor.

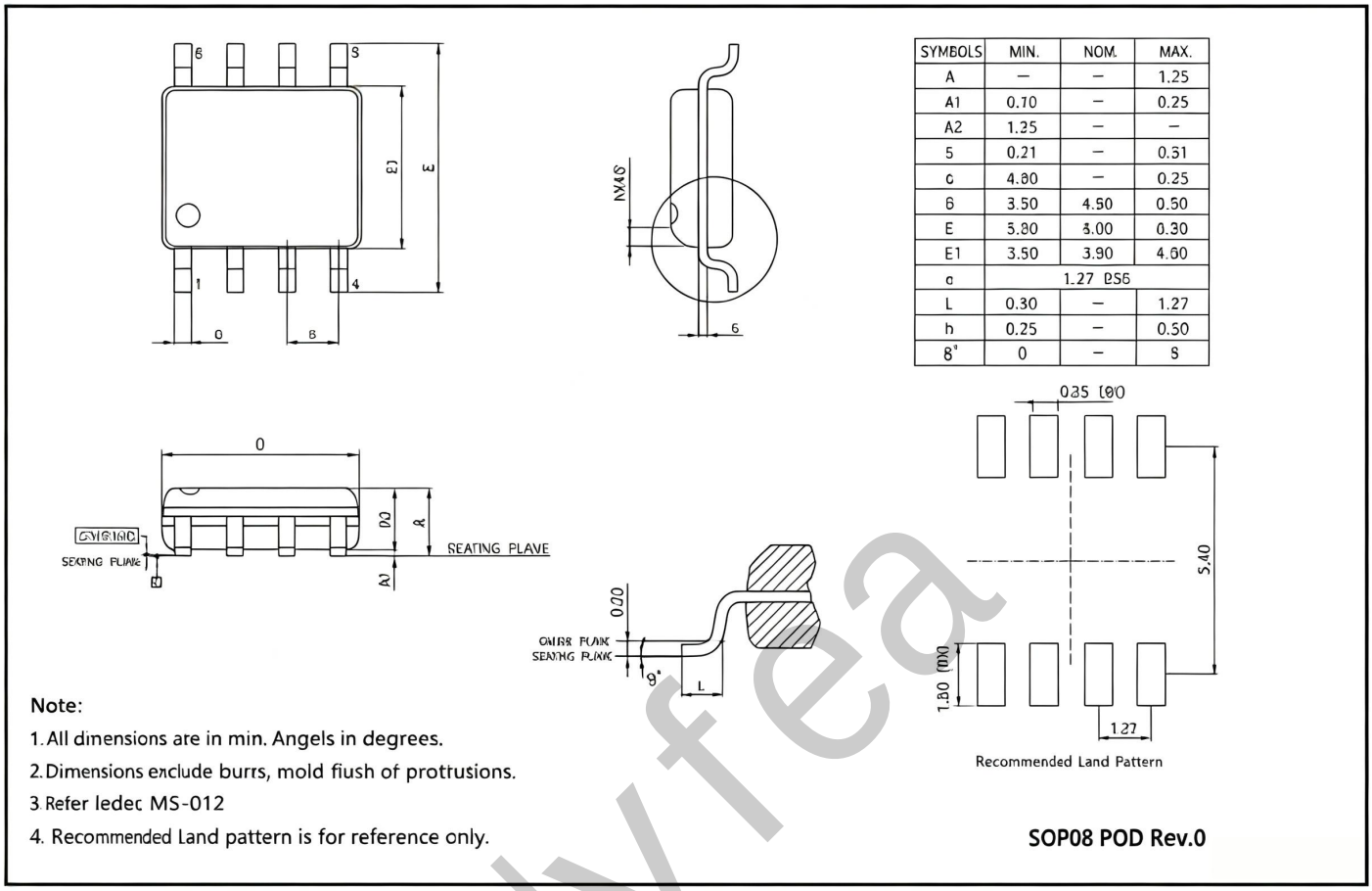
8.10 Preferred initial power-on defaults

Upon initial application of power to the device, the FT bit will be set to a '0' and the OUT bit will be set to a ' 1'. All other register bits will initially power on in a random state.

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9 Package Information

FRTC4100S SOP8 Package



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.25
A1	0.10	—	0.25
A2	1.25	—	—
b	0.21	—	0.31
c	4.80	—	0.25
D	3.50	4.50	0.50
E	5.80	3.00	0.30
E1	3.50	3.90	4.00
e	1.27 BSC		
L	0.30	—	1.27
h	0.25	—	0.50
θ°	0	—	8

Note:

1. All dimensions are in min. Angels in degrees.
2. Dimensions exclude burrs, mold flush of protrusions.
3. Refer Iedec MS-012
4. Recommended Land pattern is for reference only.

SOP08 POD Rev.0

Nyfea