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PRODUCT SPECIFICATION

Customer : _____

Product Name : Real Time Clock

Part NO : FRTC4111S

Issue Date : _____

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Prepared	Checked	Customer Check
ChenTT	Zelig	

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1 Features

- Counters for seconds, minutes, hours, day, date, month, years and century
- 32 kHz crystal oscillator integrating load capacitance (12.5 pF) providing exceptional oscillator stability and high crystal series
- Serial interface supports I2C bus (400 kHz protocol)
- Ultra-low battery supply current of 0.4 µA (typ. at 3 V)
- 2.0 to 5.5 V clock operating voltage
- Automatic switchover and deselect circuitry
- 56 bytes of general purpose RAM
- Software clock calibration to compensate crystal deviation due to temperature
- Automatic leap year compensation
- Operating temperature of -40 to 85° C

2 Applications

- Portable instruments
- Electronic metering
- Battery powered products
- Telecom equipments

3 Description

The FRTC4111S is a low-power serial real-time clock (RTC) featuring 56 bytes of NVRAM. It includes a built-in 32.768 kHz oscillator (controlled by an external crystal), and the first 8 bytes of its RAM are allocated for the clock/calendar function, configured in binary-coded decimal (BCD) format. Address and data transfers are carried out serially through a two-line bidirectional bus. The internal address register is automatically incremented following each data byte write or read.

The FRTC4111S clock incorporates an internal power detection circuit that identifies power loss and seamlessly transitions to battery backup when a power failure occurs. The energy required to sustain both RAM and clock operation can be provided by a compact lithium coin cell.

With a 3V lithium cell rated at 50 mA/h, typical data retention duration exceeds 5 years.

4 Ordering Information

Ordering Code	Package	Description
FRTC4111S	SOP8	pitch 1.27mm

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5 Block Diagram

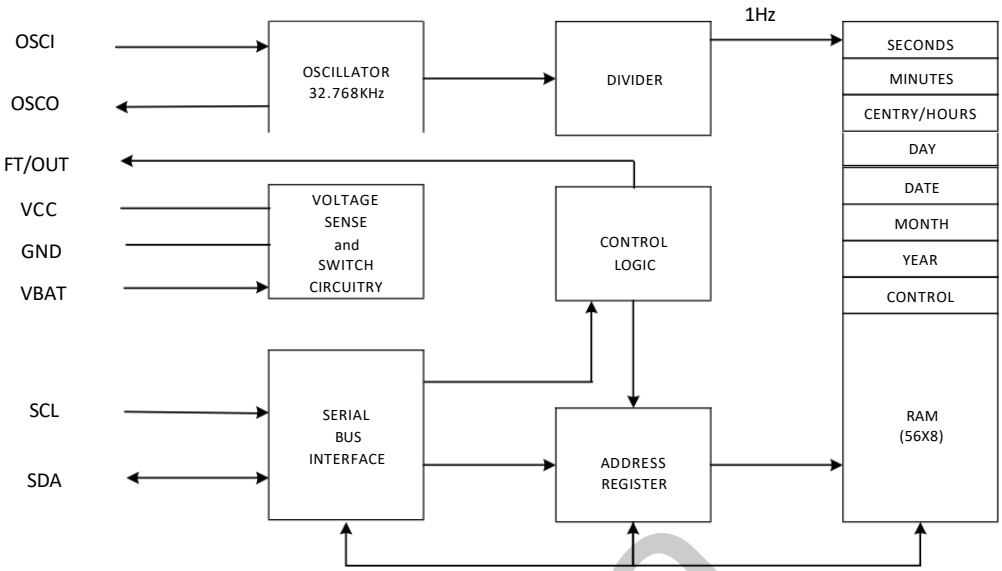


Figure 1. SOP8 Block Diagram

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6 Typical Application Circuit

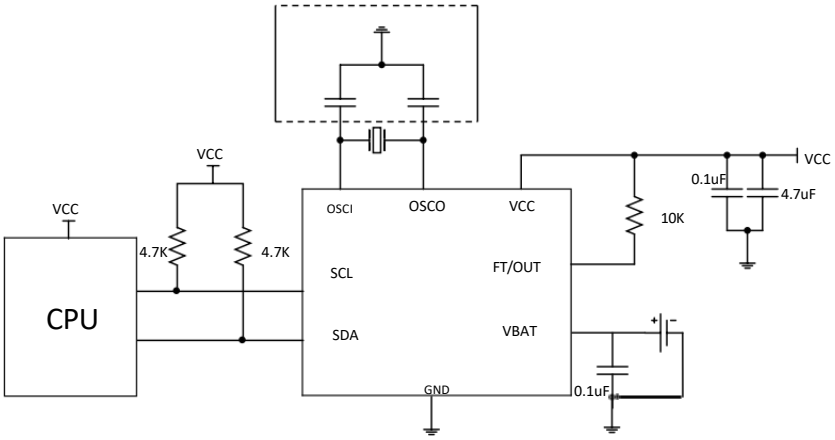


Figure 2. Typical Application Circuit

Notes:

1. FT/OUT open drain,need to add a pull resistor.
2. It is recommended to add 0.1uf capacitor to VBAT pin.

7 Pin Configuration

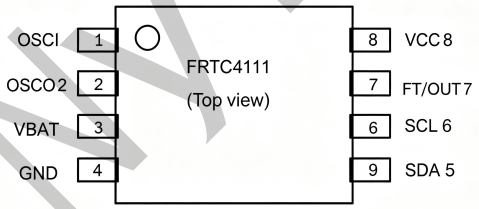


Figure 3. Pin Configuration

Pin Name	Pin No. SOP8	Type	Description
OSCI	1	Input	Oscillator input
OSCO	2	Output	Oscillator output
V_{BAT}	3	Power	Battery supply voltage
GND	4	GND	Ground
SDA	5	I/O	Serial data address input/output
SCL	6	Input	Serial clock.
FT/OUT	7	Output	Frequency test/output driver (open drain)
V_{CC}	8	Power	Supply voltage
N.C.		-	No connection

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8 Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
T_{store}	Storage Temperature	-55	_	+150	° C
V_{CC}	DC Supply Voltage	-0.3	_	6.0	V
V_{IO}	Input / Output Voltage	-0.3	_	6.0	V
IO	Output Current			20	mA

Notes:
Applying stress levels beyond those specified in the MAXIMUM RATINGS table may result in permanent damage to the device. These values are stress limits only, and proper functional operation of the device at these or any other conditions exceeding those stated in the operational sections of this specification is not guaranteed. Prolonged exposure to absolute maximum rating conditions may degrade device reliability.

9 Recommended operation conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{CC}	V_{CCA} Positive DC Supply Voltage	2.0	_	5.5	V
V_{IO}	I/O Pin Voltage	GND	_	5.5	V
T_A	Operating Temperature Range	-40	_	+85	° C

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10 DC Electrical Characteristics

10.1 DC characteristics

Symbol	Parameter	Test Condition* 1	MIN	TYP	MAX	Unit
I_{LI}	Input leakage current	0V≤VIN ≤V_{CC}			±1	μA
I_{LO}	Output leakage current	0V ≤VOUT≤V_{CC}			±1	μA
I_{CC}	Supply current	SCL clock frequency = 400 kHz			150	μA
V_{IL}	Input low voltage		-0.3		0.3*V_{CC}	V
V_{IH}	Input high voltage		0.7*V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output low voltage	I_{OL} = 3 mA			0.4	V
V_{PU}	Pull-up supply voltage (open drain)	FT/OUT			5.5	V
V_{BAT}	Battery supply voltage		2.5*2	3	3.5*3	V
I_{BAT}	Battery supply current	TA = 25 ° C, V_{CC} = 0 V, oscillator ON, V_{BAT} = 3 V		0.4	1	μA

Notes:
1. Valid for ambient operating temperature: TA = -40 to 85° C; VCC = 2.0 to 5.5 V (except where noted).
2. After switchover (V_{SO}), VBAT(min) can be 2.0 V for crystal with R_S = 40 k Ω.
3. For rechargeable back-up, VBAT(max) may be considered VCC.

10.2 Crystal electrical characteristics

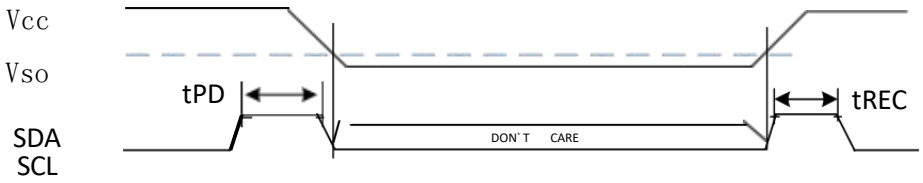
Symbol	Parameter* 1*2	MIN	TYP	MAX	Unit
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance			100	k Ω
C_L	Load capacitance		12.5		pF

Notes:
1. When the SOIC8 package is used, these values must be provided externally. The crystal selection must satisfy the conditions stated above.
2. he load capacitors are built into the FRTC4111S. When laying out the circuit board for the 32.768 kHz crystal, careful attention should be given to keeping trace lengths to a minimum and isolating the crystal from signals that generate RF interference.

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11 AC Electrical characteristics

Power down/up mode AC waveforms



11.1 Power down/up AC characteristics

Symbol	Parameter*1*2	MIN	MAX	Unit
t_{PD}	SCL and SDA at VIH before power down	0		ns
t_{REC}	SCL and SDA at VIH after power up	10		μs

Notes:
1. Valid for ambient operating temperature: TA = -40 to 85° C; VCC = 2.0 to 5.5 V (except where noted).
2. VCC fall time should not exceed 5 mV/μs.

11.2 Power down/up trip points DC characteristics

Symbol	Parameter*1*2	MIN	TYP	3 MAX*	Unit
V_{SO}	Battery backup switchover voltage	_	V_{BAT} - 0.80	_	V

Notes
1. Applies within the ambient operating temperature range of TA = -40 to +85° C and VCC = 2.0 to 5.5 V (unless otherwise specified).
2. All voltages are referenced to GND.
3. After VCC is initially powered up, I2C communication is required to perform a read/write in order to activate the oscillator.
4. When VCC < VSO, the device automatically transitions to battery mode; during this time, I2C read and write operations are not possible. Therefore, for a VCC = 3.3V application, if the initial battery voltage is ≥ VCC, it may be necessary to reduce the battery voltage.

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11.3 I2C AC Characteristics

(TA = -40 ° C to +85 ° C)

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	Unit
f_{SCL}	SCL Clock Frequency	Fast mode	100		400	kHz
		Standard mode			100	kHz
t_{BUF}	Bus Free Time Between STOP and START Condition	Fast mode	1.3			μs
		Standard mode	4.7			
$t_{HD:STA}$	Hold Time (Repeated) START Condition	Fast mode	0.6			μs
		Standard mode	4.0			
t_{LOW}	LOW Period of SCL Clock	Fast mode	1.3			μs
		Standard mode	4.7			
t_{HIGH}	HIGH Period of SCL Clock	Fast mode	0.6			μs
		Standard mode	4.0			
$t_{SU:STA}$	Setup Time for Repeated START Condition	Fast mode	0.6			μs
		Standard mode	4.7			
$t_{HD:DAT}$	Data Hold Time	Fast mode	0		0.9	μs
		Standard mode	0			
$t_{SU:DAT}$	Data Setup Time	Fast mode	100			ns
		Standard mode	250			
t_R	Rise Time of Both SDA and SCL Signals	Fast mode			300	ns
		Standard mode			1000	
t_F	Fall Time of Both SDA and SCL Signals	Fast mode			300	ns
		Standard mode			300	
$t_{SU:STO}$	Setup Time for STOP Condition	Fast mode	0.6			μs
		Standard mode	4.0			

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12 Application Information

12.1 Operation

The FRTC4111S functions as a slave device on the serial bus. Access is achieved by issuing a start condition followed by the correct slave address (D0h). The 64 bytes contained within the device can then be accessed sequentially in the following order:

- 1st byte: seconds register
- 2nd byte: minutes register
- 3rd byte: century/hours register
- 4th byte: day register
- 5th byte: date register
- 6th byte: month register
- 7th byte: years register
- 8th byte: control register
- 9th－64th bytes: RAM

The FRTC4111S continuously monitors VCC for any out-of-tolerance condition. When VCC drops below VSO, the device automatically transitions to battery mode. During this period, inputs to the device will not be acknowledged, preventing erroneous data from being written to the device. Upon power-up, the device switches from battery mode back to VCC mode when VCC > VSO and resumes recognizing inputs.

12.2 2-wire bus characteristics

This bus is designed for communication between different ICs. It comprises two lines: one bidirectional line for data signals (SDA) and one line for clock signals (SCL). Both the SDA and SCL lines must be pulled up via pull-up resistors.

The following protocol has been established:

Data transfer may be initiated only when the bus is not busy.

- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

12.2.1 Bus not busy

Both data and clock lines remain high.

12.2.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition .

12.2.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition .

12.3 Data valid

The data line is considered to carry valid data when, following a start condition, it remains stable throughout the high period of the clock signal. The data on the line may be altered during the low period of the clock signal. One clock pulse is provided for each bit of data

Every data transfer begins with a start condition and ends with a stop condition. The number of data bytes transferred between the start and stop conditions is not restricted. Information is transmitted in byte-wide units, and each receiver acknowledges with a ninth bit.

By definition, a device that sends out a message is referred to as a "transmitter," while the receiving device that accepts the message is called a "receiver." The device that manages the message is termed a "master," and the devices governed by the master are known as "slaves." .

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12.4 Acknowledge

Every byte of eight bits is followed by a single acknowledge bit. This acknowledge bit is a low level placed on the bus by the receiver, while the master generates an additional acknowledge-related clock pulse.
A slave receiver that has been addressed is required to generate an acknowledge after receiving each byte.
Likewise, a master receiver must generate an acknowledge after receiving each byte that has been clocked out of the slave transmitter.
The acknowledging device must pull the SDA line low during the acknowledge clock pulse so that the SDA line remains a stable low throughout the high period of the acknowledge-related clock pulse. Naturally, setup and hold times must be taken into account. A master receiver must indicate end-of-data to the slave transmitter by not generating an acknowledge on the final byte that has been clocked out of the slave. In this situation, the transmitter must keep the data line high so that the master can generate the STOP condition.

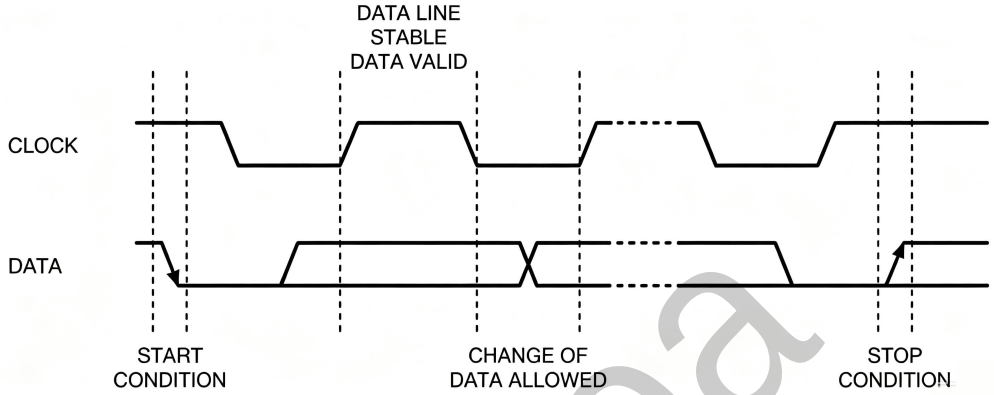


Figure4: Serial bus data transfer sequence

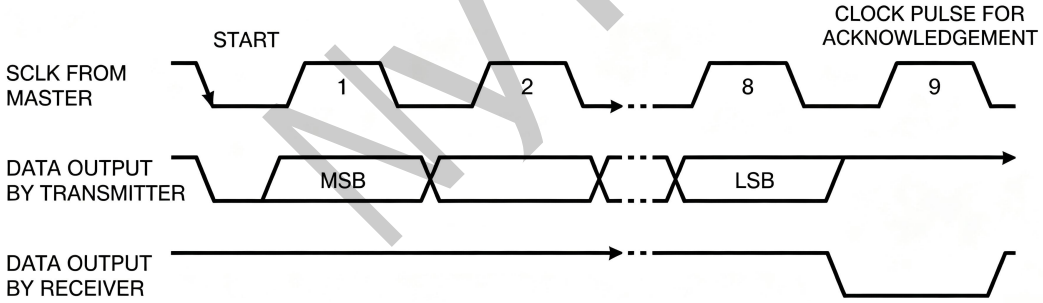


Figure5: Acknowledgement Sequence

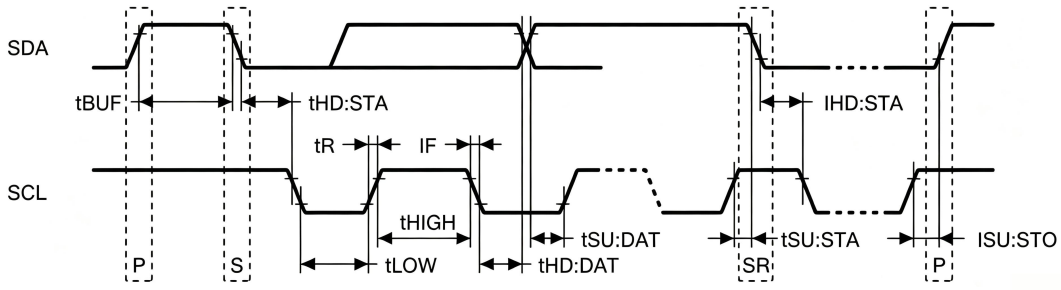


Figure6: Bus timing requirements sequence

12.5 Read mode

In this mode, the master reads from the FRTC4111S slave after first setting the slave address. Following the write-mode control bit (R/W = 0) and the acknowledge bit, the word address An is written into the on-chip address pointer. The START condition and slave address are then repeated, followed by the READ-mode control bit (R/W = 1). At this point, the master transmitter transitions into the master receiver. The data byte at the addressed location will be transmitted, and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is incremented only upon reception of an acknowledge bit. The FRTC4111S slave transmitter will then place the data byte at address An + 1 onto the bus. The master receiver reads and acknowledges the new byte, and the address pointer is incremented to An + 2.

This sequence of reading consecutive addresses continues until the master receiver issues a STOP condition to the slave transmitter.

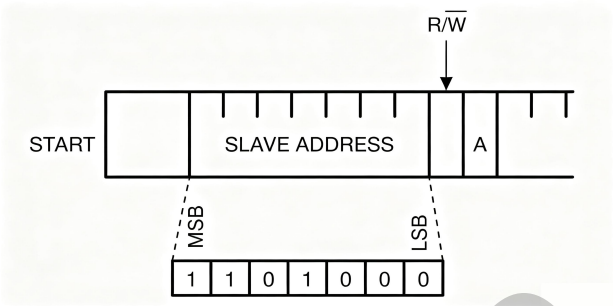


Figure7: Slave address location

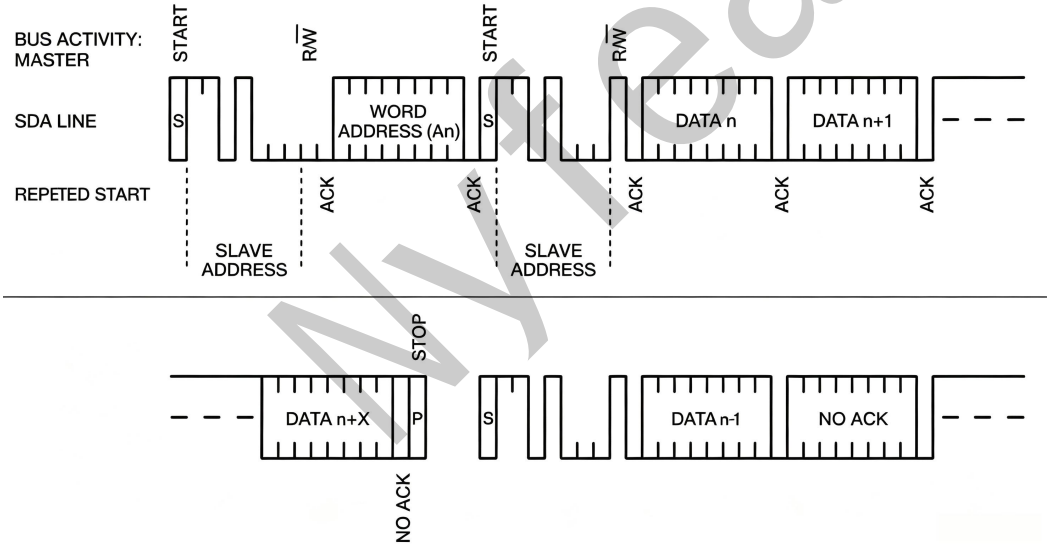


Figure8: Read Mode Sequence

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12.6 Write mode

In this mode, the master transmitter sends data to the FRTC4111S slave receiver. Following the START condition and slave address, a logic '0' (R/W = 0) is placed on the bus, indicating to the addressed device that word address An will follow and is to be written into the on-chip address pointer. The data word to be written to memory is strobed in next, and the internal address pointer is incremented to the next memory location within the RAM upon reception of an acknowledge clock. The FRTC4111S slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address, and again after it has received the word address and each data byte.

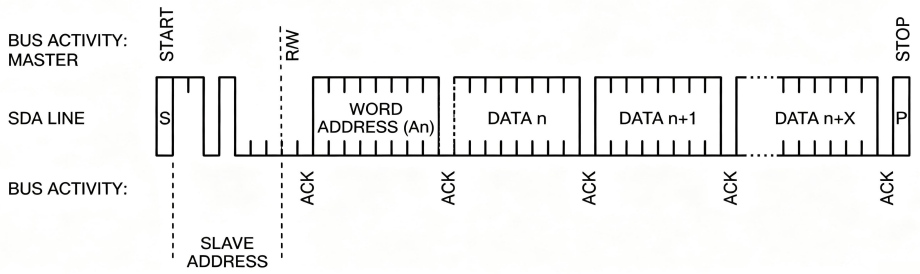


Figure9: Write mode sequence

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13 Register Configuration

Address	Data								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
00H	ST	10 seconds			Seconds				Seconds	00-59
01H	X	10 minutes			Minutes				Minutes	00-59
02H	CEB	CB	10 hours		Hours				Century/hours	0-1/00-23
03H	X	X	X	X	X	Day			Day	01-07
04H	X	X	10 dates		Date				Date	01-31
05H	X	X	X	10 M.	Month				Month	01-12
06H	10 years				Years				Year	00-99
07H	OUT	FT	S	Calibration					Control	
08H-3FH									RAM 56 x 8	00H-FFH

13.1 Seconds register(0x00)

D7(ST)	D6	D5	D4	D3	D2	D1	D0
ST= 1:oscillator stop ST=0:oscillator enable	10 seconds			Seconds			

13.2 Minutes register(0x01)

D7	D6	D5	D4	D3	D2	D1	D0
X	10 minutes			Minutes			

13.3 Century/hours register(0x02)

D7(CEB)	D6(CB)	D5	D4	D3	D2	D1	D0
CEB= 1:Century enable CEB=0:Century disable	Set Century enable(CEB= 1), CB will be toggled either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state)	10 hours		Hours			

13.4 Day register(0x03)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	Day		

13.5 Date register(0x04)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	10 dates		Date			

13.6 Month register(0x05)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	10M	Month			

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13.7 Year register(0x06)

D7	D6	D5	D4	D3	D2	D1	D0
10 years				Years			

13.8 Control register(0x07)

D7(OUT)	D6(FT)	D5	D4	D3	D2	D1	D0
Output driver pin When D6(FT)=0 OUT=0 FT/OUT pin outputs low OUT=1 FT/OUT pin outputs high	FREQUENCY TEST bit FT=0 Output 512Hz Disable FT=1 Output 512Hz Enable	Calibration offset value 111111=+126.108 ... 100010=+8.136 100001=+4.068 000000=0 000001=-2.034 000010=-4.068 ... 0 1 1111=-64.108					

13.9 RAM register(0x08-0x3F)

D7	D6	D5	D4	D3	D2	D1	D0
RAM 56 x 8							

Notes:

1. To guarantee oscillator startup after the initial power-up, set the ST bit to a '1,' then reset it to a '0.' This sequence activates a "kick start" circuit that assists oscillator startup under worst-case voltage and temperature conditions.

2. The seven clock registers may be read one byte at a time or as a sequential block. The control register (address location 7) can be accessed independently. Provisions have been made to ensure that a clock update does not occur while any of the seven clock addresses are being read. If a clock address is being read, an update of the clock registers will be delayed by 250 ms to allow the read to complete before the update takes place. This prevents data from transitioning during the read. This 250 ms delay affects only the clock register update and does not alter the actual clock time.

13.10 Preferred initial power-on defaults

Upon the initial application of power to the device, the FT bit will default to a '0' and the OUT bit will default to a '1'. All other register bits will power on in an arbitrary state. After the chip is powered on for the first time, all registers must be initialized.

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14 Clock Calibration

The FRTC4111S is driven by a quartz-controlled oscillator operating at a nominal frequency of 32,768 Hz. These devices are tested to exhibit no more than 35 ppm (parts per million) of oscillator frequency error at 25° C, which corresponds to roughly ±1.53 minutes per month. When the calibration bits are properly configured, the accuracy of each FRTC4111S improves to better than ±2 ppm at 25° C.

The oscillation rate of any crystal varies with temperature. Most clock chips attempt to compensate for crystal frequency and temperature drift using cumbersome trim capacitors. The FRTC4111S design, however, relies on periodic counter correction. The calibration circuit adds to or subtracts from the oscillator divider circuit at the divide-by-256 stage. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends on the value loaded into the five-bit calibration byte located in the control register. Adding counts speeds the clock up, while subtracting counts slows the clock down.

The calibration byte occupies the five lower order bits (D4-D0) in the control register (addr 7). This byte can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64-minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64- minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles—that is, +4.068 or -2.034 ppm of adjustment per calibration step in the calibration register. Assuming the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or -5.35 seconds per month, which corresponds to a total range of +5.5 or -2.75 minutes per month.

Two methods are available for determining how much calibration a given FRTC4111S may require. The first involves simply setting the clock, letting it run for a month, and comparing it to a known accurate reference (such as WWV broadcasts). While this may seem crude, it allows the designer to give the end user the ability to calibrate the clock as their environment may require, even after the final product is packaged in a non-user-serviceable enclosure.

All the designer has to do is provide a simple utility that accesses the calibration byte. The second approach is better suited to a manufacturing environment and involves the use of test equipment. When the frequency test (FT) bit, the seventh-most significant bit in the control register, is set to a '1', and the oscillator is running at 32,768 Hz, the FT/OUT pin of the device will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 ppm oscillator frequency error, requiring a -10 (XX001010) to be loaded into the calibration byte for correction. Note that setting or changing the calibration byte does not affect the frequency test output frequency.

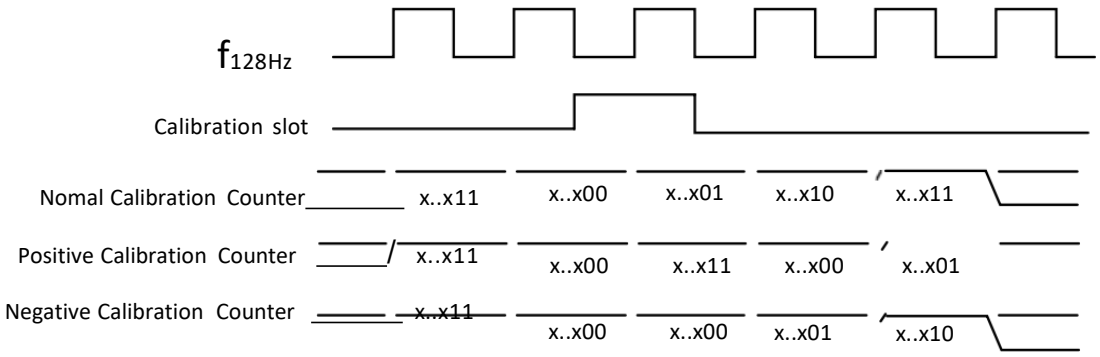
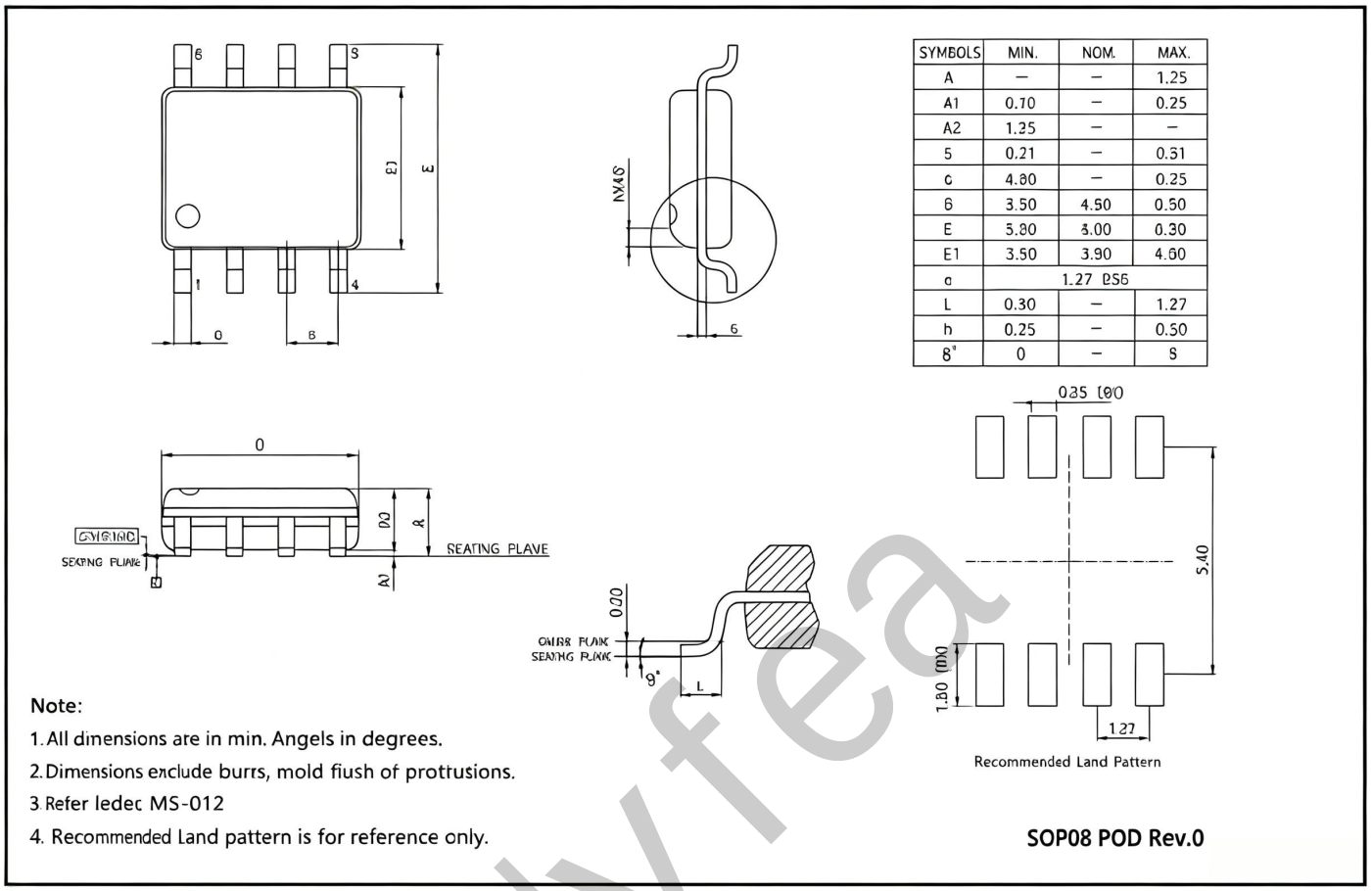


Figure10: Clock Calibration

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15 Package Information

FRTC4111S SOP-8 Package



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.25
A1	0.10	—	0.25
A2	1.25	—	—
b	0.21	—	0.31
c	4.80	—	0.25
θ	3.50	4.50	0.50
E	5.80	3.00	0.30
E1	3.50	3.90	4.60
e	1.27 BSC		
L	0.30	—	1.27
h	0.25	—	0.50
θ°	0	—	8

Note:

1. All dimensions are in min. Angels in degrees.
2. Dimensions exclude burrs, mold flush of protrusions.
3. Refer ledec MS-012
4. Recommended Land pattern is for reference only.

SOP08 POD Rev.0

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