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PRODUCT SPECIFICATION

Customer : _____

Product Name : Real Time Clock

Part NO : FRTC1337S

Issue Date : _____

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Prepared	Checked	Customer Check
ChenTT	Zelig	

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1 Features

- Using external 32.768kHz quartz crystal
- Supports I2C-Bus high speed mode (400 kHz)
- Includes time (Hour/Minute/Second) and calendar Year/Month/Date/Day) counter functions (BCD code)
- Programmable square wave output signal
- Two Time-of-Day Alarms
- Oscillator Stop Flag
- Operating range:1.8V to 5.5V

2 Description

The FRTC1337S is a serial real-time clock designed for low-power operation, integrating a full calendar and clock function. It features two programmable time-of-day alarms and a configurable square-wave output signal. Communication with the device is carried out over a two-wire bidirectional serial interface for data and address transfer.

The built-in clock/calendar system provides accurate tracking of seconds, minutes, hours, day, date, month, and year. The device automatically adjusts the date at month-end, accommodating months with fewer than 31 days, and includes leap-year compensation. The timekeeping format is selectable, supporting either 24-hour mode or 12-hour mode with an AM/PM indicator.

3 Applications

- Portable instruments
- Electronic metering
- Telecom equipments

4 Ordering Information

Ordering Code	Package	Description
FRTC1337S	SOP8	pitch 1.27mm

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5 Function Block

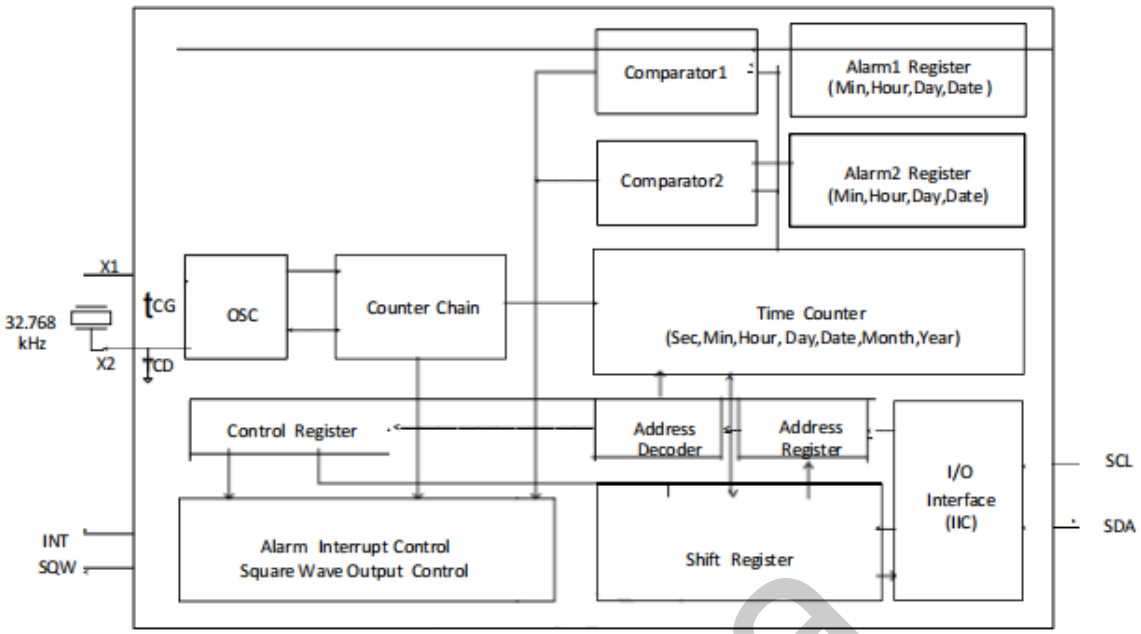

Figure1 Function Block

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6 Pin Configuration

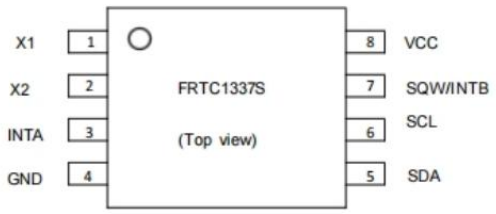

Figure2 Pin Configuration

Pin No	Pin	Type	Description
1	X1	I	**Oscillator Circuit Input.** Together with X2, 32.768kHz crystal is connected between them. Or external clock input.
2	X2	O	**Oscillator Circuit Output.** Together with X1, 32.768 kHz crystal is connected between them. When 32.768kHz external input, X2 must be float.
6	SCL	I	**Serial Clock Input.** SCL is used to synchronize data movement on the IIC serial interface.
5	SDA	I/O	**Serial Data Input/ Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor.
3	INTA	O	**Interrupt Output.** When enabled, INTA is asserted low when the time matches the values set in the alarm registers. This pin is an open-drain output and requires an external pull up resistor.
7	SQW/INTB	O	**Square-Wave/ Interrupt Output.** Programmable square-wave or interrupt output signal. It is an open-drain output and requires an external pull up resistor.
8	VCC	P	**Power.**
4	GND	P	**Ground.**

7 Typical Application Circuit

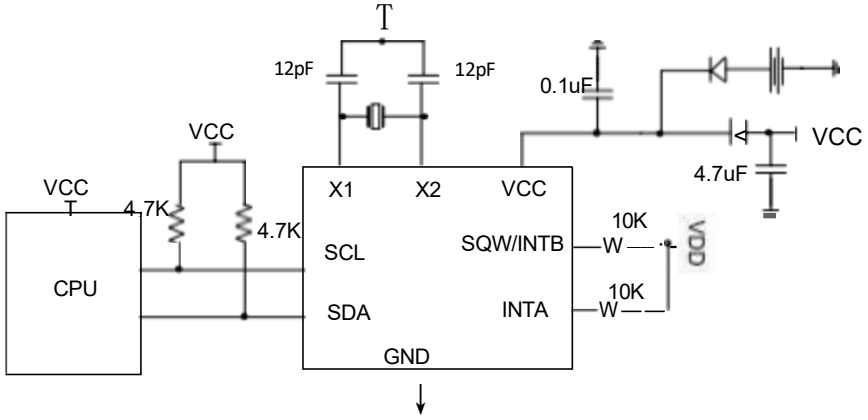

Figure3 Typical Application Circuit

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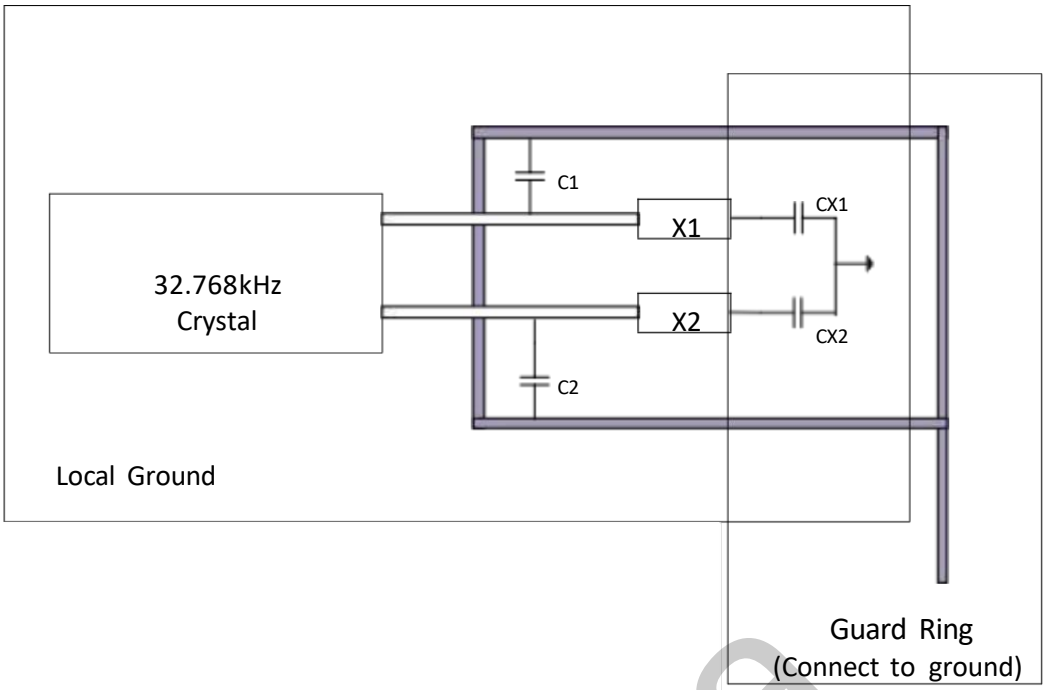
8 Recommended Layout for Crystal



Parameter	Symbol	MIN	TYP	MAX	Unit
Nominal Frequency	fo	_	32.768	_	kHz
Series Resistance	ESR	_	_	70	kΩ
Load Capacitance	C 1(Optional)	0	_	15	pF
Load Capacitance	C2(Optional)	0	_	15	pF
Build- in Cap	CX1 , CX2	_	12	_	pF

Note:
The crystal, traces and crystal input pins should be isolated from RF generating signals.

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9 Function Description

9.1 Clock function

The CPU is capable of both reading from and writing to the device, accessing timekeeping data such as the year (represented by the last two digits), month, date, day, hour, minute, and second. The device automatically recognizes leap years by applying the rule that any two-digit year evenly divisible by 4 is considered a leap year. This automatic adjustment remains valid through the year 2099, ceasing at 2100.

9.2 Alarm function

The device integrates two independent alarm systems, designated as Alarm 1 and Alarm 2. Each alarm can generate an interrupt output to the host CPU via either the INTA or INTB pin when the current time—including date, day of the week, hour, minute, or second—matches the preset alarm settings. The two alarms are capable of issuing interrupt signals independently at their respective programmed times. Furthermore, the alarm function for each channel can be configured to operate in either single-match mode or repeat-alarm mode, with both modes individually selectable for enabling or disabling as needed.

9.3 Programmable square wave output

A square wave output enable bit controls square wave output at pin 7. Frequencies are selectable: 1, 4.096k, 8.192k, 32.768k Hz.

9.4 Interface with CPU

Communication with the device is conducted through the I2C bus interface, which utilizes two signal lines: SCL serving as the serial clock input and SDA functioning as the bidirectional serial data line. Given that the SDA pin employs an open-drain output structure, an external pull-up resistor must be incorporated on the circuit board, particularly when the host CPU's I/O port also features an open-drain configuration. The serial clock line (SCL) supports a maximum operating frequency of 400 kHz, enabling compatibility with the I2C bus high-speed transmission mode.

9.5 Oscillator fail detect

When oscillator fail, FRTC1337S OSF bit will be set.

9.6 Oscillator enable/ disable

Oscillator and time count chain can be enabled or disabled at the same time by /ETIME bit.

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10 Registers

Addr. (hex)*1	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds (00-59)	0	S40	S20	S10	S8	S4	S2	S1
01	Minutes (00-59)	0	M40	M20	M10	M8	M4	M2	M1
02	Hours (00-23 / 01- 12)	0	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
03	Days of the week (D01- 07)	0	0	0	0	0	W4	W2	W1
04	Dates (01-31)	0	0	D20	D10	D8	D4	D2	D1
05	Months (01- 12)	Century	0	0	MO10	MO8	MO4	MO2	MO1
06	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
07	Alarm 1: Seconds	A1M1 *2	S40	S20	S10	S8	S4	S2	S1
08	Alarm 1: Minutes	A1M2 *2	M40	M20	M10	M8	M4	M2	M1
09	Alarm 1: Hours	A1M3 *2	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
0A	Alarm 1:Day,Date	A1M4 *2	Day, / Date	0, D20	0, D10	0, D8	W4 , D4	W2 , D2	W1 , D1
0B	Alarm 2: Minutes	A2M2 *3	M40	M20	M10	M8	M4	M2	M1
0C	Alarm 2: Hours	A2M3 *3	12, /24	H20 or P, /A	H10	H8	H4	H2	H1
0D	Alarm 2: Day, Date	A2M4*3	Day, / Date	0, D20	0, D10	0, D8	W4 , D4	W2 , D2	W1 , D1
0E	Control	/ETIME * 4	0	0	RS2*5	RS1 *5	INTCN*6	A2IE *7	A1IE*7
0F	Status	OSF*9	0	0	0	0	0	A2F*8	A1F*8

Note:

1. FRTC1337S uses 8 bits for address. For excess 0FH address, 1337S will not respond
2. (no acknowledge signal was given)
3. Alarm 1 mask bits. Select alarm repeated rate when an alarm occurs.
4. Alarm 2 mask bits. Select alarm repeated rate when an alarm occurs.
5. Oscillator and time count chain enable/disable bit.
6. Square wave output frequency select.
7. Interrupt output pin select bit.
8. Alarm 1 and alarm 2 enable bits.
9. Alarm 1 and alarm 2 flag bits.
10. Oscillator stop flag.
11. All bits marked with "0" are read-only bits. Their value when read is always "0".

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10.1 Control and status register

Addr (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
0E	Control	/ ETIME	0	0	RS2	RS1	INTCN	A2IE	A1IE
	(default)	0	0	0	1	1	0	0	0
0F	Status	OSF	0	0	0	0	0	A2F	A1F
	(default)	1	0	0	0	0	0	_	_

10.2 Oscillator related bits

ETIME

Enable oscillator and time count chain bit.

/ ETIME	Data	Description	
Read / Write	0	Enable oscillator and time count chain.	Default
	1	Disable oscillator and time count chain.	

Oscillator Stop Flag.

The Oscillator Stop Flag (OSF) bit, when set to logic 1, indicates that the oscillator has either stopped or experienced a stoppage at some point. This flag serves as a validity indicator for the clock and calendar data, allowing the system to assess whether the timekeeping information remains reliable. The OSF bit is automatically set to logic 1 whenever the oscillator ceases operation. Conditions that may trigger this flag include, but are not limited to:

1) Initial power application to the device.
2) Insufficient voltage on the VCC pin to sustain oscillation.
3) Disabling the oscillator via the /ETIME bit.
4) External disturbances affecting the crystal, such as electrical noise, leakage currents, or other environmental factors.

Once set, the OSF bit remains at logic 1 until explicitly cleared by writing a logic 0 to this bit..

10.3 Square wave frequency selection bits

RS2, RS1

Square wave Rate Select. These bits control the frequency of the square-wave output when the square wave has been enabled.

RS2, RS1	Data	SQW output freq. (Hz)	
Read / Write	00	1	
	01	4.096k	
	10	8. 192k	
	11	32.768k	Default

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10.4 Interrupt related bits

10.4.1 INTCN

The interrupt output pin select bit determines the routing relationship between the two alarm channels and the interrupt output pins. This bit configures how Alarm 1 and Alarm 2 are mapped to the available interrupt output pins.

INTCN	Data	Description	
Read / Write	1	A match between the timekeeping registers and the alarm 1 registers activates the INTA pin (if the alarm 1 is enabled) and a match between the timekeeping registers and the alarm 2 registers activates the SQW/INTB pin (if the alarm 2 is enabled).	
	0	A match between the timekeeping registers and either alarm 1 or alarm 2 registers activates the INTA pin (if the alarms are enabled) . In this configuration, a square wave is output on the SQW/ INTB pin.	Default

10.4.2 A1IE

Alarm 1 Interrupt Enable.

A1IE	Data	Description	
Read/ Write	0	The A1 F bit does not initiate the INTA signal.	Default
	1	Permits the alarm 1 flag (A1F) bit in the status register to assert INTA.	

10.4.3 A1F

Alarm 1 Flag.

A1F	Data	Description	
Read / Write	0	The time do not match the alarm 1 registers.	Default
Read	1	Indicates that the time matched the alarm 1 registers. If the A1 IE bit is also logic 1, the INTA pin goes low. A1F is cleared when written to logic 0. Attempting to write to logic 1 leaves the value unchanged.	

10.4.4 A2IE

Alarm 2 Interrupt Enable.

A2 IE	Data	Description	
Read / Write	0	The A2 F bit does not initiate an interrupt signal.	Default
	1	Permits the alarm 2 flag (A2F) bit in the status register to assert INTA (when INTCN = 0) or to assert SQW/INTB (when INTCN = 1) .	

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10.4.5 A2F

Alarm 2 Flag.

A1F	Data	Description	
Read / Write	0	The time do not match the alarm 2 registers.	Default
Read	1	Indicates that the time matched the alarm 1 registers. This flag can be used to generate an interrupt on either INTA or SQW/INTB depending on the status of the INTCN bit. If the INTCN = 0 and A2F = 1(and A2IE = 1), the INTA pin goes low. If the INTCN = 1 andA2F = 1 (and A2IE = 1), the SQW/ INTB pin goes low. A2F is cleared when written to logic 0. Attempting to write to logic 1 leaves the value unchanged.	

10.5 Time Counter

Time digit display (in BCD code):

The timekeeping registers follow standard sequential counting and carry operations. The seconds register counts from 00 to 59; upon incrementing from 59 to 00, a carry is generated and propagated to the minutes register. Similarly, the minutes register operates within the range of 00 to 59, producing a carry to the hours register when it transitions from 59 to 00. The hours register's behavior is dependent on the /12_24 bit configuration; it increments according to the selected time format and generates a carry to both the day register and the day-of-the-week register when rolling over from 11 PM to 12 AM (in 12-hour mode) or from 23 to 00 (in 24-hour mode).

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
00	Seconds	0	S40	S20	S10	S8	S4	S2	S1
	(default)	0	_	_	_	_	_	_	_
01	Minutes	0	M40	M20	M10	M8	M4	M2	M1
	(default)	0	_	_	_	_	_	_	_
02	Hours	0	12, /24	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	0	_	_	_	_	_	_	_

Note:

Any registered imaginary time should be replaced with correct time, otherwise it will cause the clock counter malfunction.

10.6 12, /24 bit

This bit is used to select between 12-hour clock system and 24-hour clock system.

12, /24	Data	Description
Read / Write	0	24-hour mode
	1	12-hour mode

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12, /24	Description	Hours register			
		24-hour clock	12-hour clock	24-hour clock	12-hour clock
0	24-hour time display	00	52 (AM 12)	12	72 (PM 12)
		01	41 (AM 01)	13	61 (PM 01)
		02	42 (AM 02)	14	62 (PM 02)
		03	43 (AM 03)	15	63 (PM 03)
		04	44 (AM 04)	16	64 (PM 04)
		05	45 (AM 05)	17	65 (PM 05)
1	12-hour time display	06	46 (AM 06)	18	66 (PM 06)
		07	47 (AM 07)	19	67 (PM 07)
		08	48 (AM 08)	20	68 (PM 08)
		09	49 (AM 09)	21	69 (PM 09)
		10	50 (AM 10)	22	70 (PM 10)
		11	51 (AM 11)	23	71 (PM 11)

Note:

This bit is provided to select the desired timekeeping format, allowing the user to choose between 12-hour and 24-hour clock operation. It is essential that this selection be made prior to writing any time data into the device registers, as the hour register's counting behavior and interpretation depend on the selected format.

10.7 Days of the week Counter

The day-of-week counter operates as a divide-by-7 counter, cycling sequentially from 01 through 07 and then wrapping back to 01. The numeric values assigned to specific days are user-defined; however, they must follow a sequential order. For example, if 01 represents Sunday, then 02 must represent Monday, 03 for Tuesday, and so forth. Any illogical or non-sequential time and date entries may lead to undefined or erroneous operation of the device.

Addr (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
03	Days of the week	0	0	0	0	0	W4	W2	W1
	(default)	0	0	0	0	0	-	-	-

10.8 Calendar Counter

All time and date data is stored in BCD (Binary-Coded Decimal) format. The date register follows month-specific range limits, with automatic carry-over to the month field upon rollover:

Day digits: Ranges from 1 to 31 for months with 31 days (January, March, May, July, August, October, and December); 1 to 30 for months with 30 days (April, June, September, and November); 1 to 29 for February in leap years; and 1 to 28 for February in ordinary (non-leap) years. The day counter cycles back to 1 after reaching its maximum, generating a carry to the month register.

Month digits: Ranges from 1 to 12. Upon rolling over from 12 to 1, a carry is propagated to the year register.

Year digits: Ranges from 00 to 99. Leap-year recognition applies to years 00, 04, 08, and so on up to 96 (i.e., any two-digit year divisible by 4).

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Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
04	Dates	0	0	D20	D10	D8	D4	D2	D1
	(default)	0	0	-	-	-	-	-	-
05	Months	Century* 1	0	0	M10	M8	M4	M2	M1
	(default)	-	0	0	-	-	-	-	-
06	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	(default)	-	-	-	-	-	-	-	-

Note:
The century bit is toggled when the years register overflows from 99 to 00

10.9 Alarm Register

Addr	Description	D7	D6	D5	D4	D3	D2	D1	D0
07	Alarm 1: Seconds	A1M1* 1	S40	S20	S10	S8	S4	S2	S1
	(default)	_	_	_	_	_	_	_	_
08	Alarm 1: Minutes	A1M2* 1	M40	M20	M10	M8	M4	M2	M1
	(default)	_	_	_	_	_	_	_	_
09	Alarm 1: Hours	A1M3* 1	12 , /24	H20 or P/A	H10	H8	H4	H2	H1
	(default)	_	_	_	_	_	_	_	_
0A	Alarm 1: Day, Date	A1M4* 1	Day , * 1 / Date	0 , D20	0 , D10	0 , D8	W4 , D4	W2 , D2	W1 , D1
	(default)	_	_	_	_	_	_	_	_
0B	Alarm 2: Minutes	A2M2 *2	M40	M20	M10	M8	M4	M2	M1
	(default)	_	_	_	_	_	_	_	_
0C	Alarm 2: Hours	A2M3 *2	12, /24	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	_	_	_	_	_	_	_	_
0D	Alarm 2: Day, Date	A2M4 *2	Day, / Date*2	0, D20	0, D10	0, D8	W4 , D4	W2 , D2	W1 , D1
	(default)	_	_	_	_	_	_	_	_

Note:
1 、Alarm mask bit, using to select Alarm 1 alarm rate.
2 、Alarm mask bit, using to select Alarm 2 alarm rate.

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10.10 Alarm Function

Addr. (hex)	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds	0	S40	S20	S10	S8	S4	S2	S1
01	Minutes	0	M40	M20	M10	M8	M4	M2	M1
02	Hours	0	12, /24	H20 or A, /P	H10	H8	H4	H2	H1
03	Days of the week	0	0	0	0	0	W4	W2	W1
04	Dates	0	0	D20	D10	D8	D4	D2	D1
07	Alarm 1: Seconds	A1M1	S40	S20	S10	S8	S4	S2	S1
08	Alarm 1: Minutes	A1M2	M40	M20	M10	M8	M4	M2	M1
09	Alarm 1 Hours	A1M3	12, /24	H20 or A, /P	H10	H8	H4	H2	H1
0A	Alarm 1: Day, Date	A1M4	Day, / Date	0, D20	0, D10	0, D8	W4 , D4	W2 , D2	W1 , D1
0B	Alarm 2: Minutes	A2M2	M40	M20	M10	M8	M4	M2	M1
0C	Alarm 2: Hours	A2M3	12, /24	H20 or A, /P	H10	H8	H4	H2	H1
0D	Alarm 2: Day,Date	A2M4	Day, / Date	0, D20	0, D10	0, D8	W4 , D4	W2 , D2	W1 , D1
0E	Control	/ ETIME	0	0	RS2	RS1	INTCN	A2IE	A1IE
0F	Status	OSF	0	0	0	0	0	A2F	A1F

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Note:

The alarm function does not support mixed hour-format operation; that is, the timekeeping registers and the alarm registers must operate under the same hour system (either both in 12-hour mode or both in 24-hour mode).

The FRTC1337S is equipped with two time-of-day/date alarms. Through the INTCN bit in the control register, these alarms can be configured to operate in two distinct output modes: each alarm can drive its own separate interrupt output pin, or both alarms can be combined to drive a common interrupt output. Bit 7 of each alarm register serves as a mask bit for that channel.

When all mask bits for a given alarm are set to logic 0, the alarm will trigger only when the values in the timekeeping registers (addresses 00h through 04h) exactly match the values stored in the corresponding alarm registers. Alternatively, the alarms can be programmed for repetitive operation, generating interrupts at intervals such as every second, minute, hour, day, or date. The possible configurations are summarized in Table 2 and Table 3

Bit 6 of each alarm day/date register, designated as the Day/Date select bit, determines whether the alarm value stored in bits 0 through 5 of that register corresponds to the day of the week or the date of the month. When this bit is set to logic 0, the alarm condition is evaluated against the date of the month. When set to logic 1, the alarm condition is evaluated against the day of the week.

When the values in the FRTC1337S timekeeping registers match the programmed alarm register settings, the corresponding alarm flag bit (A1F for Alarm 1 or A2F for Alarm 2) is set to logic 1. If the associated alarm interrupt enable bit (A1IE or A2IE) is also set to logic 1, the alarm condition will assert one of the interrupt output signals (INTA or SQW/INTB). The match detection is performed during the once-per-second update cycle of the time and date registers.

10.10.1 Alarm 1 Mask Bits

Day, /Date	Alarm 1 register mask bits				Alarm rate
	A1M4	A1M3	A1M2	A1M1	
■	1	1	1	1	Alarm once per second
■	1	1	1	0	Alarm when seconds match
×	1	1	0	0	Alarm when minutes and seconds match
×	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match
Others					Ignored.

10.10.2 Alarm 2 Mask Bits

Day, /Date	Alarm 2 register mask bits			Alarm rate
	A2M4	A2M3	A2M2	
■	1	1	1	Alarm once per minute (00 seconds of every minute)
■	1	1	0	Alarm when minutes match
■	1	0	0	Alarm when hours, minutes
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match
Others				Ignored.

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11 I2C Bus Interface

This two-wire serial bus is designed for communication between multiple integrated circuits. It comprises two signal lines: SDA (Serial Data), which is bidirectional for data transmission, and SCL (Serial Clock), which carries the clock signal. Both lines require external pull-up resistors to ensure proper logic levels.

The bus protocol adheres to the following fundamental rules:

1) A data transfer can be initiated only when the bus is in the idle (not busy) state.
2) During data transfer, the SDA line must remain stable while the SCL line is at a logic high level.
3) Any change in the SDA state while SCL is high is interpreted as a control signal (START or STOP condition).

Based on these rules, the following bus conditions are defined for proper operation:

11.1 Bus not busy

Both data and clock lines remain high.

11.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

11.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

11.4 Data valid

Following a START condition, data on the SDA line is considered valid when it remains stable throughout the high period of the SCL clock signal. The data state may be changed only while the clock signal is low. Each data bit corresponds to one clock pulse.

Every data transfer is initiated by a START condition and terminated by a STOP condition. The number of data bytes that can be transmitted between START and STOP is unlimited. Data is transferred in byte-wide format, with the most significant bit sent first. Each receiving device is required to acknowledge every byte by generating a ninth-bit acknowledgement (ACK) during the clock cycle following the data byte.

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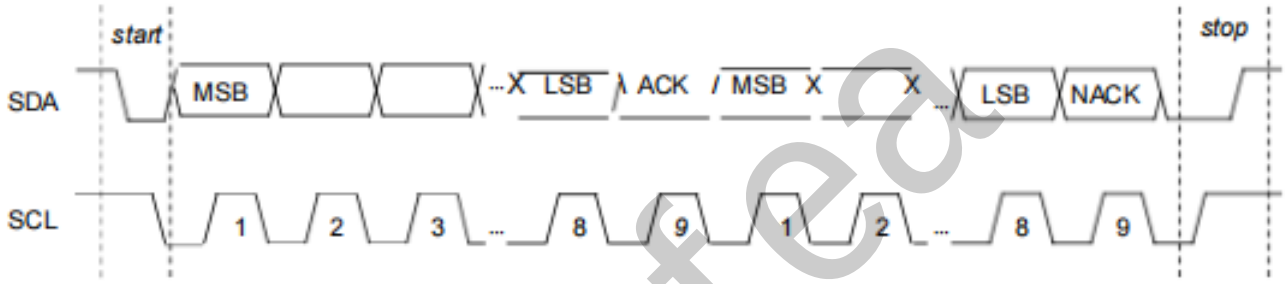
11.5 Acknowledge

Every 8-bit data byte transmitted on the bus is followed by one acknowledge bit. This acknowledge bit is a logic-low level driven onto the SDA line by the receiver, while the master generates the corresponding clock pulse for this acknowledge cycle.

An addressed slave receiver is required to produce an acknowledge after each byte it receives. Likewise, when the master operates as a receiver, it must generate an acknowledge after each byte clocked out from a slave transmitter.

The acknowledging device must pull the SDA line low during the acknowledge clock pulse, ensuring that SDA remains stable at a low level throughout the high period of that clock cycle. Proper setup and hold times must be observed for reliable operation.

To signal the end of a data transfer, the master receiver must withhold the acknowledge (i.e., not generate an ACK) after the last byte clocked out from the slave transmitter. In this case, the slave transmitter must release the SDA line (leave it high) so that the master can then issue a STOP condition to terminate the transaction.



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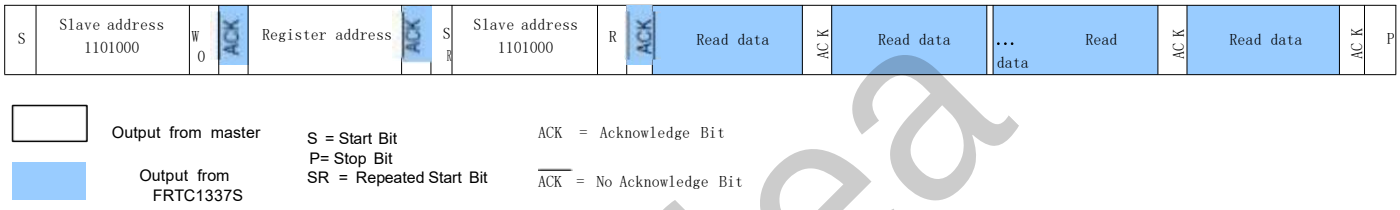
11.6 Read mode

In this read mode, the master first configures the slave address and the internal address pointer of the FRTC1337S. This is accomplished by sending the slave address with the write control bit (R/W = 0), followed by the word address (An) which is written into the on-chip address pointer, and then receiving an acknowledge bit from the slave.

Next, the master repeats the START condition and resends the slave address, this time with the read control bit (R/W = 1). At this point, the master transmitter transitions into the master receiver role. The slave transmitter then places the data byte at the addressed location (An) onto the bus, and the master receiver responds with an acknowledge bit.

The address pointer is incremented automatically only upon the successful reception of an acknowledge bit. The slave transmitter then outputs the data byte at address An + 1, the master receiver acknowledges it, and the pointer advances to An + 2.

This sequential read cycle continues—each new byte being acknowledged by the master—until the master receiver sends a STOP condition to terminate the transfer.

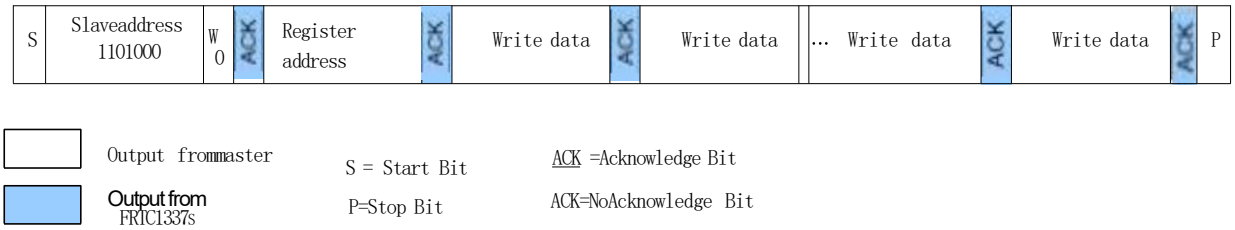


11.7 Write mode

In this mode, the master transmitter sends data to the FRTC1337S operating as a slave receiver. After the START condition and the slave address are transmitted, a logic 0 (R/W = 0) is placed on the bus to indicate to the addressed device that a word address (An) will follow and is to be written into the internal address pointer.

Following the successful write of the word address, the data byte to be written is clocked in next. Upon reception of an acknowledge clock from the slave, the internal address pointer is automatically incremented to point to the next memory location within the device's register space.

The FRTC1337S slave receiver generates an acknowledge clock signal after each of the following events: after receiving the slave address, after receiving the word address, and after each data byte it receives from the master transmitter.



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12 Maximum Ratings

Storage Temperature	-65 ℃ to +150 ℃
Ambient Temperature with Power Applied	-40℃ to +125 ℃
Supply Voltage to Ground Potential (Vcc to GND)	- 0.3V to 6.5V
DC Input (All Other Inputs except Vcc & GND)	- 0.3V to VCC + 0.3V
DC Output Voltage (SDA, /INT pins)	-0.3V to +6.5V
Power Dissipation	320mW (Depend on package)

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

13 Recommended Operating Condition

Part No.	Symbol	Description		MIN	P	MAX	Unit
FRTC1337S	VCC	Po er vol a e		1.	-	5.5	V
	VO C	Oscillator voltage		1.7	-	5.5	
	VIH	Input high level	CL, SDA	0.7VCC	-	VCC+0.3	
			NTA, SQW/ INTB	_	-	5.5	
	VI	Input low level		-0.3	-	0.3VCC	
	TA	Operating temperature		-40	-	85	° C

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14 DC Electrical Characteristics

Unless otherwise specified, VCC = 1.8~5.5V, TA = -40 ° C to +85 ° C

Sym.	Item	PIN	Condition	MIN	TYP	MAX	Unit
VCC	Supply voltage	VCC		1.8	_	5.5	V
VOSC	Oscillator voltage	VCC		1.7	_	5.5	V
ICC	Active supply current	VCC	Note 1, 5	_	_	150	μA
	Standby current	VCC	Note 2, 3, 5	_	0.5	0.8	
	Timekeeping current	VCC	Note 2, 4, 5	_	350	600	nA
	Data retention current	VCC	Note 2, 6	_	_	150	
VIL1	Low- level input voltage	SCL		-0.3	_	0.3VCC	V
VIH1	High- level input voltage	SCL		0.7VCC	_	VCC+0.3	
IOL	Low- level output current	SDA, /INTA, /INTB	VOL = 0.4V	-	_	3	mA
IIL	Input leakage current	SCL		-	_	1	μA
IOZ	Output current when OFF	SDA, INTA, INTB		-	_	1	μA

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Note:

The following conditions apply to the electrical specifications:

1. SCL clock operates at a maximum frequency of 400 kHz, with VIL set to 0.0V and VIH set to VCC.
2. Parameters are specified while the 2-wire bus is inactive, under the same input voltage levels (VIL = 0.0V, VIH = VCC).
3. The square-wave output (SQW) function is enabled during measurement.
4. For specifications requiring the SQW function disabled, the INTCN bit is set to logic 1.
5. Measurements are performed using the recommended crystal connected across the X1 and X2 pins.
6. The crystal oscillator is disabled for relevant test conditions.

15 AC Electrical Characteristics

Sym	Description	Value	Unit
VHM	Rising and falling threshold voltage high	0.8 VCC	V
VHL	Rising and falling threshold voltage low	0.2 VCC	V



16 I2C AC Characteristics

Symbol	Item	MIN	TYP	MAX	Unit
fSCL	SCL clock frequency			400	kHz
tSU; STA	START condition set- up time	0.6			us
tHD; STA	START condition hold time	0.6			us
tSU; DAT	Data set-up time (RTC read/write)	200			ns
tHD;DAT1	Data hold time (RTC write)	35			ns
tHD;DAT2	Data hold time (RTC read)	0			us
tSU; STO	STOP condition setup time	0.6			us
tBUF	Bus idle time between a START and STOP condition	1.3			us
tLOW	When SCL = ″L″	1.3			us
tHIGH	When SCL = ″H″	0.6			us
tr	Rise time for SCL and SDA			0.3	us
tf	Fall time for SCL and SDA			0.3	us
tSP *	Allowable spike time on bus			50	ns
CB	Capacitance load for each bus line			400	pF

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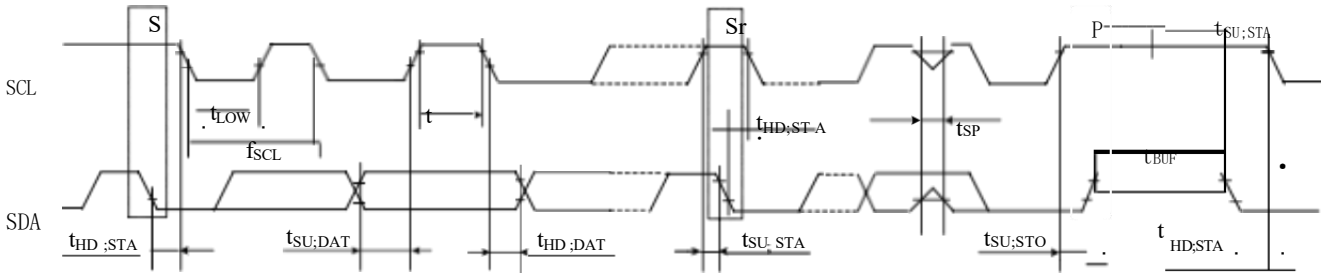

S: condition P: Stop condition SR: Restart condition

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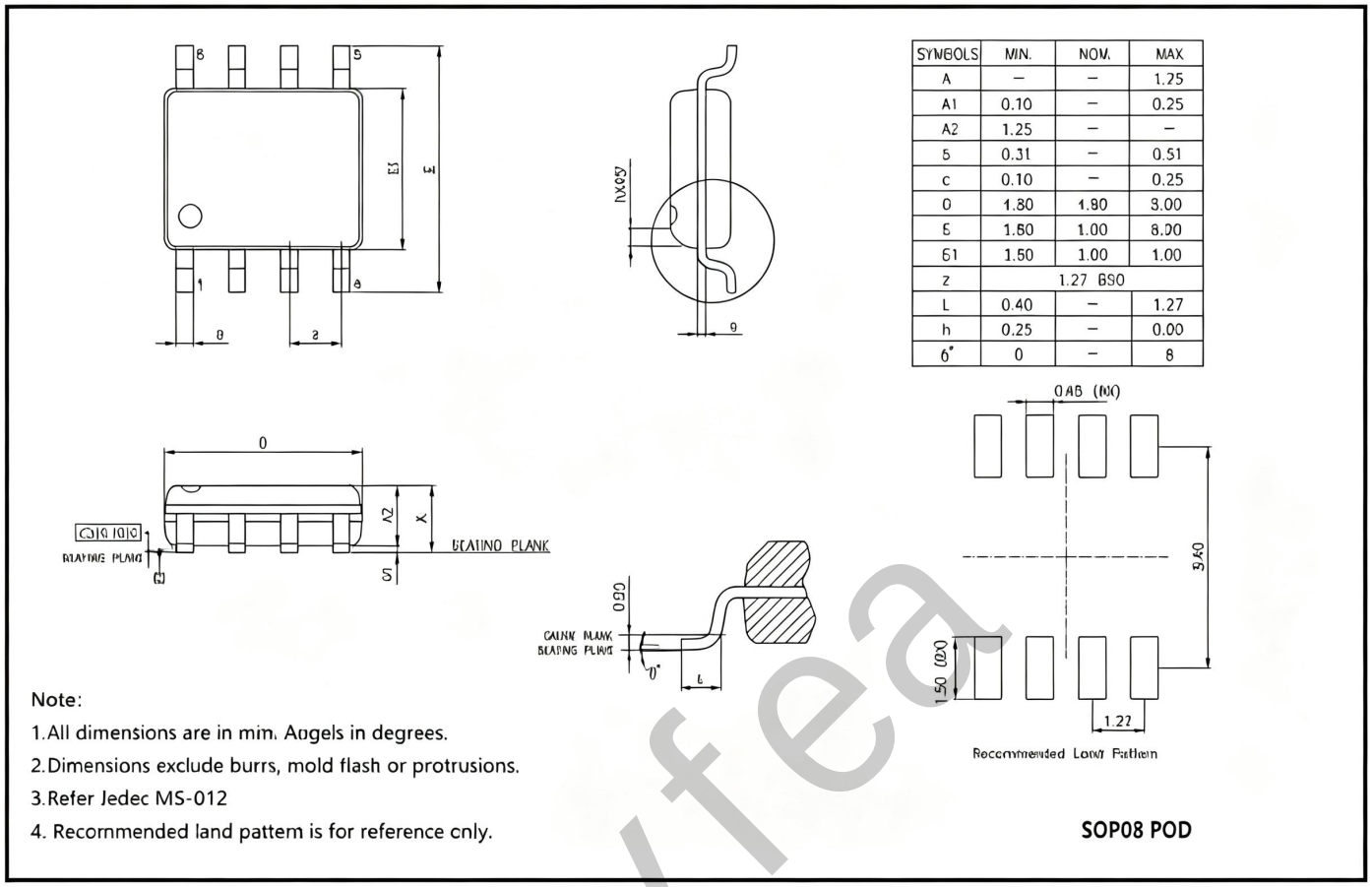
17 Package Information

FRTC1337S SOP8 Package



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