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PRODUCT SPECIFICATION

Customer: _____

Product Name: Real Time Clock

Part NO: FRTC1339M

Issue Date: _____

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Prepared	Checked	Customer Check
ChenTT	Zelig	

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1 Features

- Real-time clock (RTC) counts seconds, minutes, hours, day, date, month, and year
- with leap-year compensation valid up to 2100
- 2-wire serial interface
- Two time-of-day alarms
- Programmable square-wave output
- Oscillatorstop flag
- Automatic power-fail detect and switch circuitry
- Trickle charge capability
- Operating Temperature: -40 ~ 125° C

2 Applications

- Handhelds (GPS, POS Terminal)
- Consumer Electronics (Set-Top Box, Digital Recording, Network Appliance)
- Office Equipment (Fax/Printer, Copier)
- Medical (Glucometer, Medicine Dispenser)
- Telecommunications (Router, Switcher, Server)

3 Description

The FRTC1339M is a low-power serial real-time clock/date device featuring two programmable time-of-day alarms and a configurable square-wave output. Communication with the device is carried out via a 2-wire bidirectional serial bus for address and data transfer.

The clock/date subsystem provides comprehensive timekeeping data, including seconds, minutes, hours, day, date, month, and year. The date is automatically adjusted at month-end to accommodate months with fewer than 31 days, with full leap-year correction applied as necessary. The time format is user-selectable, supporting either 24-hour mode or 12-hour mode with an AM/PM indicator.

Additionally, the FRTC1339M incorporates a built-in power-sense circuit that continuously monitors the primary supply voltage and automatically switches to backup power upon detection of a power failure.

4 Ordering Information

Ordering Code	Package	Package Description
FRTC1339M	MSOP-8	Pitch 0.65mm

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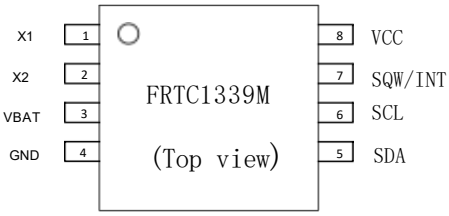
5 Pin Configurations



MSOP8(Top view)

Pin Name	Pin No.	Description
X1	1	32 . 768 kHz Crystal Connection
X2	2	
V_{BACKUP}	3	Secondary Power Supply
GND	4	Ground
SDA	5	Serial Data.
SCL	6	Serial Clock.
SQW	7	Square-Wave/ Interrupt Output ,Open drain
V_{CC}	8	Power Supply

6 Marking information

Marking	Information
FRTC	Part number:FRTC
1339M	1339M
YYWW	date code

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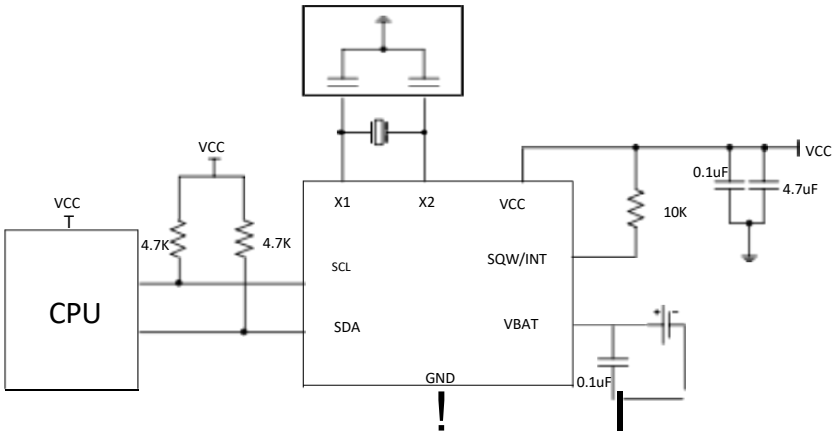
7 Product Features

7.1 Typical Application Circuit



Notes:

1. It is recommended to add 0.1uf capacitor to VBAT pin.
2. If the time accuracy requirement is high, please reserve the crystal matching capacitor.

7.2 Maximum Ratings

Symbol	Parameter	Min	TYP	Max	Unit
T_{store}	Storage Temperature	-55	_	+125	° C
T_{op}	Operating Temperature Range	-40	_	+85	° C
V_{IN}	Voltage Range on Any Pin Relative to Ground	-0.3	_	6	V

Note:

Maximum ratings listed in this specification represent stress limits beyond which permanent damage to the device may occur. These values are intended as stress ratings only, and the device is not guaranteed to function under these or any other conditions exceeding those specified in the operational sections of this document. Prolonged exposure to absolute maximum rating conditions may adversely affect device reliability and long-term performance.

7.3 Recommended Operation Conditions

(TA = -40 ° C to +85 ° C)

Symbol	Parameter	Conditions	Min	TYP	Max	Unit
V_{CC}	Supply Voltage	FRTC1339M	2.97	3.3	5.5	V
V_{IH}	SCL/SDA pins		0.7 x V_{CC}	_	V_{CC} + 0.5	V
V_{IL}	SCL/SDA pins		-0.5	-	+0 .3 x VCC	V
V_{PF}	Power-Fail Voltage	FRTC1339M	2.70	2.85	2.97	V
V_{BACKUP}	Backup supply Voltage		1.4	3.0	3.7	V

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7.4 DC Electrical Characteristics

Unless otherwise specified, -40 ° C≤T_A≤ 85 ° C , ($V_{CC(MIN)}$ ≤V_{CC}≤ $V_{CC(MAX)}$)

Symbol	Parameter	Test Conditions*1	MIN	TYP	MAX	Unit
I_{LI}	Input Leakage	SCL only	_	_	1	μA
I_{LO}	I/O Leakage	SDA and SQW/INT		_	1	μA
I_{OL}	Logic 0 Out: SDA and SQW/INT	V_{OL} = 0.4V, V_{CC} > 2.0V	3	_		mA
	Logic 0 Out: SDA and SQW/INT	V_{OL} = 0.2 (V_{CC}), V_{CC} ≤2.0V	3	_		mA
	Logic 0 Out: SDA and SQW/INT	V_{OL} = 0.2 (V_{CC}) 1.3V < V_{CC} < 1.8V	250	_		μA
I_{CCA}	V_{CC} Active Current*2		_	_	450	μA
I_{CCS}	V_{CC} Standby Current*3		_	80	150	μA
R1	Trickle Charge Resistor Register	10h = A5h, V_{CC} = Typ, V_{BACKUP} = 0V		250		Ω
R2	Trickle Charge Resistor Register	10h = A6h, V_{CC} = Typ, V_{BACKUP} = 0V		2000		Ω
R3	Trickle Charge Resistor Register	10h = A7h, V_{CC} = Typ, V_{BACKUP} = 0V		4000		Ω
I_{BKLKG}	V_{BACKUP} Leakage Current			25	100	nA
I_{BKOSC}	V_{BACKUP} Current*4	V_{CC} = 0V, EOSC = 0, SQW Off		400	700	nA
I_{BKSQW}	V_{BACKUP} Current*4	V_{CC} = 0V, EOSC = 0, SQW On		600	1000	nA
I_{BKDR}	V_{BACKUP} Current*4	V_{CC} = 0V, EOSC = 1		10	100	nA

Note:
1. Limits at -40° C are guaranteed by design and not production tested.
2. I_{CCA} : SCL at f_{SC} max, V_{IL} = 0.0V, V_{IH} = V_{CC}, trickle charge disabled.
3. Specified with 2-wire bus inactive, V_{IL} = 0.0V, V_{IH} = V_{CC}, trickle charge disabled.
4. Using recommended crystal on X1 and X2.

7.5 Crystal Specifications*1

Symbol	Parameter	MIN	TYP	MAX	Units
f_O	Nominal Frequency		32.768		kHZ
ESR	Series Resistance			70	kΩ
C_L	Load Capacitance		6		pF

Note:
1. The crystal, traces, and crystal input pins should be isolated from RF generating signals.

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7.6 AC Electrical characteristics

(T_A = -40° C to +85° C) *1 V_{CC} = MIN to MAX

Symbol	Parameter	Test Conditions*1	MIN	TYP	MAX	Unit
f_{SCL}	SCL Clock Frequency	Fast mode	100		400	kHz
		Standard mode			100	kHz
t_{BUF}	Bus Free Time Between STOP and START Condition	Fast mode	1.3			μs
		Standard mode	4.7			
$t_{HD:STA}$	Hold Time (Repeated) START Condition*2	Fast mode	0.6			μs
		Standard mode	4.0			
t_{LOW}	LOW Period of SCL Clock	Fast mode	1.3			μs
		Standard mode	4.7			
t_{HIGH}	HIGH Period of SCL Clock	Fast mode	0.6			μs
		Standard mode	4.0			
$t_{SU:STA}$	Setup Time for Repeated START Condition	Fast mode	0.6			μs
		Standard mode	4.7			
$t_{HD:DAT}$	Data Hold Time*3/4	Fast mode	0		0.9	μs
		Standard mode	0			
$t_{SU:DAT}$	Data Setup Time*5	Fast mode	100			ns
		Standard mode	250			
t_R	Rise Time of Both SDA and SCL Signals *6	Fast mode	20 + 0.1C_B		300	ns
		Standard mode	20 + 0.1C_B		1000	
t_F	Fall Time of Both SDA and SCL Signals *6	Fast mode	20 + 0.1C_B		300	ns
		Standard mode	20 + 0.1C_B		300	
$t_{SU:STO}$	Setup Time for STOP Condition	Fast mode	0.6			μs
		Standard mode	4.0			
C_B	Capacitive Load for Each Bus Line*6				400	pF
$C_{I/O}$	I/O Capacitance (SDA, SCL) *7			10		pF
t_{OSF}	Oscillator Stop Flag (OSF) Delay*8			100		ms

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Note:

1. Specifications at -40° C are guaranteed by design and are not subject to production testing.
2. The first clock pulse is generated after the specified period has elapsed.
3. The device must internally provide a minimum hold time of 300 ns for the SDA signal, referenced to the VIHMIN of the SCL signal, in order to bridge the undefined region during the falling edge of SCL.
4. The maximum tHD:DAT specification only needs to be satisfied when the device does not stretch the low period (tLOW) of the SCL signal.
5. A fast-mode device may be used in a standard-mode system, provided that the tSU:DAT requirement of ⩾ 250 ns is met. This condition is automatically satisfied if the device does not stretch the SCL low period. If SCL stretching is employed, the next data bit must be output to the SDA line at least tR MAX + tSU:DAT = 1000 + 250 = 1250 ns before the SCL line is released.
6. CB represents the total capacitance of one bus line, measured in picofarads (pF).
7. Any specifications noted as "guaranteed by design" are verified through characterization and are not covered by production testing.
8. The parameter tOSF defines the minimum oscillator stop duration required to set the OSF flag, under the condition that VCC is within the range of VCC MINV to VCC MAX and VBAT is between 1.4V and 3.7V.

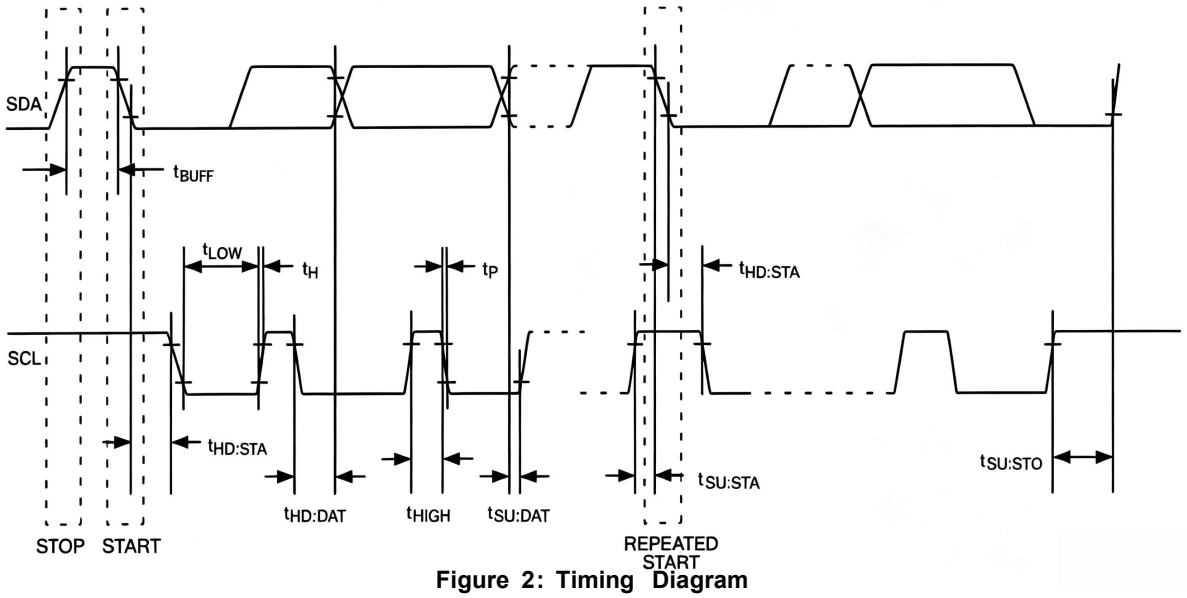

Figure 2: Timing Diagram

7.7 Power-Up/Power-Down Characteristics

(TA = -40° C to +85° C) *1

Symbol	Parameter	Test Conditions*1	MIN	TYP	MAX	Unit
t_{REC}	Recovery at Power-Up*2				2	ms
t_{VCCF}	V_{CC} Fall Time	$V_{PF(MAX)}$ to $V_{PF(MIN)}$	300			μs
t_{VCCR}	V_{CC} Rise Tim	$V_{PF(MIN)}$ to $V_{PF(MAX)}$	0			μs

Note:
1. Limits at -40° C are guaranteed by design and not production tested.
2. This delay applies only if the oscillator is enabled and running. If the oscillator is disabled or stopped, no power-up delay occurs.

Test Circuits

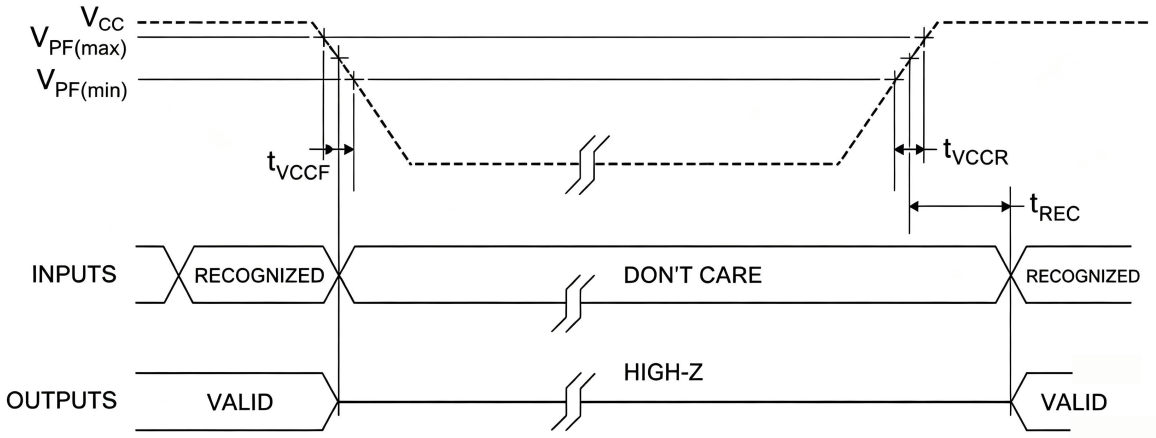

Figure 3: Power-Up/Power-Down Timing

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8 Functional Description

The FRTC1339M is a low-power serial real-time clock/date device featuring two programmable time-of-day alarms and a configurable square-wave output. Communication with the device is carried out via a 2-wire bidirectional serial bus for address and data transfer.

The clock/date subsystem provides comprehensive timekeeping data, including seconds, minutes, hours, day, date, month, and year. The date is automatically adjusted at month-end to accommodate months with fewer than 31 days, with full leap-year correction applied as necessary. The time format is user-selectable, supporting either 24-hour mode or 12-hour mode with an AM/PM indicator.

Additionally, the FRTC1339M incorporates a built-in power-sense circuit that continuously monitors the primary supply voltage and automatically switches to backup power upon detection of a power failure.

8.1 Application Information

The FRTC1339M functions as a slave device on the serial bus. Bus access is initiated by issuing a START condition, followed by the device identification code and the appropriate data. Once access is established, subsequent registers may be accessed sequentially until a STOP condition is issued.

The device is fully accessible for both read and write operations when VCC is above the power-fail threshold (VPF). However, when VCC drops below VPF, the internal clock registers are blocked from any access. The power-switching logic operates as follows: if VPF is lower than VBACKUP, the device switches from VCC to VBACKUP when VCC falls below VPF. Conversely, if VPF is higher than VBACKUP, the switch occurs when VCC drops below VBACKUP. The registers are maintained from the VBACKUP supply until VCC is restored to normal operating levels. A block diagram illustrating the main functional elements of the serial real-time clock is provided in Figure: Block Diagram.

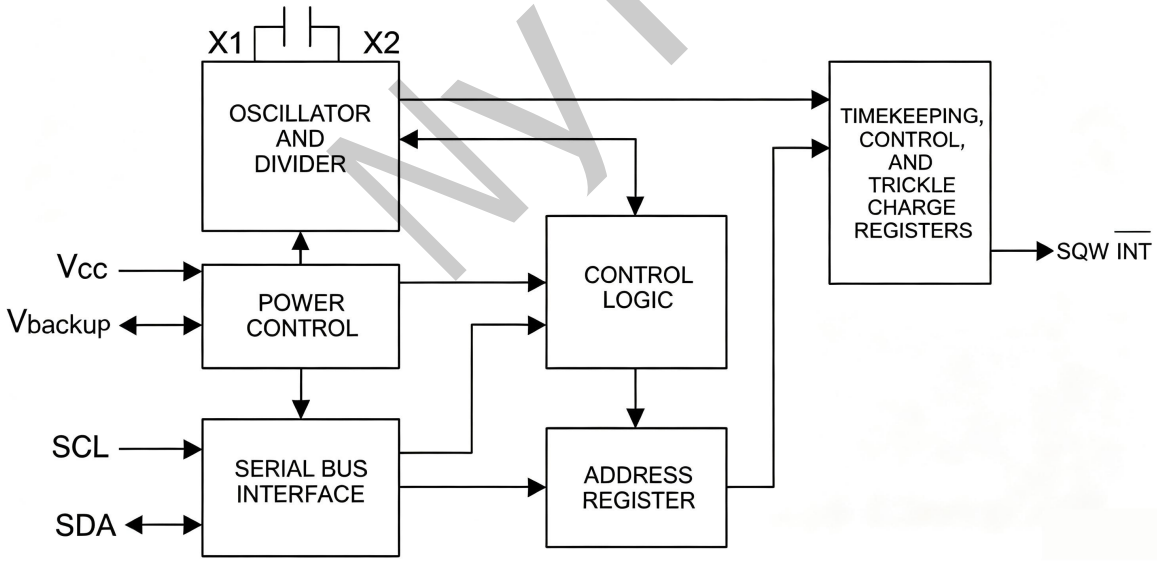

Figure 4: Block Diagram

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8.2 Signal Descriptions

V_{CC}, GND - DC power is provided to the device on these pins.
SCL (Serial Clock Input) - SCL is used to synchronize data movement on the serial interface.

SDA (Serial Data Input/Output) - SDA is the input/output pin for the 2-wire serial interface. The SDA pin is an open- drain output and requires an external pullup resistor.

V_{BACKUP} (Secondary Supply Input) - Connection for a secondary power supply. Supply voltage must be held between 1.4V and 3.7V for proper operation. This pin can be connected to a primary cell such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle charge feature.

SQW/INT (Square-Wave/Interrupt Output)-The SQW/INT pin provides a programmable square-wave output or interrupt-output signal, as configured by the user. This pin features an open-drain output stage and therefore requires an external pull-up resistor to ensure proper logic-level signaling.

X1, X2-The X1 and X2 pins are connections for a standard 32.768 kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6 pF. Alternatively, the FRTC1339M may be driven by an external 32.768 kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is left floating.

The oscillator is controlled by an enable bit located in the control register. Oscillator startup times are highly dependent on crystal characteristics, PC board leakage, and layout design. High equivalent series resistance (ESR) and excessive capacitive loads are the primary contributors to extended startup durations. With a crystal meeting the recommended specifications and proper PCB layout, the oscillator typically starts within one second.

8.3 Clock Accuracy

The address map for the FRTC1339M registers is shown in the figure below. The overall timekeeping accuracy of the clock is influenced by several factors. Primary among these are the precision of the external crystal itself and the degree to which the capacitive load presented by the oscillator circuit matches the load capacitance for which the crystal was trimmed. Any mismatch between these capacitances will introduce frequency deviation and degrade accuracy. Additionally, temperature-induced frequency drift of the crystal contributes further error. External circuit noise coupled into the oscillator circuitry may also cause the clock to run fast.

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8.4 Address Map

During a multibyte access, when the address pointer reaches the end of the register space (address 10h), it wraps around to location 00h. On a 2-wire START, STOP, or when the address pointer increments to location 00h, the current time is transferred from the main registers to a secondary set of registers. All time information read during a transaction is sourced from these secondary registers, while the main clock continues to run independently. This double-buffering scheme eliminates the need to re-read the registers in the event that the main registers update during a read operation.

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function	Range
00H	0	10 Seconds			Seconds				Seconds	00-59
01H	0	10 Minutes			Minutes				Minutes	00-59
02H	0	12/24	AM/PM 10HR	10HR	Hour				Hours	1-12 +AM/PM 00-23
03H	0	0	0	0	0	Day			Day	1-7
04H	0	0	10 Date		Date				Date	00-31
05H	Century	0	0	10 Month	Month				Month/ Century	01-12 +Century
06H	10 Year				Year				Year	00-99
07H	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00-59
08H	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00-59
09H	A1M3	12/24	AM/PM 10 Hour	10 Hour	Hour				Alarm 1 Hours	1-12 +AM/PM 00-23
0AH	A1M4	DY/DT	10 Date		Day Date				Alarm 1 Day Alarm 1 Date	1-7 1-31
0BH	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00-59
0CH	A2M3	12/24	AM/PM 10 Hour	10 Hour	Hour				Alarm 2 Hours	1-12 +AM/PM 00-23
ODH	A2M4	DY/DT	10 Date		Day Date				Alarm 2 Day Alarm 2 Date	1-7 1-31
0EH	EOSC	0	BBSQI	RS2	RS1	INTCN	A2IE	A1IE	Control	-
0FH	OSF	0	0	0	0	0	A2F	A1F	Status	-
10H	TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	Trickle Charge	-

Figure: FRTC1339M TIMEKEEPER REGISTERS

Note: Unless otherwise specified, the registers' state are not defined when power is first applied or V_{CC} and V_{BACKUP} falls below the V_{BACKUP} min. All registers need to be initialized after power-on.

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8.5 Time And Date Operation

Time and date information is obtained by reading the appropriate register bytes, as illustrated in the timekeeper registers figure. Similarly, the time and date are set or initialized by writing to the corresponding register bytes. All time and date register contents are stored in binary-coded decimal (BCD) format.

The FRTC1339M supports both 12-hour and 24-hour timekeeping formats. Bit 6 of the hours register serves as the mode-select bit: when set to logic 1, the 12-hour mode is selected; when cleared to logic 0, the 24-hour mode is active. In 12-hour mode, bit 5 functions as the AM/PM indicator, with logic 1 representing PM and logic 0 representing AM. In 24-hour mode, bit 5 acts as the second 10-hour bit, extending the range to 20 – 23 hours. Whenever the 12/24-hour mode bit is changed, all hours values—including those for the alarms—must be re-entered.

The century bit (bit 7 of the month register) toggles when the year register overflows from 99 to 00. The day-of-week register increments at midnight. The values assigned to each day of the week are user-defined but must follow a sequential order—for example, if 1 represents Sunday, then 2 must represent Monday, and so forth. Illogical or non-sequential time and date entries may result in undefined operation.

To prevent errors during internal register updates, secondary (user) buffers are employed when reading or writing the time and date registers. When reading, these user buffers are synchronized to the internal registers upon any START or STOP condition, as well as when the address pointer rolls over to 00h. The countdown chain is reset whenever the seconds register is written; write transfers occur on the acknowledge pulse from the device. Once the countdown chain is reset, the remaining time and date registers must be written within one second to avoid rollover issues. The 1 Hz square-wave output, if enabled, transitions high 500 ms after the seconds data transfer, provided the oscillator is already running.

8.6 Alarms

The FRTC1339M incorporates two time-of-day/date alarms. Alarm 1 is programmed by writing to registers 07h through 0Ah, while Alarm 2 is configured via registers 0Bh through 0Dh. The alarms can be programmed—through the alarm enable and INTCN bits in the control register—to activate the SQW/INT output upon an alarm match condition.

Bit 7 of each alarm register serves as a mask bit. When all mask bits for a given alarm are set to logic 0, the alarm triggers only when the values in the timekeeping registers (00h – 06h) exactly match the values stored in the corresponding alarm registers. Alternatively, the alarms can be programmed to repeat at intervals such as every second, minute, hour, day, or date. The possible configurations are summarized in the table below. Any settings not listed in the table may result in illogical operation.

The DY/DT bits (bit 6 of the alarm day/date registers) determine whether the alarm value stored in bits 0 through 5 of that register corresponds to the day of the week or the date of the month. When DY/DT is set to logic 0, the alarm condition is evaluated against the date of the month. When set to logic 1, the alarm condition is evaluated against the day of the week.

When the RTC register values match the alarm register settings, the corresponding alarm flag bit (A1F or A2F) is set to logic 1. If the associated alarm interrupt enable bit (A1IE or A2IE) is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition activates the SQW/INT output signal.

DY/DT	Alarm 1 Register Mask Bits (BIT 7)				Alarm Rate
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

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DY/DT	Alarm 2 Register Mask Bits (BIT 7)			Alarm Rate
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 second of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

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9 Special Purpose Registers

The FRTC1339M has two additional registers (control and status) that control the RTC, alarms, and square-wave output.

9.1 Control Register (0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EOSC	0	BBSQI	RS2	RS1	INTCN	A2 IE	A1 IE

EOSC (Enable Oscillator) - This bit controls the oscillator operation: when set to logic 0, the oscillator is started and enabled; when set to logic 1, the oscillator is stopped. Upon initial power application, this bit is automatically set to logic 0 (enabled), ensuring the oscillator begins running immediately..

BBSQI (Battery-Backed Square-Wave and Interrupt Enable) - This bit, when set to logic 1, enables the square-wave or interrupt output while VCC is absent and the FRTC1339M is powered by the VBACKUP pin. When BBSQI is set to logic 0, the SQW/INT pin enters a high-impedance state when VCC falls below the power-fail trip point. This bit is disabled (logic 0) upon initial power application.

RS2 and RS1 (Rate Select) - These bits control the frequency of the square-wave output when the square-wave function has been enabled. The table below lists the square-wave frequencies that can be selected with the RS bits. Both bits are set to logic 1 (32 kHz) when power is first applied.

Square-Wave Output Frequency

RS2	RS1	SQW Output Frequency
0	0	1HZ
0	1	4.096kHz
1	0	8.192kHz
1	1	32.768kHz

INTCN (Interrupt Control)-This bit controls the relationship between the two alarms and the interrupt output pins. When the INTCN bit is set to logic 1, a match between the timekeeping registers and the Alarm 1 or Alarm 2 registers activates the SQW/INT pin (provided that the alarms are enabled). When the INTCN bit is set to logic 0, a square wave is output on the SQW/INT pin. This bit is set to logic 0 when power is first applied.

A1IE (Alarm 1 Interrupt Enable) - When set to logic 1, this bit permits the A1F bit in the status register to assert the SQW/INT output (when INTCN = 1). When the A1IE bit is set to logic 0 or INTCN is set to logic 0, the A1F bit does not initiate an interrupt signal. The A1IE bit is disabled (logic 0) when power is first applied.

A2IE (Alarm 2 Interrupt Enable) - When set to logic 1, this bit permits the A2F bit in the status register to assert the SQW/INT output (when INTCN = 1). When the A2IE bit is set to logic 0 or INTCN is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

9.2 Status Register (0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSF	0	0	0	0	0	A2F	A1F

OSF (Oscillator Stop Flag) - A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and can be used to judge the validity of the clock and date data. This bit is edge-triggered and set to logic 1 anytime the oscillator stops . The following are examples of conditions that can cause the OSF bit to be set:

1. The OSF (Oscillator Stop Flag) bit is set to logic 1 when any of the following conditions occur:
2. The first time power is applied to the device.
3. The voltage present on both VCC and VBACKUP is insufficient to support oscillation.
4. The EOSC bit is turned off (oscillator disabled).

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5. External influences on the crystal, such as noise, leakage, or other environmental factors.
6. This bit remains at logic 1 until it is written to logic 0. The OSF bit can only be written to logic 0; attempting to write logic 1 has no effect. 1 leaves the value unchanged.

A1F (Alarm 1 Flag) - A logic 1 in the A1F bit indicates that the current time matched the Alarm 1 register settings. If the A1IE bit is set to logic 1 and the INTCN bit is set to logic 1, the SQW/INT pin is also asserted. The A1F bit is cleared when written to logic 0. This bit can only be written to logic 0; attempting to write logic 1 leaves the value unchanged.

A2F (Alarm 2 Flag) - A logic 1 in the A2F bit indicates that the time matched the Alarm 2 registers. If the A2IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/ INT pin is also asserted. A2 F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

9.3 Trickle Charge Register (10h)

The simplified schematic in Figure: Programmable Trickle Charge illustrates the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4 - 7) control the enabling of the trickle charger. To prevent accidental activation, only the pattern 1010 enables the charger; all other patterns disable it. The trickle charger is disabled when power is first applied.

The diode select (DS) bits (bits 2 and 3) determine whether a diode is connected between VCC and VBACKUP. The ROUT bits (bits 0 and 1) select the value of the resistor connected between VCC and VBACKUP. The bit value configurations are shown in the table below.

Table: Trickle Charge Register (10h) Bit Values

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function
TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
X	X	X	X	X	X	0	0	Disabled
1	0	1	0	0	1	0	1	No diode, 250Ω resistor
1	0	1	0	1	0	0	1	One diode, 250 Ω resistor
1	0	1	0	0	1	1	0	No diode, 2k Ω resistor
1	0	1	0	1	0	1	0	One diode, 2 k Ω resistor
1	0	1	0	0	1	1	1	No diode, 4k Ω resistor
1	0	1	0	1	0	1	1	One diode, 4 k Ω resistor

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The diode and resistor selection is determined by the user according to the maximum charging current desired for the battery or supercapacitor. The maximum charging current can be calculated as illustrated in the following example:

Assume that a system power supply of 3.3V is applied to VCC and a super cap is connected to VBACKUP. Also assume that the trickle charger has been enabled with a diode and resistor R2 between V_{CC} and V_{BACKUP}. The maximum current I_{MAX} would, therefore, be calculated as follows:

$$I_{MAX} = (3.3V - \text{diode drop}) / R2 \approx (3.3V - 0.7V) / 2k\Omega \approx 1.3mA$$

As the super cap or battery charges, the voltage drop between VCC and V BACKUP decreases and, therefore, the charge current decreases.

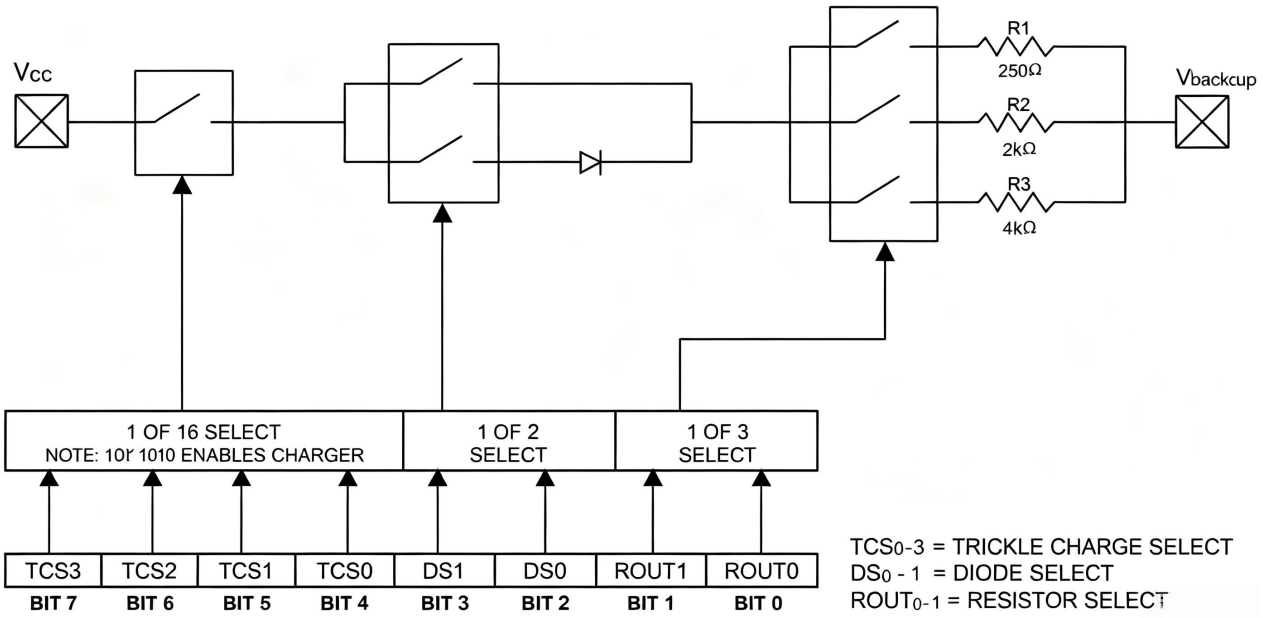

Figure 5: Programmable Trickle Charge

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10 I2C Bus

The FRTC1339M supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access , and generates the START and STOP conditions. The FRTC1339M operates as a slave on the 2- wire bus. Connections to the bus are made by the open- drain I/ O lines SDA and SCL.

The following bus protocol has been defined (Figure: Data Transfer on I2C Serial Bus).

1) Data transfer can be initiated only when the bus is not busy.
2) During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly , the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW , while the clock is HIGH, defines a START condition .

Stop data transfer: A change in the state of the data line , from LOW to HIGH, while the clock line is HIGH, defines the STOP condition .

Data valid: Following a START condition, the state of the SDA line is considered valid data when it remains stable throughout the HIGH period of the SCL clock signal. Any changes to the data line must occur while the clock signal is LOW. Each data bit corresponds to one clock pulse.

Every data transfer is initiated by a START condition and terminated by a STOP condition. The number of data bytes transmitted between START and STOP is not fixed and is determined by the master device. Data is transferred on a byte-wide basis, with each byte followed by a ninth acknowledge bit generated by the receiver.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull the SDA line low during the acknowledge clock pulse, ensuring that SDA remains stable at a logic-low level throughout the entire high period of the acknowledge-related clock pulse. Proper setup and hold times must be observed to guarantee reliable ACK detection.

To signal the end of a data transfer, the master must not generate an acknowledge bit (i.e., it must issue a NACK) on the last byte clocked out from the slave. In this case, the slave must release the SDA line and leave it high, enabling the master to generate a STOP condition and terminate the transaction. .

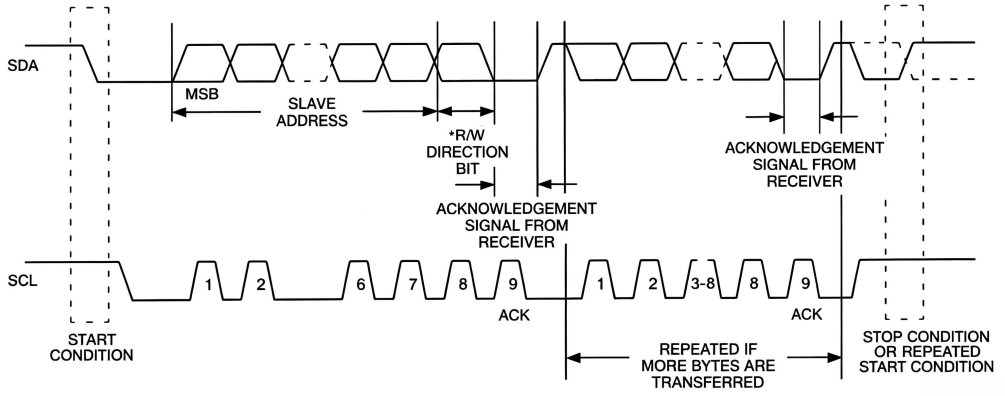

Figure 6 : Data Transfer on I2C Serial Bus

Depending upon the state of the R/W bit, two types of data transfer are possible:

Data transfer from a master transmitter to a slave receiver. The master transmits the first byte, which contains the slave address. This is followed by a sequence of data bytes. The slave returns an acknowledge bit after each byte it receives. Data is transferred with the most significant bit (MSB) first.

Data transfer from a slave transmitter to a master receiver. The master initiates the transfer by transmitting the first byte, which contains the slave address. The slave then returns an acknowledge bit, after which it begins transmitting a number of data bytes. The master returns an acknowledge bit after every received byte except the last one; upon receiving the final byte, the master issues a not-acknowledge (NACK) to signal the end of the data transfer.

The master device is responsible for generating all serial clock pulses, as well as the START and STOP conditions. A transfer may be terminated either with a STOP condition or with a repeated START condition. Since a repeated START condition also serves as the beginning of the next serial transfer, the bus is not released between transactions. All data is transferred with the most significant bit (MSB) first.

The FRTC1339M can operate in the following two modes:

1) **Slave receiver mode (write mode) :** Serial data and clock are received through the SDA and SCL lines, respectively. An acknowledge bit is transmitted by the receiver after each byte is received. START and STOP conditions are recognized as the beginning and end of a serial transfer.

Address recognition is performed by the hardware after the reception of the slave address and the direction bit (R/W), as illustrated in Figure: Data Write. The slave address byte is the first byte received after the master generates a START condition. This byte contains the 7-bit FRTC1339M address—1101000—followed by the direction bit (R/W), which is set to 0 for a write operation.

After receiving and decoding the slave address byte, the slave outputs an acknowledge on the SDA line. Once the FRTC1339M acknowledges the slave address and write bit, the master transmits a register address to the FRTC1339M, which sets the internal register pointer. The FRTC1339M acknowledges this transfer as well.

The master may then transmit zero or more bytes of data, with the FRTC1339M acknowledging each byte received. The register pointer increments automatically after each data byte is transferred. The master generates a STOP condition to terminate the data write operation. .

2) **Slave transmitter mode (read mode) :** The first byte is received and handled in the same manner as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. The FRTC1339M transmits serial data on SDA while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer, as illustrated in Figure: Data Read.

The slave address byte is the first byte received after the master generates the START condition. This byte contains the 7-bit FRTC1339M address—1101000—followed by the direction bit (R/W), which is set to 1 for a read operation. After receiving and decoding the slave address byte, the slave outputs an acknowledge on the SDA line.

The FRTC1339M then begins transmitting data from the register address pointed to by the register pointer. If the register pointer is not set before the initiation of a read mode, the first address that is read is the last one stored in the register pointer. The register pointer is incremented after each byte is transferred. The FRTC1339M must receive a "not acknowledge" (NACK) to terminate a read operation..

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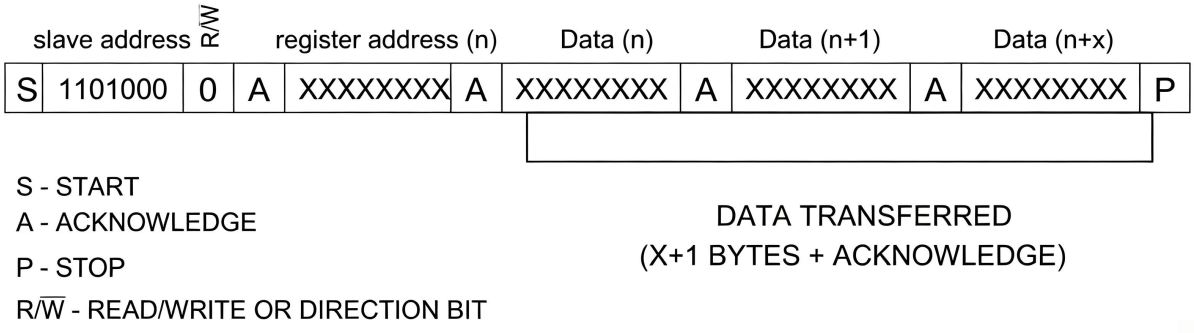

Figure 7 : Data Write— Slave Receiver Mode

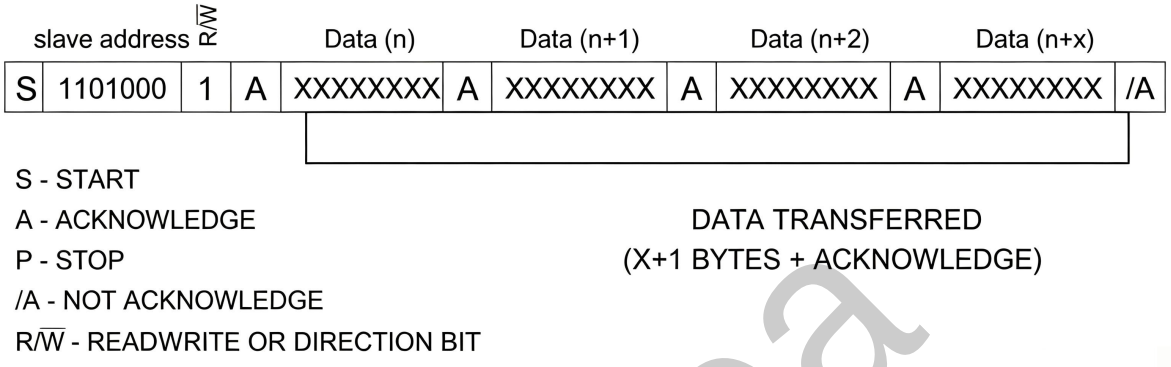

Figure 8: Data Read—Slave Transmitter Mode

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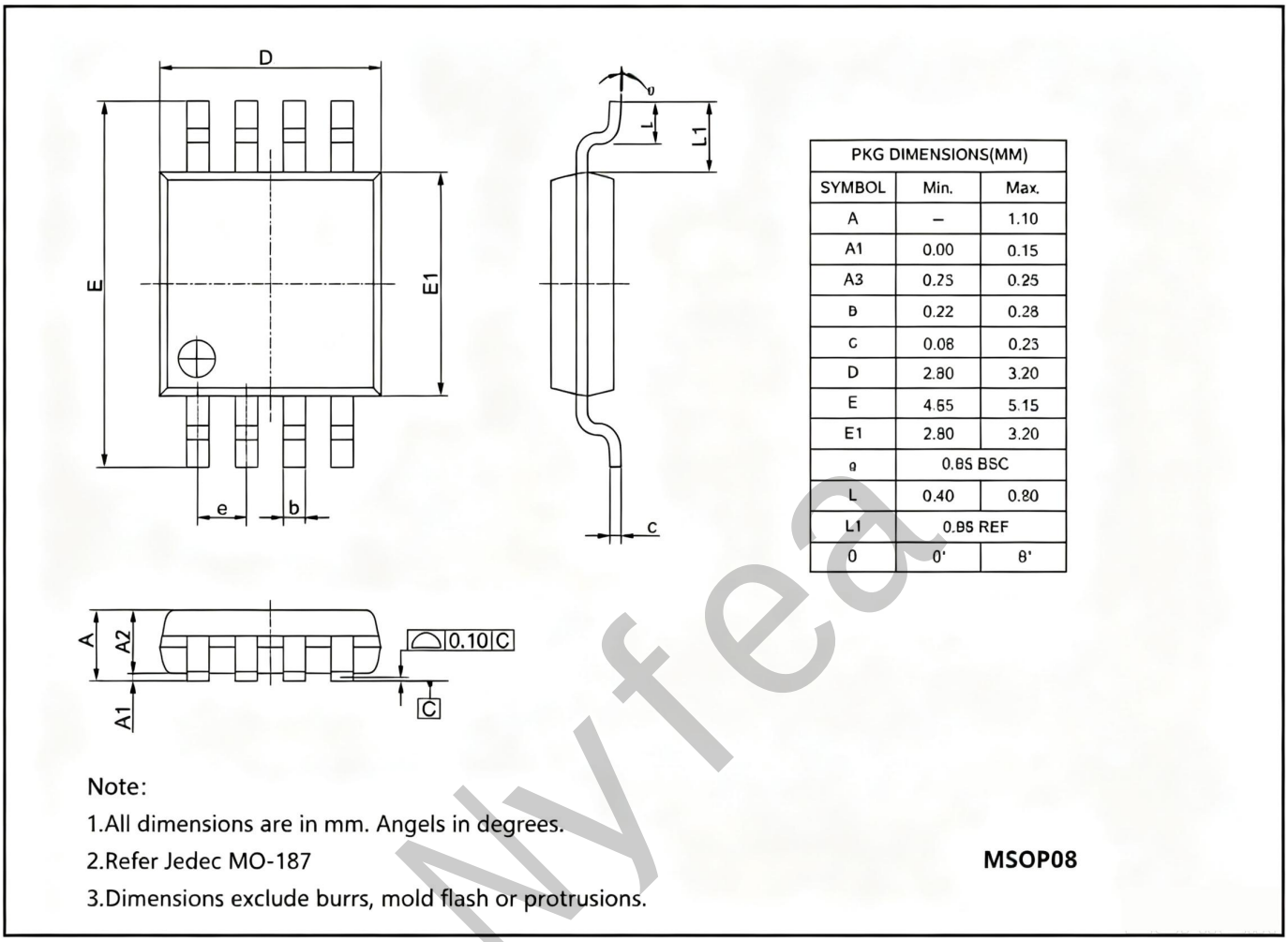
11 Package Information

FRTC1339M MSOP-8 Package



PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	–	1.10
A1	0.00	0.15
A3	0.25	0.25
B	0.22	0.28
C	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°

Note:

1.All dimensions are in mm. Angels in degrees.

2.Refer Jedec MO-187

3.Dimensions exclude burrs, mold flash or protrusions.

MSOP08

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12 Reel Information

Package	Reel size (inch)	1 pin location	Reel width (mm)	Winding step (mm)	Tail blank tape length (mm)	Head blank tape length(mm)	SPQ	Reel/inner box	Maximum circuits per box (K)	Inner box/outer box	Maximum circuit number of outer box (K)	Humidity level	Moisture-proof packing
MSOP08	13	Top left corner	12	8	240	1120	4000	1	4	8	32	3	Yes