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Nyfea product specification

PRODUCT SPECIFICATION

Customer: _____

Product Name: Real Time Clock

Part NO: FRTC8900

Issue Date: _____

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Prepared	Checked	Customer Check
ChenTT	Zelig	

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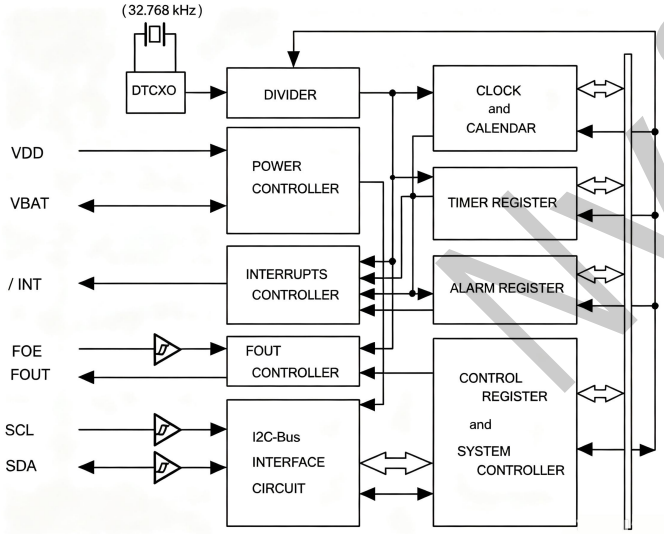
1 Features

- Integrated 32.768 kHz DTCXO
- High accuracy: within ±3.0 ppm
- Compatible with I2C high-speed mode (up to 400 kHz)
- Alarm interrupt capability configurable for day, date, hour, and minute
- Wake-up timer interrupt
- Time update interrupt for seconds and minutes
- Temperature-compensated 32.768 kHz output with output enable control (FOE and FOUT pins)
- Automatic leap-year adjustment (2000 through 2099)
- Broad interface voltage range: 2.5 V to 5.5 V
- Broad timekeeping voltage range: 1.6 V to 5.5 V
- Low power consumption: 0.54 μA at 3 V (typical)
- On-chip backup switchover circuitry with trickle charging
- Industrial temperature range (-40 ° C to +85 ° C)

2 Block Diagram



3 Description

This module is an I2C-bus-compatible real-time clock (RTC) that incorporates a 32.768 kHz DTCXO.

Beyond its calendar capabilities (year, month, date, day, hour, minute, second) and clock counter operation, the module offers a wide range of additional features, including alarm functionality, a wake-up timer, a time update interrupt, and a 32.768 kHz output.

Through its battery backup switchover capability and interface power supply input pin, the FRTC8900 accommodates a variety of power supply configurations.

The devices within this module are manufactured using a CMOS process to achieve low current draw, allowing for extended battery backup operation.

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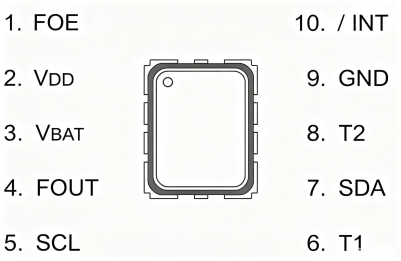
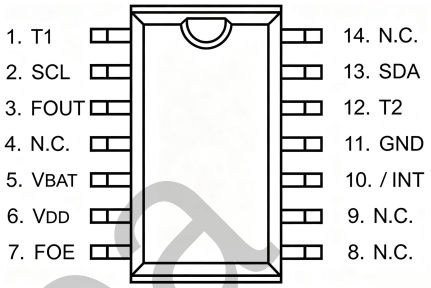
4 Packege and Ordering Information

Ordering Code	Package	Package Description	Δf / f Frequency stability			
			Condition	MIN	TYP	MAX
FRTC8900S		SOP-14 (10. 1mmX7. 1mm)	Ta= 0 to +50℃, VDD=3.0 V	-1.5		1.5
			Ta= -40 to +85℃, VDD=3.0 V	-3		3
FRTC8900CE		3225-10(3.2mmX2.5mm)	Ta= -40 to +85℃, VDD=3.0 V	-3		3

5 Pin Configuration



3225-10L



SOP-14

Pin Name	3225-10	SOP-14	I/O Type	Description
FOE	1	7	Input	This is an input pin used to control the output mode of the FOUT pin. When this pin's level is high, the FOUT pin is in output mode. When it is low, output via the FOUT pin is stopped.
VDD	2	6	Power	This pin is connected to a positive power supply.
V_{BAT}	3	5	Power	This is the power supply pin for backup battery. Connect this pin to a large-capacity capacitor, a secondary battery or similar. When the battery switchover function is not needed, VBAT must be connected to VDD.
FOUT	4	3	Output	This is the C-MOS output pin with output control provided via the FOE pin. When FOE = "H" (high level), this pin outputs a 32.768 kHz signal. (depend on FSEL bit) When output is stopped, the FOUT pin = "Hi-Z" (high impedance).
SCL	5	2	Input	This is the serial clock input pin for I2C Bus communications.
T1	6	1	Input	Used by the manufacturer for testing. (Do not connect externally.)
SDA	7	13	I/O	This pin's signal is used for input and output of address, data, and ACK bits, synchronized with the serial clock used for I2C communications. Since the SDA pin is an N-ch open drain pin during output, be sure to connect a suitable pull- up resistance relative to the signal line capacity.
T2	8	12	Input	Used by the manufacturer for testing. (Do not connect externally.)
GND	9	11	Power	This pin is connected to ground.
/INT	10	10	Input	This pin is used to output alarm signals, timer signals, time update signals, and other signals. This pin is an open drain pin.
N.C.		4, 8, 9, 14	-	This pin is not connected to the internal IC. Leave N.C. pins open or connect them to GND or VDD.

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6 Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
T_{store}	Storage Temperature	-55	_	+125	° C
V_{DD}	DC Supply Voltage VDD	-0.3	_	6.5	V
V_{BAT}	Battery Supply voltage	-0.3	_	6.5	V
V_I	Input Voltage on FOE, SCL, SDA	GND-0.3	_	6.5	V
V_{O1}	Output Voltage on FOUT pins	GND-0.3		VDD+0.3	V
V_{O2}	Output Voltage on SDA and /INT pins	GND-0.3		6.5	V
LU	Latch-Up			±200	mA
CDM	Charged Device Model			1000	V
HBM	Human Body Model			4000	V

Notes:
Applying stress levels beyond those specified in the MAXIMUM RATINGS may result in permanent damage to the device. These values are provided as stress limits only, and proper device operation under these conditions or any other conditions exceeding those stated in the operational sections of this specification is not guaranteed. Prolonged exposure to absolute maximum rating conditions may compromise device reliability.

7 Recommended operation conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{DD}	Operating supply voltage in normal mode	2.5	3.0	5.5	V
V_{BAT}	Backup power supply voltage	1.6	3.0	5.5	V
V_{TEM}	Temp. compensation voltage	2.0	3.0	5.5	V
T_{OPR}	Operating temperature	-40		85	℃

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8 DC Electrical Characteristics

Unless otherwise specified, -40 ° C≤T_A≤ 85 ° C

Symbol	Item	Condition		MIN	TYP	MAX	Unit
I_{DD1}	Average Current Consumption (1)	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = GND, V_{DD} = V_{BAT} FOUT: output OFF (High Z) Compensation interval 2.0 s VDET3 voltage detection time 2ms	V_{DD} = 5 V		0.59	2.4	μA
I_{DD2}	Average Current Consumption (2)		V_{DD} = 3 V		0.54	2.2	
I_{DD3}	Average Current Consumption (3)	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = V_{DD} , V_{DD} = V_{BAT} FOUT :32.768 kHz, CL =0pF Compensation interval 2.0 s VDET3 voltage detection time 2ms	V_{DD} = 5 V		1.66	3.4	μA
I_{DD4}	Average Current Consumption (4)		V_{DD} = 3 V		1.18	2.8	
V_{IH}	High-level Input voltage	SCL, SDA, FOE pins		0.8 × V_{DD}		5.5	V
V_{IL}	Low-level Input voltage	SCL, SDA, FOE pins		GND - 0.3		0.2 × V_{DD}	V
V_{OH1}	High-level output voltage	FOUT pin	V_{DD}=5 V, I_{OH}=-1 mA	4.5		5.0	V
V_{OH2}			V_{DD}=3 V, I_{OH}=-1 mA	2.2		3.0	
V_{OH3}			V_{DD}=3 V, I_{OH}=-100 μA	2.9		3.0	
V_{OL1}	Low-level output voltage	FOUT pin	V_{DD}=5 V, I_{OL}= 1 mA	GND		GND+0.5	V
V_{OL2}			V_{DD}=3 V, I_{OL}= 1 mA	GND		GND+0.8	
V_{OL3}			V_{DD}=3 V, I_{OL}= 100 μA	GND		GND+0.1	
V_{OL4}		/ INT pin	V_{DD}=5 V, I_{OL}= 1 mA	GND		GND+0.25	V
V_{OL5}			V_{DD}=3 V, I_{OL}= 1 mA	GND		GND+0.4	
V_{OL6}		SDA pin	V_{DD} ≥2 V, I_{OL}=3 mA	GND		GND+0.4	V
I_{LK}	Input leakage current	FOE, SCL, SDA pins, V_{IN} = V_{DD} or GND		-0.5		0.5	μA
I_{OZ}	Output leakage current	/ INT, SDA, FOUT pins, V_{OUT} = V_{DD} or GND		-0.5		0.5	μA

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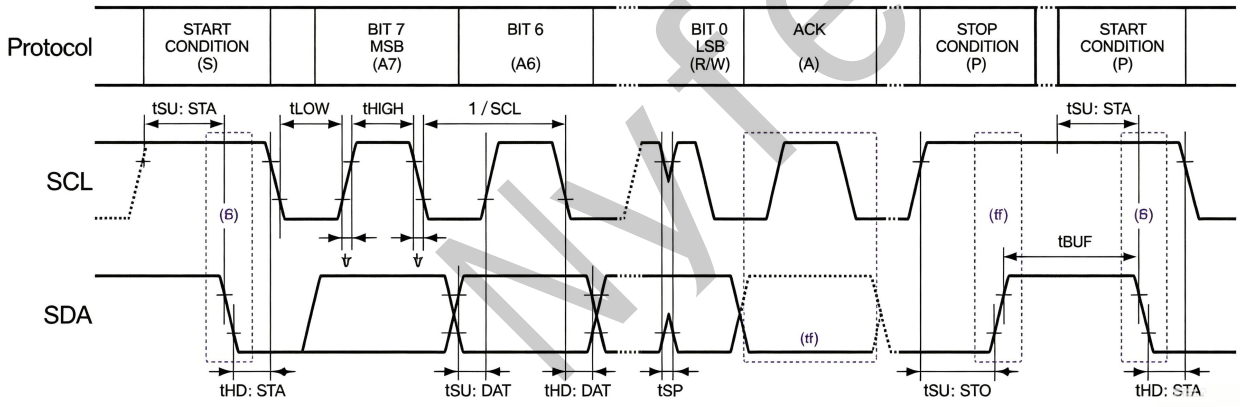
9 AC Characteristics - I2C Bus

Unless otherwise specified, -40 ° C≤TA≤ 85 ° C

Item	Symbol	Condition	MIN	TYP	MAX	Unit
SCL clock frequency	f_{SCL}				400	kHz
Start condition setup time	$t_{SU;STA}$		0.6			μs
Start condition hold time	$t_{HD;STA}$		0.6			μs
Data setup time	$t_{SU;DAT}$		100			ns
Data hold time	$t_{HD;DAT}$		0			ns
Stop condition setup time	$t_{SU;STO}$		0.6			μs
Bus idle time between start condition and stop condition	t_{BUF}		1.3			μs
Time when SCL = "L"	t_{LOW}		1.3			μs
Time when SCL = "H"	t_{HIGH}		0.6			μs
Rise time for SCL and SDA	t_r				0.3	μs
Fall time for SCL and SDA	t_f				0.3	μs
Allowable spike time on bus	t_{SP}				50	ns



10 AC Characteristics - Frequency

Unless otherwise specified, -40 ° C≤TA≤ 85 ° C

Symbol	Parameter	Suffix	Condition	MIN	TYP	MAX	Unit
f / V	Frequency/voltage characteristics		Ta= +25℃, VDD=2.0 V to 5.5 V	-1		1	ppm
t_{STA}	Oscillation start time		Ta= +25℃, VDD= 1.6 V to 5.5 V			0.5	s
			Ta= -40 to +85℃, VDD= 1.6 V to 5.5 V			1	
fa	Aging		Ta= +25℃, VDD=3.0 V, first year	-3		3	ppm
T_{sensor}	Temperature Sensor Accuracy		VDD=3.0 V	-4		4	℃
Duty	FOUT duty		50% of VDD level	40	50	60	%

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11 Register Table

11.1 Basic Time and Calendar Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
00 or 10	SEC	○	40	20	10	8	4	2	1	R/W
01 or 11	MIN	○	40	20	10	8	4	2	1	R/W
02 or 12	HOUR	○	○	20	10	8	4	2	1	R/W
03 or 13	WEEK	○	6	5	4	3	2	1	0	R/W
04 or 14	DAY	○	○	20	10	8	4	2	1	R/W
05 or 15	MONTH	○	○	○	10	8	4	2	1	R/W
06 or 16	YEAR	80	40	20	10	8	4	2	1	R/W
07	RAM	●	●	●	●	●	●	●	●	R/W
08	MIN Alarm	AE	40	20	10	8	4	2	1	R/W
09	HOUR Alarm	AE	●	20	10	8	4	2	1	R/W
0A	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
	DAY Alarm		●	20	10	8	4	2	1	R/W
0B or 1B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0C or 1C	Timer Counter 1	●	●	●	●	2048	1024	512	256	R/W
0D or 1D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	R/W
0E or 1E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	R/W
0F or 1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET	R/W

Note:

1 After the first power-up (starting from 0 V), or if the VLF bit reads back as "1", be sure to initialize all registers before using the RTC. Take care not to enter incorrect date or time values, since clock operation cannot be guaranteed when the date or time data is invalid.

2 At initial power-up, the default register settings are as follows:

Initial value_0:

TEST, WADA, USEL, TE, FSEL1, FSEL0, TSEL0, UF, TF, AF, CSEL1, UIE, TIE, AIE, RESET, VDETOFF, SWOFF, BKSMP1, BKSMP0

Initial value_1:

TSEL1, VLF, VDET, CSEL0

At this stage, all remaining register values are undefined, so a reset must be performed before using the module.

3 The UF, TF, AF, VLF, and VDET bits can only be written with a "0".

4 Any bit marked with "○" should be set to "0" after initialization.

5 Any bit marked with "." is a RAM bit that can be used to read or write arbitrary data.

6 The TEST bit is reserved for manufacturer testing. Always write "0" to this bit.

7 When the alarm function is not in use, registers 08h－0Ah may be repurposed as RAM. (AIE: "0")

8 Reads from registers at addresses 0Bh－0Ch return preset data.

9 When the timer function is not in use, registers 0Bh－0Ch may be repurposed as RAM. (TE, TIE: "0")

11.2 Temperature Data, Backup power supply control register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
17	TEMP	128	64	32	16	8	4	2	1	READ
18	Backup Function	○	○	○	○	VDET OFF	SW OFF	BK SMP1	BK SMP0	R/W
19	Not use	○	○	○	○	○	○	○	○	READ
1A	Not use	○	○	○	○	○	○	○	○	READ

The temperature data are updated during operation of the temperature compensation circuit.

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12 Details of Registers

12.1 Clock counter (SEC - HOUR)

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
00 or 10	SEC	○	40	20	10	8	4	2	1	R/W
01 or 11	MIN	○	40	20	10	8	4	2	1	R/W
02 or 12	HOUR	○	○	20	10	8	4	2	1	R/W

Note:

1. "○" denotes write-protected bits. Reading these bits always returns zero.
2. The clock counter tracks seconds, minutes, and hours.
3. Data is represented in BCD format. For instance, a "seconds" register value of "0101 1001" corresponds to 59 seconds.
4. Note that writing invalid time data may disrupt normal operation of the clock counter.

12.1.1 Second counter

This second counter counts from "00" to "01," "02," and up to 59 seconds, after which it starts again from 00 seconds.

12.1.2 Minute counter

This minute counter counts from "00" to "01," "02," and up to 59 minutes, after which it starts again from 00 minutes.

12.1.3 Hour counter

This hour counter counts from "00" hours to "01," "02," and up to 23 hours, after which it starts again from 00 hours.

12.2 Calendar counter (WEEK - YEAR)

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
03 or 13	WEEK	○	6	5	4	3	2	1	0	R/W

Day-of-the-Week Counter

The day of the week is represented by 7 bits, spanning bit 0 through bit 6.

The day data values increment in the following sequence: 01h, 02h, 04h, 08h, 10h, 20h, 40h, then back to 01h, 02h, and so on.

Week	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sunday	01h	0	0	0	0	0	0	0	1
Monday	02h	0	0	0	0	0	0	1	0
Tuesday	04h	0	0	0	0	0	1	0	0
Wednesday	08h	0	0	0	0	1	0	0	0
Thursday	10h	0	0	0	1	0	0	0	0
Friday	20h	0	0	1	0	0	0	0	0
Saturday	40h	0	1	0	0	0	0	0	0

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12.2.1 Date counter

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
04 or 14	DAY	○	○	20	10	8	4	2	1	R/W

The date counter advances dates differently depending on the month setting.
A leap year is recognized whenever the year value is divisible by four (for example, 04, 08, 12, 88, 92, or 96). During February of a leap year, the counter progresses through dates as "01," "02," "03," up to "28," then "29," followed by "01," and so on.

Month	Date update pattern
1, 3, 5, 7, 8, 10, or 12	1～31
4, 6, 9, or 11	1～30
February in normal year	1～28
February in leap year	1～29

12.2.2 Month counter

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
05 or 15	MONTH	○	○	○	10	8	4	2	1	R/W
06 or 16	YEAR	80	40	20	10	8	4	2	1	R/W

The month counter counts from 01 (January), 02 (February), and up to 12 (December), then starts again at 01 (January).

12.2.3 Year counter

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
06 or 16	YEAR	80	40	20	10	8	4	2	1	R/W

The year counter counts from 00, 01, 02 and up to 99, then starts again at 00.
Any year that is a multiple of four (04, 08, 12, 88, 92, 96, etc.) is handled as a leap year.

12.3 Alarm registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
08	MIN Alarm	AE	40	20	10	8	4	2	1	R/W
09	HOUR Alarm	AE	○	20	10	8	4	2	1	R/W
0A	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
	DAY Alarm		○	20	10	8	4	2	1	R/W

The alarm interrupt function works together with the AIE, AF, and WADA bits to configure alarms for designated date, day, hour, and minute values.
Once the values set in the alarm registers and the WADA bit match the current time, the /INT pin is driven low, and the AF bit is set to "1" to signal that an alarm interrupt event has been triggered.
Note:The AE bit is active-low. Therefore, to enable an interrupt once per hour when the current minutes match the alarm setting, set the AE bit of register 08h to 0, while setting the AE bits of registers 09h and 0Ah to 1.
To generate an alarm interrupt only once per week, all three AE bits must be set to "0."

1) The alarm function is not a hardware feature but rather a software function implemented inside the RTC.
2) If the "AE" bit of register 0Ah is set to "1," the day setting is ignored, and an interrupt is generated once the current time matches the minute and/or hour setting in the alarm register

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(Example) Writing 80h (AE = "1") to the WEEK Alarm / DAY Alarm register (Reg - 0Ah):
In this case, only the hour and minute settings serve as alarm comparison targets. The week and date settings are excluded from the alarm comparison. Consequently, an alarm is triggered whenever only the hour and minute values match the alarm data.

3) If all three AE bit values are " 1" the week/date and time settings are ignored, and an alarm interrupt event will occur once per minute.

12.4 Fixed-cycle timer control registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0B or 1B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0C or 1C	Timer Counter 1	○	○	○	○	2048	1024	512	256	R/W

Note:
These registers are used to configure the preset countdown value for the fixed-cycle timer interrupt function. The TE, TF, TIE, and TSEL0/1 bits are also involved in setting up this function.
Once a fixed-cycle timer interrupt event occurs, the /INT pin is driven low, and the TF bit is set to "1".

12.5 Extension registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0B or 1B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0C or 1C	Timer Counter 1	○	○	○	○	2048	1024	512	256	R/W
0D or 1D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	R/W

Note:
1. The default value is the value that is read (or is set internally) after powering up from 0 V
2. "0" mandatory" 0" Make sure to always write 0 into this bit.
3. "-" indicates a default value is undefined.

This register is used to specify the target for the alarm function or time update interrupt function and to select or set operations such as fixed-cycle timer operations.

12.5.1 TEST bit

This bit is reserved for manufacturer testing and must always remain "0." Take care not to write a "1" to this bit when modifying other bits.

TEST	Data	Description
Write/Read	0	Normal operation mode (Default)
	1	Setting prohibited (manufacturer's test bit)

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12.5.2 WADA (Week Alarm/Day Alarm) bit

This bit selects whether WEEK or DAY is used as the target for the alarm interrupt function.
Writing a "1" to this bit selects a DAY alarm, meaning the alarm interrupt is triggered whenever the set time is reached, regardless of the actual day.
Writing a "0" to this bit selects a WEEK alarm, so an alarm interrupt is generated only when the set time is reached on a specific day of the week.

12.5.3 USEL (Update Interrupt Select) bit

This bit determines whether the RTC issues a "second update" or "minute update" interrupt, enabling external clocks to be synchronized with the RTC's time registers.

USEL	Data	update interrupts	Auto reset time tRTN
Write/Read	0	second update (Default)	500 ms
	1	minute update	Min. 7.813 ms

12.5.4 TE (Timer Enable) bit

This bit controls whether the fixed-cycle timer interrupt function starts or stops.
Writing a "1" to this bit starts the fixed-cycle timer interrupt function (a countdown begins from the preset value).
Writing a "0" to this bit stops the fixed-cycle timer interrupt function.

12.5.5 FSEL0, 1 (FOUT frequency Select 0 , 1) bits

The combination of these two bits is used to set the FOUT frequency. Note: All frequencies are temperature compensated

FSEL1	FSEL0	FOUT
0	0	32768Hz
0	1	1024Hz
1	0	1Hz
1	1	32768

12.5.6 TSEL0, 1 (Timer Select 0, 1) bits

The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function.

TSEL1	TSEL0	Timer		Auto reset time tRTN (Min.)	Effect of RESET bit
0	0	4096 Hz	Once per 244.14 μs	122 us	———
0	1	64 Hz	Once per 15.625 ms	7.813 ms	Does not operate when the RESET bit value is "1".
1	0	"Second" update	Once per second	7.813 ms	
1	1	"Minute" update	Once per minute	7.813 ms	

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12.6 Flag register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0E or 1E	Flag Register	〇	〇	UF	TF	AF	〇	VLF	VDET	R/W

The default values are automatically loaded after power-on from 0 V.
"〇" denotes write-protected bits; reading these bits always returns zero.
"-" indicates that the default value is undefined.

12.6.1 UF (Update Flag) bit

If this flag bit is preset to "0," its value changes from "0" to "1" once a time update interrupt event occurs. After the flag bit becomes "1," it holds that value until a "0" is written to it.

12.6.2 TF (Timer Flag) bit

If this flag bit is preset to "0," its value changes from "0" to "1" once a fixed-cycle timer interrupt event occurs. After the flag bit becomes "1," it holds that value until a "0" is written to it.

12.6.3 AF (Alarm Flag) bit

If set to "0" beforehand, this flag bit's value changes from "0" to "1" when an alarm interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.

12.6.4 VLF (Voltage Low Flag) bit

VLF indicates whether clock functions and internal data have been reliably retained.
When VLF is set to "1," it signals the possibility that both stored data and clock/calendar data have been lost. There are two causes for VLF being set:

1. A supply voltage drop below 1.6 V (VCLK) was detected. The VLF voltage detector operates continuously, with a detection response time of roughly 1 ms to 10 ms.
2. The internal crystal oscillation stopped. This detector also operates continuously, with a detection response time of roughly 100 ms.

Once VLF is set to "1," it remains "1" until a "0" is written to it. After the initial power-on from 0 V, verify that VLF has been set to "1.

VLF	Data	Description
Write	0	The VLF bit is cleared to zero to prepare for the next status detection.
	1	Invalid (writing a 1 will be ignored)!
Read	0	No supply voltage drop occurred, so data are not compromised.
	1	Low voltage has been detected, so data loss might have occurred, and time information might be compromised. All registers must be initialized. (This setting is retained until a "zero" is written to this bit.)

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12.6.5 VDET (Voltage Detection Flag) bit

VDET indicates whether temperature compensation has been reliably retained.
When VDET is set to "1," it signals the possibility that the clock stability history has been lost.
The cause of VDET being set is a detected supply voltage drop below 1.95 V (VDET).
VDET is checked at every temperature compensation timing, with a detection response time of roughly 1 ms to 10 ms. Once VDET becomes "1," it remains "1" until a "0" is written to it.
After powering up from 0 V, make sure to set this bit's value to "1."

VDET	Data	Description
Write	0	The VDET bit is cleared to zero to prepare for the next low voltage detection.
	1	Invalid (writing a 1 will be ignored)!
Read	0	Temperature compensation is normal.
	1	Temperature compensation has been stopped.

12.7 Control register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0F or 1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET	R/W

Notes
The default value refers to the value that is read (or set internally) after power-up from 0 V.
"○" denotes write-protected bits; reading these bits always returns zero.
"-" indicates that no default value has been defined..

This register is used to control interrupt event output from the /INT pin and the stop/start status of clock and calendar operations.

12.7.1 CSEL0 , 1 (Compensation interval Select 0 , 1) bits

The combination of these two bits is used to set the temperature compensation interval.

CSEL1	CSEL0	Compensation Interval
0	0	0.5s
0	1	2.0s (default)
1	0	10s
1	1	30s

12.7.2 UIE (Update Interrupt Enable) bit

When a time update interrupt event occurs (i.e., when the UF bit transitions from "0" to "1"), this bit determines whether an interrupt signal is produced (the /INT pin switches from Hi-Z to low) or not (the /INT pin stays Hi-Z).
Writing a "1" to this bit causes an interrupt signal to be generated (the /INT pin switches from Hi-Z to low) when an interrupt event occurs.
Writing a "0" to this bit prevents any interrupt signal from being generated when an interrupt event occurs

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UIE	Data	Function
Write/Read	0	When a time update interrupt event occurs, an interrupt signal is notgenerated or is canceled (/INT status changes from low to Hi-Z).
	1	When a time update interrupt event occurs, an interrupt signal is generated(/INT status changes from Hi-Z to low). * When a time update interrupt event occurs, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is ″1″. This /INT status is automatically cleared(/INT status changes from low to Hi-Z) earliest 7.813 ms after the interrupt occurs.

12.7.3 TIE (Timer Interrupt Enable) bit

When a fixed-cycle timer interrupt event occurs (when the TF bit value changes from ″0″ to ″1″), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z). When a ″1″ is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.
When a ″0″ is written to this bit, no interrupt signal is generated when an interrupt event occurs.

TIE	Data	Function
Write/Read	0	When a fixed-cycle timer interrupt event occurs, an interrupt signal is notgenerated or is canceled (/INT status changes from low to Hi-Z).
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal isgenerated (/INT status changes from Hi-Z to low). * When a fixed-cycle timer interrupt event has been generated low-level output from the /INT pinoccurs only when the value of the control register's TIE bit is ″1″. Earliest 7.813 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi- Z).

12.7.4 AIE (Alarm Interrupt Enable) bit

When an alarm timer interrupt event occurs (when the AF bit value changes from ″0″ to ″1″), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).
When a ″1″ is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.
When a ″0″ is written to this bit, no interrupt signal is generated when an interrupt event occurs.

AIE	Data	Function
Write/Read	0	When an alarm interrupt event occurs, an interrupt signal is not generatedor is canceled (/INT status changes from low to Hi-Z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When an alarm interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's AIE bit is ″1″. This setting is retained until the AFbit value is cleared to zero. (No automatic cancellation)

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12.7.5 RESET bit

RESET bit was prepared for the synchronized starting of time or timer. The detailed function of reset.

For example.

S denotes a start condition, P denotes a stop condition, and RS denotes a repeated start condition.

S --- Slave address (write) --- ACK1 --- 0Fh --- ACK2 --- 01h --- ACK3 --- RS --- R/W access --- P.

The RESET bit is set at ACK3, but the RESET operation is not carried out at that point.

After the RESET bit is set, the RESET function takes effect momentarily at the following P (stop condition), and the RESET bit is automatically cleared. The portion of the circuit affected by RESET is the 2 Hz countdown chain derived from 16 kHz, which is cleared.

The next update timing of the seconds counter following RESET falls within a range of 1000 ms to 30.5 μs after the 1000 ms point. RESET influences the time update interrupt, alarm, and timer functions.

Note:
RESET is not released by the reception of a RE-START condition before receiving a STOP condition. Unnecessary use of RESET will be the cause of delay error of Calendar and Clock.

12.8 Temperature Data register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
17	TEMP	128	64	32	16	8	4	2	1	READ

Notes:
1. This register allows you to read digital temperature data.
2. The temperature data is refreshed while the temperature compensation circuit is running.
3. You can convert the temperature data to degrees Celsius using the following expression.

12.9 Backup power supply control register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
18	Backup Function	○	○	○	○	VDET OFF	SW OFF	BK SMP1	BK SMP0	R/W

This register controls the functionality of the power switchover and backup function.

12.9.1 VDETOFF bit (Voltage Detector OFF)

This bit controls the voltage detection circuit of the main power supply VDD.

12.9.2 SWOFF bit (Switch OFF)

This bit controls the internal P-MOS switch for preventing back flow between V_{core} and VBAT.

12.9.3 BKSMP1, BKSMP0 bit (Backup mode Sampling time)

These bits control the operation time when to be intermittently driven the VDD voltage detection.

12.9.4 SW2OFF bit (Switch OFF)

This bit controls the internal P-MOS switch for preventing back flow from VBAT.

12.9.5 The power switchover control.

To use the battery backup switchover function, the voltage comparator (VDD detector) must be enabled via the VDETOFF bit. When VDETOFF = 0, the power switchover function is active; when VDETOFF = 1, the function is disabled.

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When the power switchover function is active, the internal COMPEN signal is asserted 62.5 ms after the seconds counter increments, which activates the voltage comparator.

The comparator's active period (VDD measurement period) is governed by the BKSMP0 and BKSMP1 bits. Two modes are available: VDET3 < VDD (Normal Mode) and VDD ≤ VDET3 (Backup Mode).

12.10 Normal Mode

VDD voltage is detected every one second.

Comparator function intermittently ON, Pch-Switch intermittently OFF In case of VDD ≤VDET3, it moves to Backup Mode.

12.11 Backup Mode

VDD voltage is detected every one second.

Comparator function intermittently ON, Pch-Switch OFF in Backup Mode In case of VDET3 < VDD, it moves to Normal Mode.

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13 I2C Bus Interface

The FRTC8900 is compatible with the I2C protocol. In this protocol, the device that manages the message is referred to as the master, while devices controlled by the master are called slaves. The bus must be managed by a master device, which produces the serial clock (SCL), governs bus access, and generates the START and STOP conditions. The FRTC8900 functions as a slave on the I2C bus. The bus specifications define two modes: standard mode (100 kHz cycle rate) and fast mode (400 kHz cycle rate). The FRTC8900 supports both modes. Bus connections are established through the open-drain I/O lines SDA and SCL.

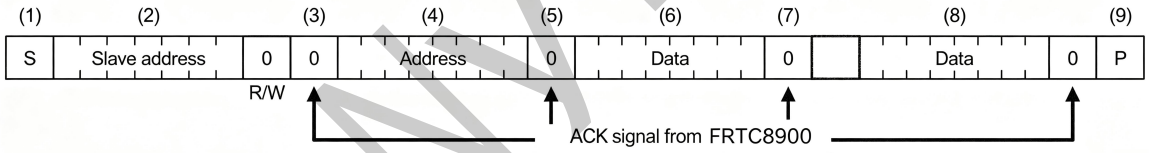
Slave addresses are fixed at a length of 7 bits. This RTC's slave address is [0110010]. An R/W bit (shown as "*" above) is appended to each 7-bit slave address during 8-bit transfers.

	Transfer Data	Slave Address							R/W bit
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	65 h	0	1	1	0	0	1	0	1= Read
Write	64 h								0 = Write

13.1 I2C write sequence

Because the FRTC8900 features an address auto-increment function, once the initial address is specified, the FRTC8900 advances the receive address by one byte each time data is transferred.

1) The CPU issues a start condition [S].
2) The CPU sends the FRTC8900's slave address with the R/W bit configured for write mode.
3) The CPU checks for an ACK signal from the FRTC8900.
4) The CPU sends the write address to the FRTC8900.
5) The CPU checks for an ACK signal from the FRTC8900.
6) The CPU sends write data to the address specified in step (4).
7) The CPU checks for an ACK signal from the FRTC8900.
8) Steps (6) and (7) are repeated as needed. Addresses are incremented automatically.
9) The CPU issues a stop condition [P].



13.2 I2C read sequence

After using write mode to write the address to be read, set read mode to read the actual data.

1) CPU transfers start condition [S].
2) CPU transmits the FRTC8900's slave address with the R/W bit set to write mode.
3) Check for ACK signal from FRTC8900.
4) CPU transfers address for reading from FRTC8900.
5) Check for ACK signal from FRTC8900.
6) CPU transfers RESTART condition [Sr] (in which case, CPU does not transfer a STOP condition [P]).
7) CPU transfers FRTC8900's slave address with the R/W bit set to read mode.
8) Check for ACK signal from FRTC8900(from this point on, the CPU is the receiver and the FRTC8900 is the transmitter).
9) Data from address specified at (4) above is output by the FRTC8900.
10) CPU transfers ACK signal to FRTC8900.
11) Repeat (9) and (10) if necessary. Read addresses are automatically incremented.
12) CPU transfers ACK signal for "1".
13) CPU transfers stop condition [P].

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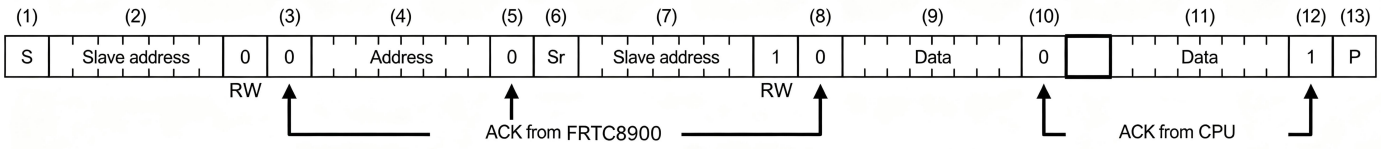
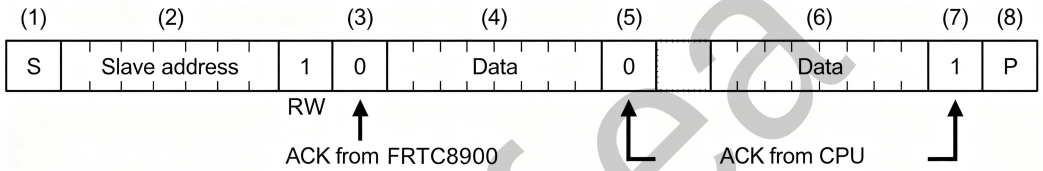


13.3 Read sequence when address is not specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address + 1.

1) CPU transfers start condition [S].
2) CPU transmits the FRTC8900's slave address with the R/W bit set to read mode.
3) Check for ACK signal from FRTC8900(from this point on, the CPU is the receiver and the FRTC8900 is the transmitter).
4) Data is output from the FRTC8900 to the address following the end of the previously accessed address
5) CPU transfers ACK signal to FRTC8900
6) Repeat (4) and (5) if necessary. Read addresses are automatically incremented in the FRTC8900.
7) CPU transfers ACK signal for " 1".
8) CPU transfers stop condition [P].



13.4 Address auto increment in Read/Write

In Basic time and calendar resister.

Address: 08 - 09 - 0A - 0B - 0C - 0D - 0E - 0F - 00 - 01 - 02 - In Extension resister

Address : 18 - 19 - 1A - 1B - 1C - 1D - 1E - 1F - 10 - 11 - 12 -

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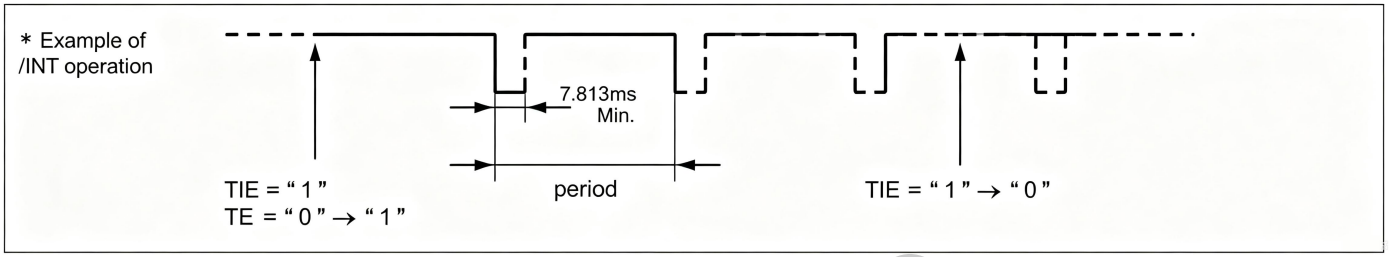
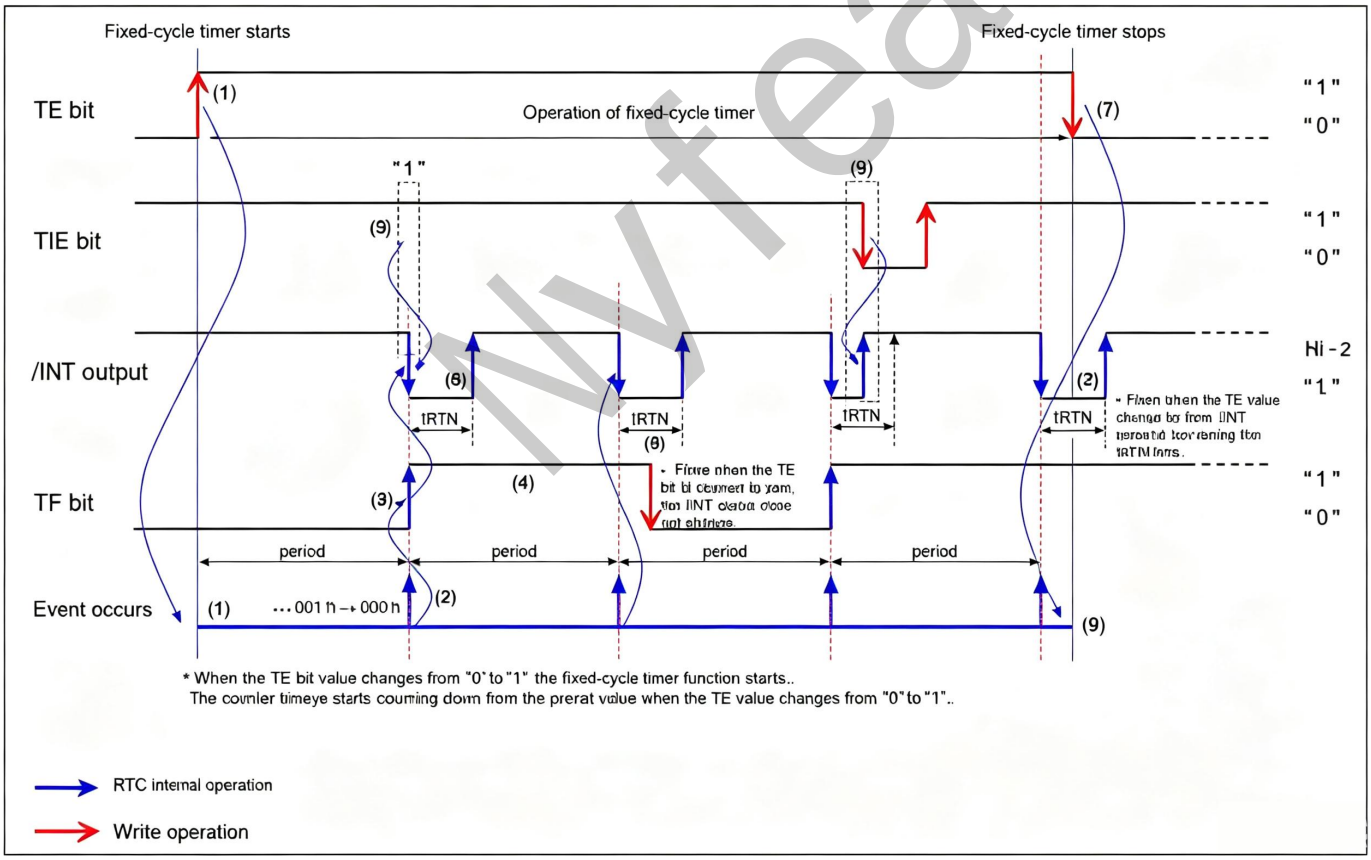
14 Function Description

14.1 Fixed Cycle Timer Interrupt Function

This interrupt is released automatically, making it well suited for wake-up timer or interval-based operation systems.
The fixed-cycle timer interrupt generation function periodically produces an interrupt event at any fixed cycle selected between 244.14 μs and 4095 minutes.
When an interrupt event occurs, the /INT pin is driven low, and the TF bit is set to "1" to indicate that an event has been generated. However, when a fixed-cycle timer interrupt event occurs, low-level output from the /INT pin is produced only if the control register's TIE bit is "1". At the earliest, 7.813 ms after the interrupt occurs, the /INT status is automatically cleared (the /INT status changes from low level to Hi-Z).



Fixed-cycle Timer Interrupt Timing Chart.



(1) When a " 1" is written to the TE bit, the fixed-cycle timer countdown starts from the preset value.
(2) A fixed-cycle timer interrupt event starts a countdown based on the countdown period (source clock). After the interrupt event occurs, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)
(3) When a fixed-cycle timer interrupt event occurs, " 1" is written to the TF bit.
(4) When the TF bit = " 1" its value is retained until it is cleared to zero.

(5) If the TIE bit = " 1" when a fixed-cycle timer interrupt occurs, /INT pin output goes low. If the TIE bit = "0" when a fixed-cycle timer interrupt occurs, /INT pin output remains Hi-Z.

(6) Output from the /INT pin remains low during the t_{RTN} period following each event, after which it is automatically cleared to Hi-Z status. /INT is again set low when the next interrupt event occurs.

(7) When a "0" is written to the TE bit, the fixed-cycle timer function is stopped, and the /INT pin is set to Hi-Z status. When /INT=low, the fixed-cycle timer function is stopped. The t_{RTN} period is the maximum amount of time before the /INT pin status changes from low to Hi-Z.

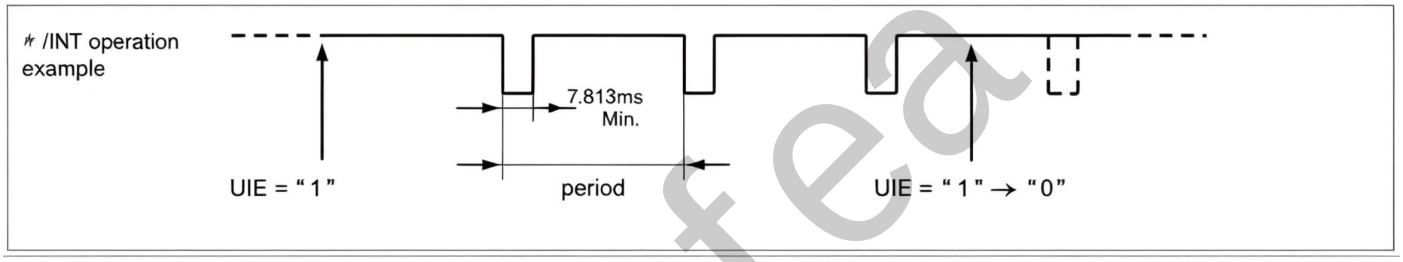
(8) As long as /INT=low, the /INT pin status does not change when the TF bit value changes from " 1" to "0".

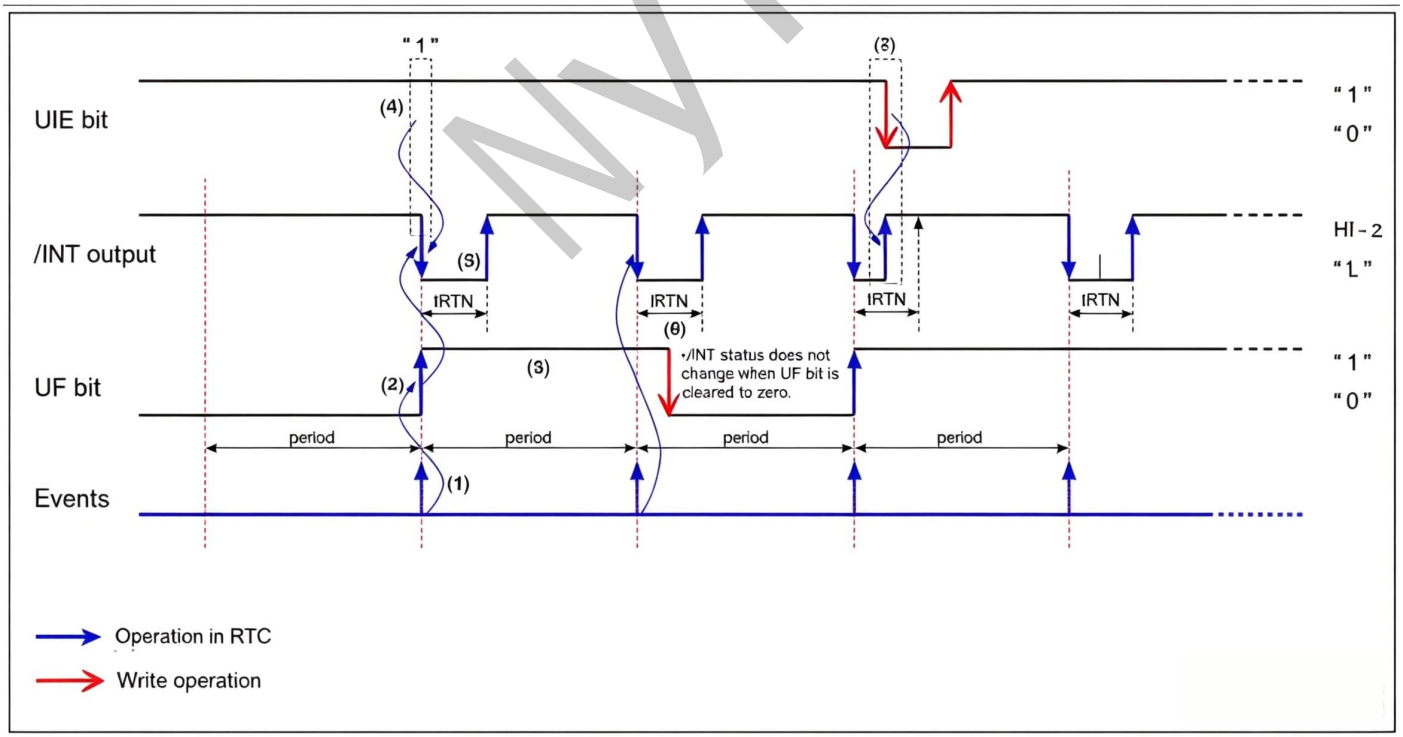
(9) When /INT= low, the /INT pin status changes from low to Hi-Z as soon as the TIE bit value changes from " 1" to "0".

14.2 Time Update Interrupt Function

The time update interrupt function produces interrupt events at one-second or one-minute intervals, synchronized with the internal clock timing.

When an interrupt event occurs, the UF bit is set to "1" and the /INT pin is driven low to indicate that an event has been generated. (However, when a fixed-cycle timer interrupt event occurs, low-level output from the /INT pin is produced only if the control register's UIE bit is "1".) The /INT status is automatically cleared (the /INT status changes from low level to Hi-Z) at the earliest 7.813 ms (a fixed value) after the interrupt occurs.





1) A time update interrupt event is triggered when the internal clock's value matches either the second update time or the minute update time. The USEL bit determines which of these two—the second update time or the minute update time—must be matched.

2) When a time update interrupt event occurs, the UF bit is set to "1."

3) Once the UF bit is "1," it remains so until it is cleared to zero.

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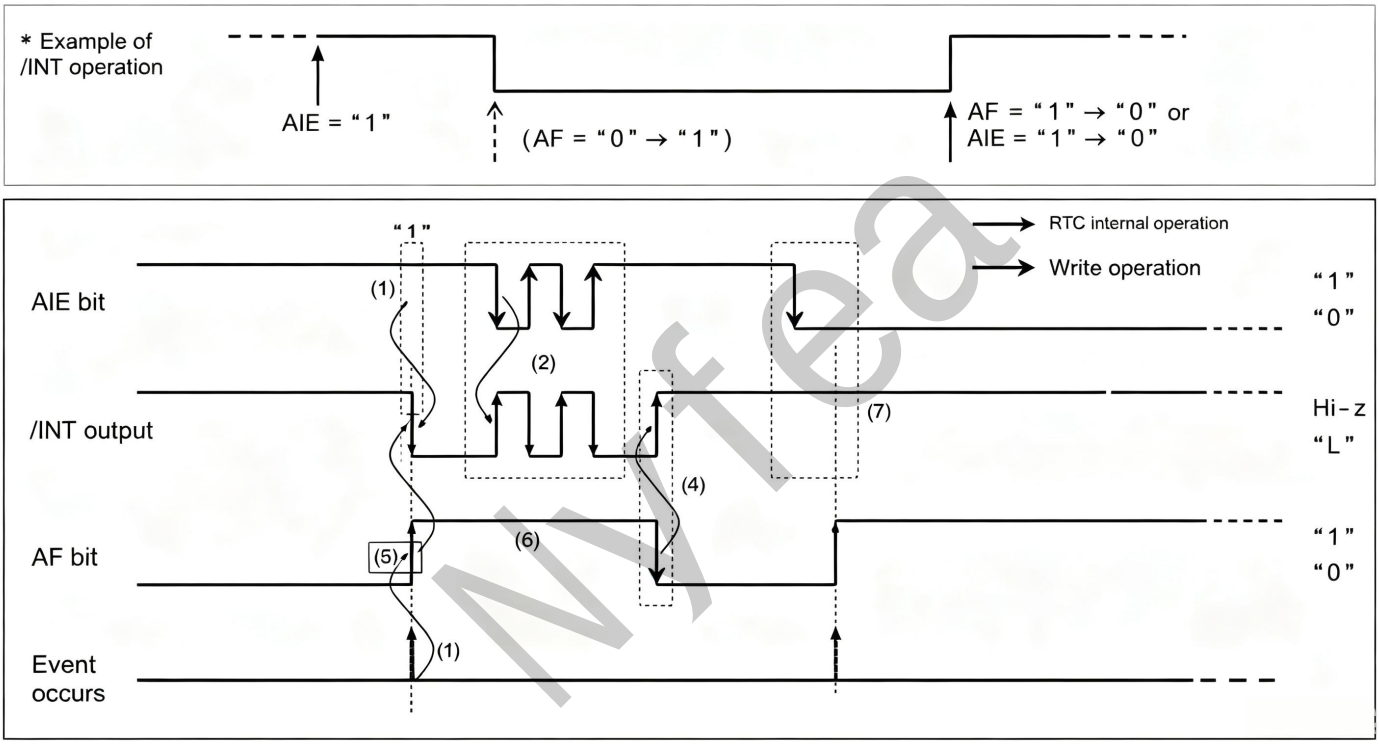
4) When a time update interrupt occurs, the /INT pin outputs low if UIE = "1."
5) If UIE = "0" when a timer update interrupt occurs, the /INT pin remains Hi-Z.
6) With each event, the /INT pin outputs low only for the duration of tRTN (which is fixed at 7.813 ms for time update interrupts), after which it is automatically cleared to Hi-Z.
7) The /INT pin output goes low again when the next interrupt event occurs.
8) While /INT is low, the /INT pin status does not change, even if the UF bit value transitions from "1" to "0."
9) While /INT is low, the /INT pin status changes from low to Hi-Z as soon as the UIE bit value transitions from "1" to "0."

14.3 Alarm Interrupt Function

The alarm interrupt generation function generates interrupt events for alarm settings such as date, day, hour, and minute settings. When an interrupt event occurs, the AF bit value is set to " 1" and the /INT pin goes to low level to indicate that an event has occurred.



(1) The minute, hour, day, and date on which an alarm interrupt event should occur must be set in advance, together with the WADA bit. (Note: Even if the current date/time is used as the setting, the alarm will not trigger until the counter reaches that date/time again—meaning the alarm will occur on the next occurrence, not immediately.)
(2) When a time update interrupt event occurs, the AF bit is set to "1."
(3) Once the AF bit = "1," it remains so until it is cleared to zero.
(4) If AIE = "1" when an alarm interrupt occurs, the /INT pin output goes low. When an alarm interrupt event occurs, the /INT pin output goes low, and this state is held until it is cleared via the AF bit or AIE bit.
(5) If the AIE value changes from "1" to "0" while /INT is low, the /INT status immediately changes from low to Hi-Z. After an alarm interrupt occurs and before the AF bit is cleared to zero, the /INT status can be controlled through the AIE bit.
(6) If the AF bit value changes from "1" to "0" while /INT is low, the /INT status immediately changes from low to Hi-Z.
(7) If the AIE bit value is "0" when an alarm interrupt occurs, the /INT pin status remains Hi-Z

13.4 The interrupt functions via /INT-pin or polling

1) How to identify events, when the interruption was occurred./INT output pin is common output terminal of interrupt events of three types (Fixed-cycle timer interrupt ,Alarm interrupt, Time update interrupt).When INT asserted to Low, the system can determine in which interruption was occurred, by confirming status of (TF,AF, UF).

2) The method of detection of interruption with not using an INT output.

1. be left open INT.
2. be clears to 0 in TIE, AIE, and UIE bits.
3. monitor the TF, AF, UF. (Polling).

13.5 Temperature compensation function

During RTC production, the individual characteristics of the built-in crystal are programmed into the RTC's non-volatile memory. The integrated temperature sensor measures the module's actual temperature and compensates the crystal oscillator's frequency using the stored compensation data. This means not only the time information is temperature-compensated, but also the FOUT signal, even when outputting 32.768 kHz. This function operates within the supply voltage range VTEM. Even if the supply voltage drops below VTEM and the VDET bit is set to "1," temperature compensation resumes once the supply voltage rises above VTEM again.

Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0F, 1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	◦	◦	RESET

CSEL1, CSEL0 bit (Compensation Interval Select 1,0)

This bit sets an interval of a temperature compensation operation.

Current consumption decreases when increasing the Compensation Interval by means CSEL1,0. CSEL1,0 is set at the time of initial power-up to ("0"," 1").

CSEL1	CSEL0	Compensation Interval
0	0	0.5s
0	1	2.0s (default)
1	0	10s
1	1	30s

13.6 Battery backup switchover function

This function incorporates a supply voltage detector that senses whether the main supply voltage "VDD" falls below a threshold (VDET3). During the voltage detection period, the built-in P-channel switch positioned between the main supply voltage pin "VDD" and the backup power supply pin "VBAT" is opened. If VDET3 < VDD, the RTC operates in Normal Mode; otherwise (VDD ≤ VDET3), it switches to Backup Mode. To measure the supply voltage applied to VDD, the P-channel switch opens once per second, and the diode prevents current from flowing from VBAT through the RTC into VDD.

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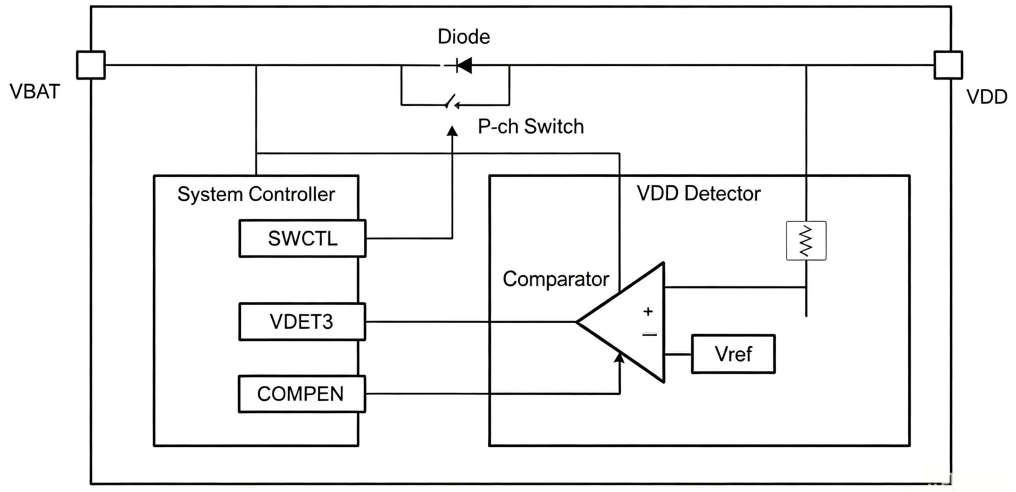

Diode (between VDD and VBAT) reference characteristic’s

Symbol	Characteristics	Condition
On-Resistance of Pch-Switch	100 ohm(typ.)	VDD = 3.0 V, Ta=25℃
V_f	0.60 V / 1 mA (typ) 0.85V / 10mA (typ)	VDD = 3.0 V, Ta=25℃
I_R	Less than 6 nA	VDD = 5.5 V , -40 to 105℃

13.7 Battery Backup related register setting

After a power-on reset, VDETOFF = 0, SWOFF = 0, BKSMP0 = 0, and BKSMP1 = 0 are loaded as the default values.

Therefore, one second after the power-on reset, the VDD voltage is detected, and the device enters either Normal Mode (VDET3 < VDD) or Backup Mode (VDD ≤ VDET3).

The duration of VDD voltage detection is governed by the BKSMP0 and BKSMP1 bits and can be configured as 2 ms, 16 ms, 128 ms, or 256 ms. The VDD voltage is measured at the end of this period, i.e., on the falling edge of the comparator ON signal.

13.8 Battery Backup switchover related register setting

VDD detector	VDETOFF	SWOFF	BKSMP1	BKSMP0	VDET3 Samplingperiod	Pch-Switch ON/OFF	Remarks
ON	0	X	0	0	2ms	2ms OFF	VDETOFF:0,BKSMP1:0, BKSMP0:0 default
			0	1	16ms	16ms OFF	
			1	0	128ms	128ms OFF	
			1	1	256ms	256ms OFF	
OFF	1	0	X	X	OFF	ON	VDD and VBAT short circuit via Pch-switch
		1	X	X	OFF	OFF	VDD connected via diode to VBAT

X = Don’t care.

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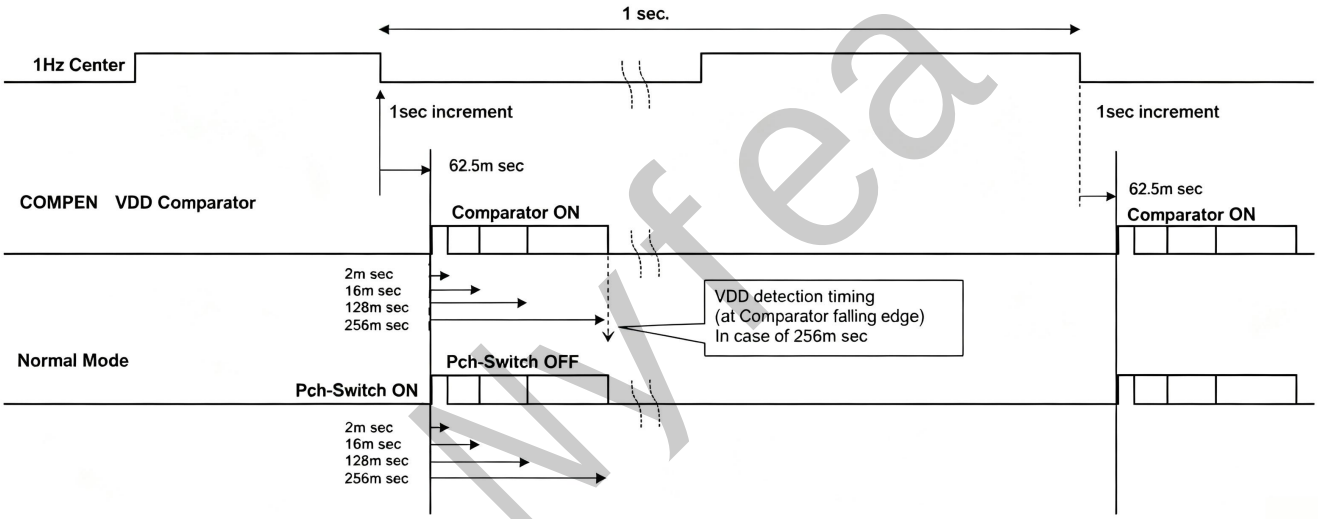
13.9 The detection period Setting

Because a VDD drop below VDET3 is detected only while the P-channel switch is open, the user should carefully configure the VDD detection period (via BKSMP0 and BKSMP1) to ensure that the VDD voltage present at the RTC's VDD pin falls below the VDET3 threshold during that window.

Term	VDD voltage detection period		Remarks
	2ms	256ms	
Current consumption (Normal Mode)	small	large	Longer detecting period increases VDD Detector current consumption .
Backup battery Charging effectiveness (Normal Mode)	Smaller detection period makes better charging effectiveness.		During detection period 、 Backup battery is charged through Diode.
Actual VDD voltage detecting period (Normal Mode)	Smaller detection period is better for slower VDD falling.	Longer detection period is better for prompt VDD falling.	



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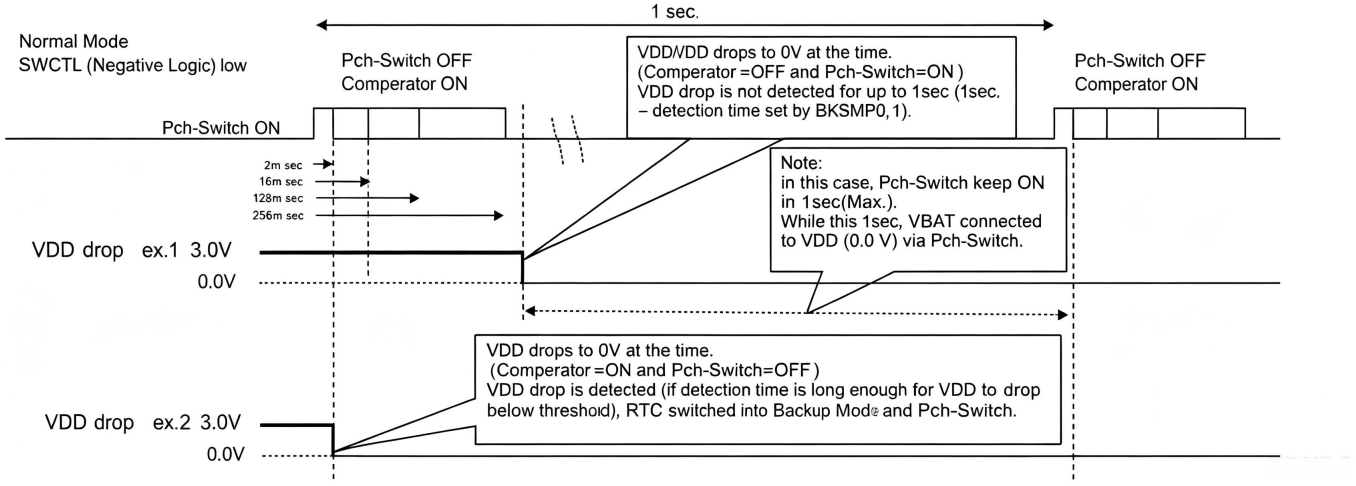
If the voltage detection period is not set long enough by means of BKSMP0 and BKSMP1, a steep VDD voltage drop might not be detected and thus the backup power supply is discharged into VDD. Between the voltage detection periods once per second, the Pch-switch is closed and thus the backup power supply discharges into VDD as well. To avoid this backup battery discharge, a diode might be set between VDD pin to power line.

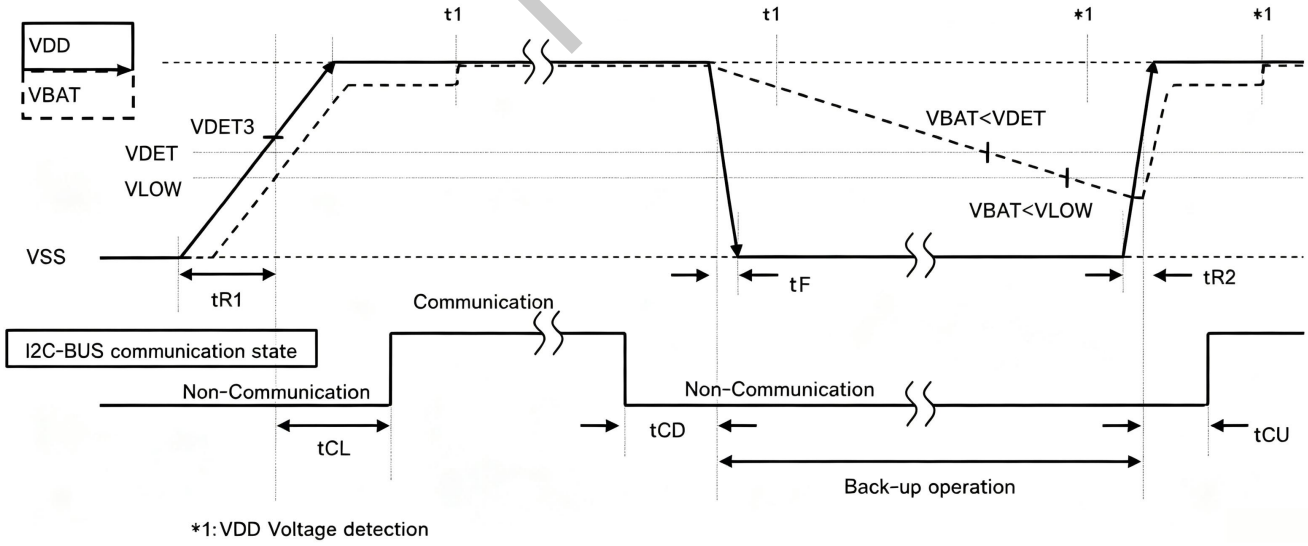


13.10 Backup and Recovery

This circuit is susceptible to power supply noise, so the supply voltage should be stabilized to prevent any adverse effect on accuracy.

tR1 is required for a proper power-on reset. If this power-on condition cannot be maintained, an initialization routine must be sent to the RTC via software. If the power supply is switched ON/OFF repeatedly within a short period, the power-on reset may become unstable. After power-OFF, keep VDD = VBAT = GND for more than 10 seconds to ensure a proper power-on reset. When the power-on reset status is uncertain, the system can initialize the RTC through software.

When a controller is shutting down, it is recommended that the CPU send a STOP condition to the RTC so that the I2C communication is left in a completed state.



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Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
VDET	Detection voltage VDET-bit threshold		1.9	1.95	2	V
VLOW	Detection voltage VLF-bit threshold		1.16		1.6	V
VDET3	Detection voltage Backup-switchover voltage		2.3	2.4	2.5	V
tR1	Power supply rise time1	VDD=VSS to 2.5V	1		10	ms/V
tCL	Access wait time (After initial power on)	After VDD=2.5V	30			ms
tCD	Access disable hold time	After stop condition	0			μs/V
tF	Power supply fall time	VDD=2.5V to VSS	2			μs/V
tR2	Power supply rise time2	VDD=VSS to 2.5V	15			μs/V
tCU	Access wait time (Normal power on)	After VDD=2.5V	0			μs

13.11 Backup return and power on initialize

Since most RTC registers are synchronized with the oscillation clock of the built-in crystal oscillator, the RTC will not operate correctly unless the integrated oscillator has stabilized.

1. First, the system should verify the status of the VLF bit.
2. If VLF is "1," the system must initialize all registers.
3. When the RTC is initially powered on, wait for tSTA (3 seconds) before setting the time and calendar. However, read access is permitted 30 ms after VDD = VCLK.

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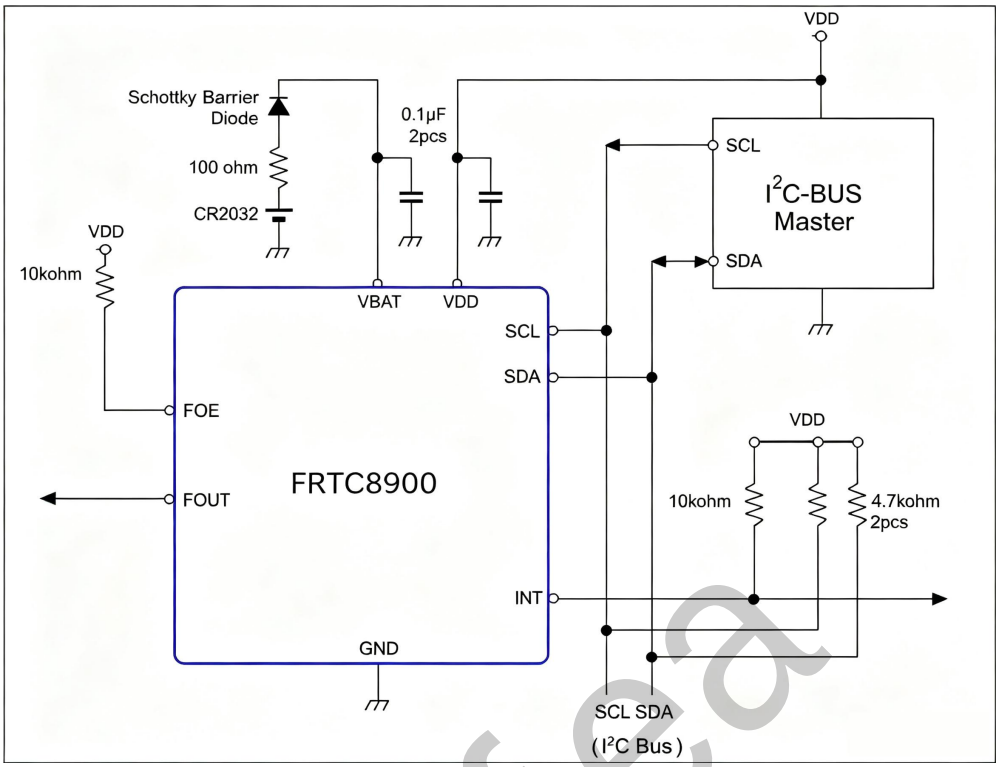
14 Application Circuit



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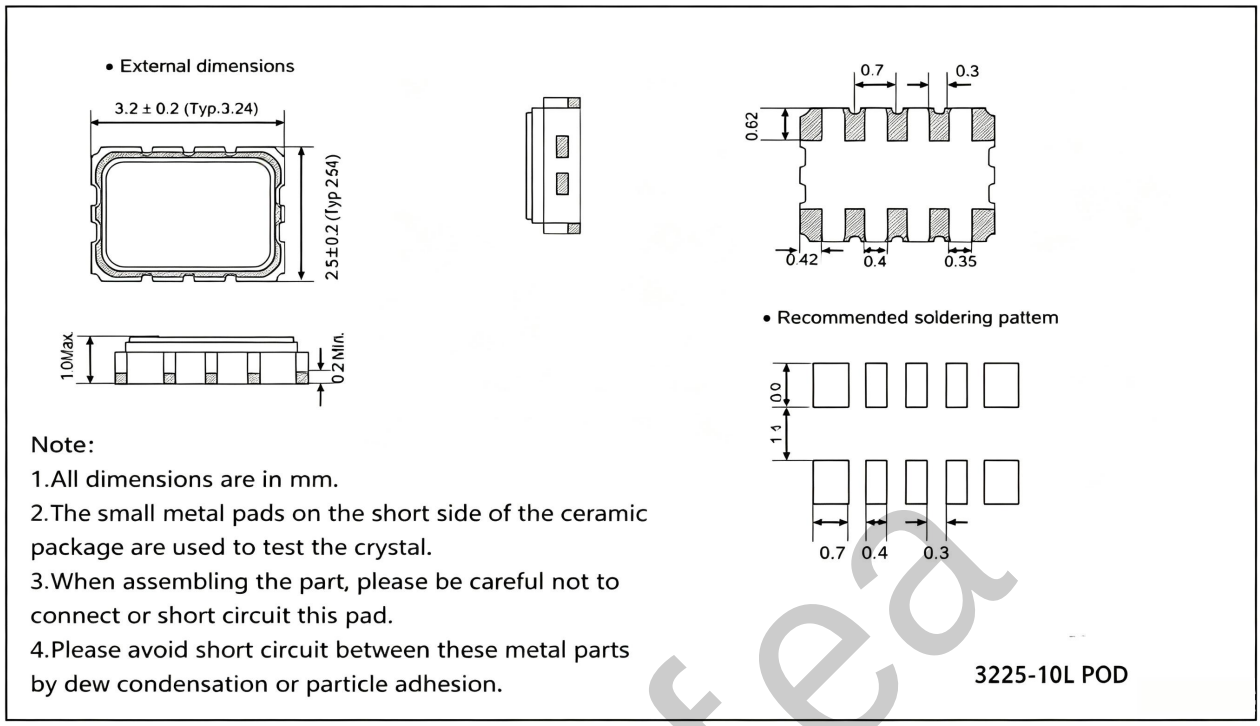
15 Package Information

15.1 FRTC8900CE 3225-10 pin Package



Note:

1.All dimensions are in mm.

2.The small metal pads on the short side of the ceramic package are used to test the crystal.

3.When assembling the part, please be careful not to connect or short circuit this pad.

4.Please avoid short circuit between these metal parts by dew condensation or particle adhesion.

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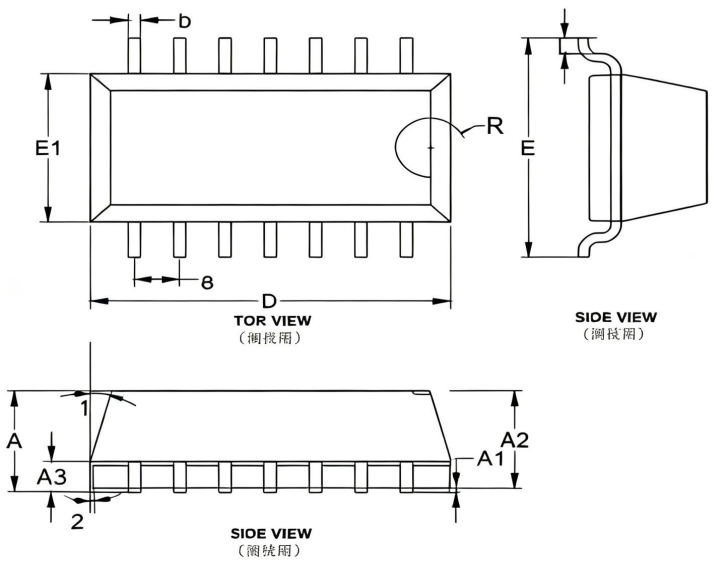
15.2 FRTC8900S SOP14 Package



Symbol	Dimensions (en)		
	Nin	TYP	Nax
A	3.000	3.300	0.500
A1	0.050	0.125	0.200
A2	3.650	3.300	3.500
A3	0.500	0.900	1.000
b	0.800	0.350	0.500
B	9.800	10.100	10.100
6	7.200	7.100	2.700
B1	4.700	3.000	3.300
e	1.22005C		
L	0.800	0.600	0.300
R	0.200	1.000	1.200
0.1	13°	13.5°	15°
02	3°	3°	7°

Note:

1. All dimentions are in mmt Angels in degrees.
2. Dimentions eaclude burrs, mold fiezh or protrutions.
3. Refer Jedec MS-012
4. Recommended land pettern is for reference only.

SOP14 POD Rev. B

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