NYFEA

www.nyfea.com

Nyfea product specification

PRODUCT SPECIFICATION

Customer : _____

Product Name : Real Time Clock

Part NO : FRTC8025S

Issue Date : _____

Nyfea

Prepared	Checked	Customer Check
ChenTT	Zelig	

NYFEA

Table Of Contents

1 Features 4

2 Block Diagram 4

3 Description 4

4 Ordering Information 4

5 Pin Configuration 5

6 Absolute Maximum Ratings 6

7 Recommended operation conditions 6

8 Frequency Characteristics 6

9 DC Electrical Characteristics 7

10 AC Characteristics - I2C Bus 8

11 Register Table 9

12 Details of Registers 10

12.1 Clock counter (SEC - HOUR) 10

12.1.1 Second counter 10

12.1.2 Minute counter 10

12.1.3 Hour counter 10

12.2 Calendar counter (WEEK - YEAR) 10

12.2.1 Day of the WEEK counter 10

12.2.2 Date counter 11

12.2.3 Month counter 11

12.2.4 Year counter 11

12.3 Alarm registers 11

12.4 Fixed-cycle timer control registers 12

12.5 Extension registers 12

12.5.1 TEST bit 12

12.5.2 WADA (Week Alarm/Day Alarm) bit 13

12.5.3 USEL (Update Interrupt Select) bit 13

12.5.4 TE (Timer Enable) bit 13

12.5.5 FSEL0, 1 (FOUT frequency Select 0 , 1) bit 13

12.5.6 TSEL0, 1 (Timer Select 0, 1) bits 13

12.6 Flag register 14

Nyfea

12.6.1 UF (Update Flag) bit 14
12.6.2 TF (Timer Flag) bit 14
12.6.3 AF (Alarm Flag) bit 14
12.6.4 VLF (Voltage Low Flag) bit 14
12.6.5 VDET (Voltage Detection Flag) bit 15
12.7 Control register 15
12.7.1 CSEL0 , 1 (Compensation interval Select 0 , 1) bits 15
12.7.2 UIE (Update Interrupt Enable) bit 15
12.7.3 TIE (Timer Interrupt Enable) bit 16
12.7.4 AIE (Alarm Interrupt Enable) bit 16
12.7.5 RESET bit 17
12.8 Temperature Data register 17
13 I2C Bus Interface 18
13.1 I2C write sequence 18
13.2 Address specification read sequence 18
13.2.1 Read sequence when address is not specified 19
13.2.2 The address auto increment in Read/Write. 19
14 Function Description 20
14.1 Fixed Cycle Timer Interrupt Function 20
14.2 Fixed-cycle Timer Interrupt Timing Chart 21
14.3 Time Update Interrupt Function 22
14.4 Alarm Interrupt Function 23
14.5 The interrupt functions via /INT or polling. 24
14.6 Temperature compensation function 24
15 Package Information 25

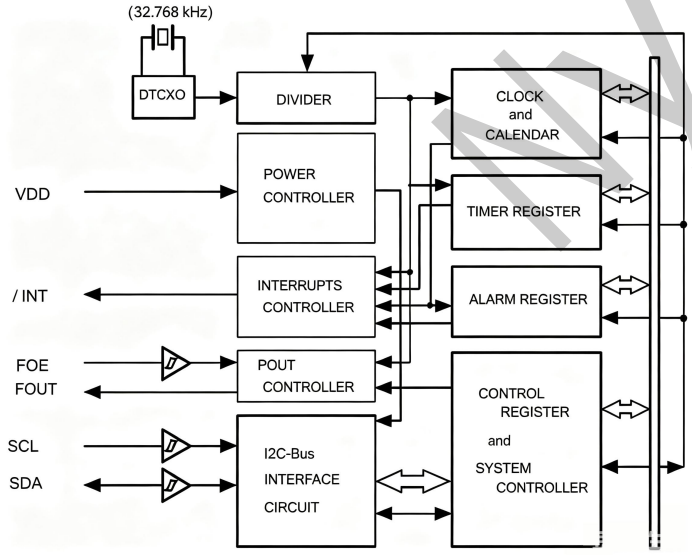
Nyfea

NYFEA

1 Features

- Built-in 32.768 kHz DTCXO
- High Stability: < ±3ppm
- Supports I2C-Bus's high-speed mode (Up to 400 kHz)
- Alarm interrupt function for day, date, hour, and minute settings
- Wakeup timer interruption
- Time update interrupt function for Seconds, minutes
- Temperature compensated 32.768 kHz output with OE function (FOE and FOUT pins)
- Auto correction of leap years (from 2000 to 2099)
- Wide interface voltage range: 1.6V ~ 5.5 V
- Low current consumption: 0.54 uA / 3 V (Typ.)
- Industry Temperature (- 40℃ ~ 85 ℃).

2 Block Diagram



3 Description

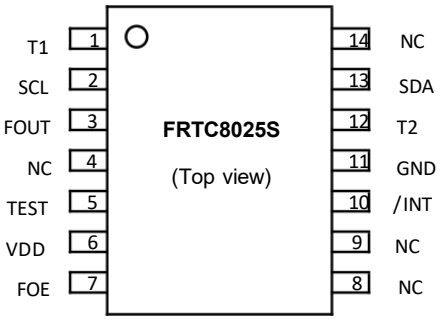
This module is an I2C bus interface-compliant real-time clock that includes a 32.768 kHz DTCXO. In addition to offering a calendar function (year, month, date, day, hour, minute, second) and a clock counter function, this module provides a wide range of additional features, including an alarm function, a wakeup timer function, a time update interrupt function, and a 32.768 kHz output function.

4 Ordering Information

Ordering Code	Package	Package Description
FRTC8025S		SOP-14 (10.1mmX7.4mm)

Nyfea

5 Pin Configuration



Pin Name	Pin No.	Type	Description
FOE	7	Input	This is an input pin used to control the output mode of the FOUT pin. When this pin's level is high, the FOUT pin is in output mode. When it is low, output via the FOUT pin is stopped.
VDD	6	Power	This pin is connected to a positive power supply.
Test	5	_	Used by the manufacturer for testing. (Do not connect externally.)
FOUT	3	Output	This is the C-MOS output pin with output control provided via the FOE pin. When FOE = "H" (high level), this pin outputs a 32.768 kHz signal. (depend on FSEL bit) When output is stopped, the FOUT pin = "Hi-Z" (high impedance).
SCL	2	Input	This is the serial clock input pin for I2C Bus communications.
T1	1	Input	Used by the manufacturer for testing. (Do not connect externally.)
SDA	13	I/O	This pin's signal is used for input and output of address, data, and ACK bits, synchronized with the serial clock used for I2C communications. Since the SDA pin is an open drain pin during output, be sure to connect a suitable pull- up resistance relative to the signal line capacity.
T2	12	Input	Used by the manufacturer for testing. (Do not connect externally.)
GND	11	Power	This pin is connected to a ground.
/INT	10	Input	This pin is used to output alarm signals, timer signals, time update signals, and other signals. This pin is an open drain pin.
N.C.	4,8,9,14	_	This pin is not connected to the internal IC. Leave N.C. pins open or connect them to GND.

Nyfea

NYFEA

6 Absolute Maximum Ratings

Symbol	Parameter	MIN	TYP	MAX	Unit
T_{store}	Storage Temperature	-55	_	+125	° C
V_{DD}	DC Supply Voltage VDD	-0.3	_	6.5	V
V_{BAT}	Battery Supply voltage	-0.3	_	6.5	V
V_I	Input Voltage on FOE, SCL, SDA	GND-0.3	_	6.5	V
V_{O1}	Output Voltage on FOUT pins	GND-0.3		VDD+0.3	V
V_{O2}	Output Voltage on SDA and /INT pins	GND-0.3		6.5	V
LU	Latch-Up			±200	mA
CDM	Charged Device Model			1000	V
HBM	Human Body Model			5000	V

Notes:

1. Applying stress levels beyond those specified in the MAXIMUM RATINGS table may result in permanent damage to the device. These values are stress limits only, and proper functional operation of the device at these or any other conditions exceeding those stated in the operational sections of this specification is not guaranteed. Prolonged exposure to absolute maximum rating conditions may degrade device reliability.

7 Recommended operation conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{DD}	Operating supply voltage (V_{DD})	1.6	3.0	5.5	V
V_{CLK}	Clock supply voltage*1	1.15	3.0	5.5	V
T_{OPR}	Operating temperature	_40	+25	+85	。C

Notes:

1. Temperature compensation ceases to function below the minimum value of VTEM. The minimum value of VCLK represents the lowest voltage required to maintain the time counting function; however, VTEM must be maintained until the oscillator has stabilized (oscillation start time tSTA).

8 Frequency Characteristics

Symbol	Parameter	Condition	TYP	Unit
△f/f	Frequency precision	Ta= 0 to +50 ℃ , V_{DD}=3.0V Ta= -40 to +85 ℃ , V_{DD}=3.0V	±1.5 ±3.0	x 10^{-6}
f/v	Frequency/voltage characteristics	Ta= +25 ℃, V_{DD} =2.0V to 5.5V	±1.0 Max.	x 10^{-6}/V
tSTA	Oscillation start time	Ta = +25 ℃ , V_{DD} = 1.6V to 5.5V	1.0 Max.	s
fa	Aging	Ta = +25 ℃, V_{DD} = 3.0V , first year	±3Max.	x 10^{-6}/year

Nyfea

NYFEA

9 DC Electrical Characteristics

Unless otherwise specified, -40 ° C≤T_A≤ 85 ° C ,

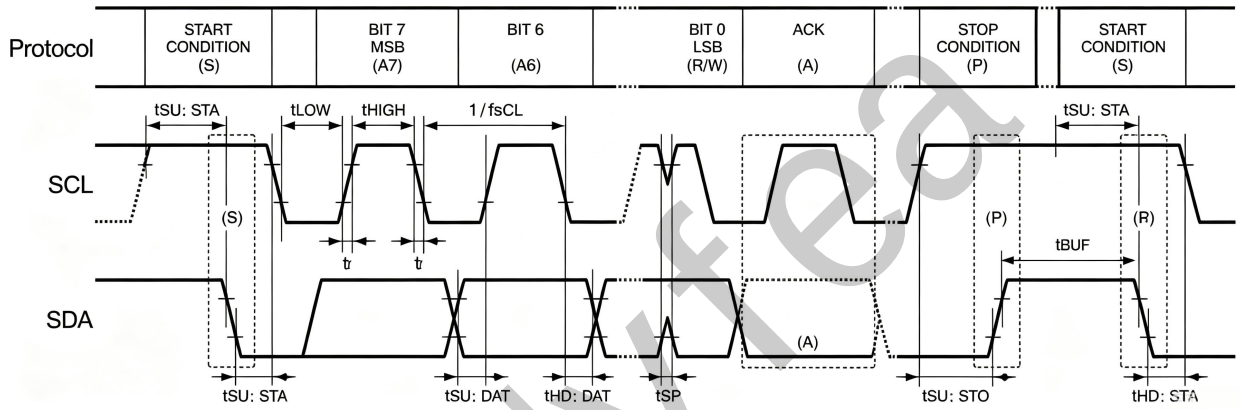
Symbol	Item	Condition		MIN	TYP	MAX	Unit
I_{DD1}	Average Current Consumption (1)	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = GND, V_{DD} = V_{BAT} FOUT: output OFF (High Z) Compensation interval 2.0 s VDET3 voltage detection time 2ms	V_{DD} = 5 V		0.59	2.4	μA
I_{DD2}	Average Current Consumption (2)		V_{DD} = 3 V		0.54	2.2	
I_{DD3}	Current Consumption (3)	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = V_{DD} , V_{DD} = V_{BAT} FOUT :32.768 kHz, CL =0pF Compensation interval 2.0 s VDET3 voltage detection time 2ms	V_{DD} = 5 V		1.66	3.4	μA
I_{DD4}	Current Consumption (4)		V_{DD} = 3 V		1.18	2.8	
V_{IH}	High-level Input voltage	SCL, SDA, FOE pins		0.8 × V_{DD}		5.5	V
V_{IL}	Low-level Input voltage	SCL, SDA, FOE pins		GND _ 0.3		0 2 × V_{DD}	V
V_{OH1}	High-level output voltage	FOUT pin	V_{DD}=5 V, I_{OH}= _1 mA	4.5		5.0	V
V_{OH2}			V_{DD}=3 V, I_{OH}=__1 mA	2.2		3.0	
V_{OH3}			V_{DD}=3 V, I_{OH}=_100 μA	2.9		3.0	
V_{OL1}	Low-level output voltage	FOUT pin	V_{DD}=5 V, I_{OL}= 1 mA	GND		GND+0.5	V
V_{OL2}			V_{DD}=3 V, I_{OL}= 1 mA	GND		GND+0.8	
V_{OL3}			V_{DD}=3 V, I_{OL}= 100 μA	GND		GND+0.1	
V_{OL4}		/ INT pin	V_{DD}=5 V, I_{OL}= 1 mA	GND		GND+0.25	V
V_{OL5}			V_{DD}=3 V, I_{OL}= 1 mA	GND		GND+0.4	
V_{OL6}		SDA pin	V_{DD} ≥2 V, I_{OL}=3 mA	GND		GND+0.4	V
I_{LK}	Input leakage current	FOE, SCL, SDA pins, V_{IN} = V_{DD} or GND		_0.5		0.5	μA
I_{OZ}	Output leakage current	/ INT, SDA, FOUT pins, V_{OUT} = V_{DD} or GND		_0.5		0.5	μA

Nyfea

10 AC Characteristics – I2C Bus

(T_A = -40° C to +85° C)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
SCL clock frequency	fSCL				400	kHz
Start condition setup time	tSU;STA		0.6			μs
Start condition hold time	tHD;STA		0.6			μs
Data setup time	tSU;DAT	Fast mode	100			ns
Data hold time	tHD;DAT		0			ns
Stop condition setup time	tSU;STO		0.6			μs
Bus idle time between start condition and stop condition	tBUF		1.3			μs
Time when SCL = "L"	tLOW		1.3			μs
Time when SCL = "H"	tHIGH		0.6			μs
Rise time for SCL and SDA	tr				0.3	μs
Fall time for SCL and SDA	tf				0.3	μs
Allowable spike time on bus	tSP				50	ns



Nyfea

NYFEA

11 Register Table

Basic Time and Calendar Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
00 or 10	SEC	○	40	20	10	8	4	2	1	R/W
01 or 11	MIN	○	40	20	10	8	4	2	1	R/W
02 or 12	HOUR	○	○	20	10	8	4	2	1	R/W
03 or 13	WEEK	○	6	5	4	3	2	1	0	R/W
04 or 14	DAY	○	○	20	10	8	4	2	1	R/W
05 or 15	MONTH	○	○	○	10	8	4	2	1	R/W
06 or 16	YEAR	80	40	20	10	8	4	2	1	R/W
07	RAM	●	●	●	●	●	●	●	●	R/W
08	MIN Alarm	AE	40	20	10	8	4	2	1	R/W
09	HOUR Alarm	AE	●	20	10	8	4	2	1	R/W
0A	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
	DAY Alarm		●	20	10	8	4	2	1	R/W
0B or 1B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0C or 1C	Timer Counter 1	●	●	●	●	2048	1024	512	256	R/W
0D or 1D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	R/W
0E or 1E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	R/W
0F or 1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET	R/W

Note:

1. After the initial power-up (from 0 V), or if the VLF bit returns "1", be sure to initialize all registers before using the RTC. Avoid entering incorrect date and time data, as clock operations are not guaranteed when the date or time data is incorrect.
2. During the initial power-up, the following are the default register settings: - Initial value_0: TEST, WADA, USEL, TE, FSEL1, FSEL0, TSEL0, UF, TF, AF, CSEL1, UIE, TIE, AIE, RESET, VDETOFF, SWOFF, BKSMP1, BKSMP0 - Initial value_1: TSEL1, VLF, VDET, CSEL0 At this point, all other register values are undefined, so be sure to perform a reset before using the module.
3. Only a "0" can be written to the UF, TF, AF, VLF, or VDET bit.
4. Any bit marked with "○" should be used with a value of "0" after initialization.
5. Any bit marked with "●" is a RAM bit that can be used to read or write any data.
6. The TEST bit is used by the manufacturer for testing. Be sure to set this bit to "0" when writing.
7. If an alarm function is not used, registers 08h - 0Ah can be used as RAM. (AIE: "0")
8. Reading the register value at addresses 0Bh - 0Ch returns pre-set data.
9. If a timer function is not used, the registers at 0Bh - 0Ch can be used as RAM. (TE, TIE: "0"))

Temperature Data register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
17	TEMP	128	64	32	16	8	4	2	1	READ

The temperature data are updated during operation of the temperature compensation circuit.

Nyfea

NYFEA

12 Details of Registers

12.1 Clock counter (SEC - HOUR)

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
00 or 10	SEC	○	40	20	10	8	4	2	1	R/W
01 or 11	MIN	○	40	20	10	8	4	2	1	R/W
02 or 12	HOUR	○	○	20	10	8	4	2	1	R/W

Note

1. ″○″ indicates write-protected bits. A zero is always read from these bits.
2. The clock counter counts seconds, minutes, and hours.
3. The data format is BCD format. For example, when the ″seconds″ register value is ″0101 1001″ it indicates 59 seconds.
4. Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

12.1.1 Second counter

The seconds counter counts from ″00″ to ″01,″ ″02,″ and so on up to 59 seconds, after which it restarts from 00 seconds.

12.1.2 Minute counter

The minutes counter counts from ″00″ to ″01,″ ″02,″ and so on up to 59 minutes, after which it restarts from 00 minutes.

12.1.3 Hour counter

The hour counter counts from ″00″ hours to ″01,″ ″02,″ and up to 23 hours, after which it starts again from 00 hours.

12.2 Calendar counter (WEEK - YEAR)

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
03 or 13	WEEK	○	6	5	4	3	2	1	0	R/W

12.2.1 Day of the WEEK counter

The day (of the week) is indicated by 7 bits, bit 0 to bit 6.
The day data values are counted as follows: Day 01h , Day 02h ,Day 04h ,Day 08h ,Day 10h ,Day 20h ,Day 01h , Day 02h , etc.

Week	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sunday	01h	0	0	0	0	0	0	0	1
Monday	02h	0	0	0	0	0	0	1	0
Tuesday	04h	0	0	0	0	0	1	0	0
Wednesday	08h	0	0	0	0	1	0	0	0
Thursday	10h	0	0	0	1	0	0	0	0
Friday	20h	0	0	1	0	0	0	0	0
Saturday	40h	0	1	0	0	0	0	0	0

Nyfea

12.2.2 Date counter

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
04 or 14	DAY	○	○	20	10	8	4	2	1	R/W

The updating of dates by the date counter varies depending on the month setting.
A leap year is designated whenever the year value is a multiple of four (such as 04, 08, 12, 88, 92, or 96). In February of a leap year, the counter counts dates from "01," "02," "03," up to "28," "29," then back to "01," and so on.

Month	Date update pattern
1, 3, 5, 7, 8, 10, or 12	1～31
4, 6, 9, or 11	1～30
February in normal year	1～28
February in leap year	1～29

12.2.3 Month counter

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
05 or 15	MONTH	○	○	○	10	8	4	2	1	R/W
06 or 16	YEAR	80	40	20	10	8	4	2	1	R/W

The month counter counts from 01 (January), 02 (February), and so on up to 12 (December), then restarts at 01 (January).

12.2.4 Year counter

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
06 or 16	YEAR	80	40	20	10	8	4	2	1	R/W

The year counter counts from 00, 01, 02, and so on up to 99, then restarts at 00.
Any year that is a multiple of four (04, 08, 12, 88, 92, 96, etc.) is treated as a leap year.

12.3 Alarm registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
08	MIN Alarm	AE	40	20	10	8	4	2	1	R/W
09	HOUR Alarm	AE	●	20	10	8	4	2	1	R/W
0A	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
	DAY Alarm		●	20	10	8	4	2	1	R/W

The alarm interrupt function works together with the AEI, AF, and WADA bits to set alarms for specified date, day, hour, and minute values.
When the settings in the alarm registers and the WADA bit match the current time, the /INT pin is driven to a low level and the AF bit is set to "1" to indicate that an alarm interrupt event has occurred.

Note:The AE bit is low-active. Therefore, to enable an interrupt once every hour when the actual minutes match the alarm setting, it is necessary to set the AE of register 08h to 0 and the AE of registers 09h and 0Ah to 1.
To generate an alarm interrupt only once a week, all three AE bits must be set to "0".

1) The alarm function is not a hardware feature but a software function inside the RTC.
2) If the "AE" bit of register 0Ah is set to "1", the day will be ignored and an interrupt will occur once the actual time matches the minutes and/or hour setting of the alarm register.

Nyfea

12.4 Fixed-cycle timer control registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0B or 1B	Timer Counter0	128	64	32	16	8	4	2	1	R/W
0C or 1C	Timer Counter1	●	●	●	●	2048	1024	512	256	R/W

Note:
These registers are used to set the preset countdown value for the fixed-cycle timer interrupt function. The TE, TF, TIE, and TSEL0/1 bits are also used to configure the fixed-cycle timer interrupt function.
When a fixed-cycle timer interrupt event occurs, the /INT pin is driven to a low level and the TF bit is set to "1".

12.5 Extension registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0B or 1B	Timer Counter0	128	64	32	16	8	4	2	1	R/W
0C or 1C	Timer Counter1	●	●	●	●	2048	1024	512	256	R/W
0D or 1D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	R/W

Note:
1) The default value is the value that is read (or is set internally) after powering up from 0 V.
2) "0" mandatory — make sure to always write 0 into this bit.
3) "-" indicates that the default value is undefined.
This register is used to specify the target for the alarm function or time update interrupt function, and to select or set operations such as fixed-cycle timer operations.

12.5.1 TEST bit

This is the manufacturer's test bit. Its value should always be "0". Be careful to avoid writing a "1" to this bit when writing to other bits.

TEST	Data	Description
Write/Read	0	Normal operation mode (Default)
	1	Setting prohibited (manufacturer's test bit)

Nyfea

12.5.2 WADA (Week Alarm/Day Alarm) bit

This bit is used to specify either WEEK or DAY as the target of the alarm interrupt function.
Writing a "1" to this bit specifies a DAY alarm, meaning the alarm interrupt is initiated regardless of the actual day when the set time is reached.
Writing a "0" to this bit specifies a WEEK alarm, so an alarm interrupt is only generated when the set time is reached on a specific day of the week.

12.5.3 USEL (Update Interrupt Select) bit

This bit is used to define whether the RTC should output a "second update" or "minute update" interrupt, allowing external clocks to be synchronized with the time registers of the RTC.

USEL	Data	update interrupts	Auto reset time tRTN
Write/Read	0	second update (Default)	500 ms
	1	minute update	Min. 7.813 ms

12.5.4 TE (Timer Enable) bit

This bit controls the start/stop setting for the fixed-cycle timer interrupt function.
Writing a "1" to this bit starts the fixed-cycle timer interrupt function (a countdown begins from a preset value).Writing a "0" to this bit stops the fixed-cycle timer interrupt function.

12.5.5 FSEL0, 1 (FOUT frequency Select 0 , 1) bit

The combination of these two bits is used to set the FOUT frequency. Note: All frequencies are temperature compensated

FSEL1	FSEL0	FOUT
0	0	32768Hz
0	1	1024Hz
1	0	1Hz
1	1	32768Hz

12.5.6 TSEL0, 1 (Timer Select 0, 1) bits

The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function (four settings are available).

TSEL1	TSEL0	Timer		Auto resettime tRT(Min.)	Effect of RESET bit
0	0	4096 Hz	Once per 244.14 μs	122 us	———
0	1	64 Hz	Once per 15.625 ms	7.813 ms	Does not operate when the RESET bit value is "1".
1	0	"Second" update	Once per second	7.813 ms	
1	1	"Minute" update	Once per minute	7.813 ms	

Nyfea

12.6 Flag register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0E or 1E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	R/W

Default is values loaded automatically after power ON from 0V.
"o" indicates write-protected bits. A zero is always read from these bits.
"-" indicates a default value is undefined.

12.6.1 UF (Update Flag) bit

If set to "0" beforehand, this flag bit's value changes from "0" to "1" when a time update interrupt event has occurred. Once this flag bit's value is "1", it is retained until a "0" is written to it.

12.6.2 TF (Timer Flag) bit

If set to "0" beforehand, this flag bit's value changes from "0" to "1" when a fixed-cycle timer interrupt event has occurred. Once this flag bit's value is "1", it is retained until a "0" is written to it.

12.6.3 AF (Alarm Flag) bit

If set to "0" beforehand, this flag bit's value changes from "0" to "1" when an alarm interrupt event has occurred. Once this flag bit's value is "1", it is retained until a "0" is written to it.

12.6.4 VLF (Voltage Low Flag) bit

VLF indicates the retained reliability of clock functions and internal data.When VLF is set to "1", it indicates the possibility that both memorized data and clock/calendar data have been lost. There are two factors that can set VLF:
1. A supply voltage drop below 1.6 V (VCLK) was detected. The VLF voltage detector is always active, with a detection speed of approximately 1 ms to 10 ms.
2. The internal crystal oscillation stopped. This detector is always active, with a detection speed of approximately 100 ms.
Once the VLF value is set to "1", it is retained until a "0" is written to it. After the initial power-on from 0 V, make sure that VLF is set to "1".

VLF	Data	Description
Write	0	The VLF bit is cleared to zero to prepare for the next status detection.
	1	Invalid (writing a 1 will be ignored)!
Read	0	No supply voltage drop occurred, so data are not compromised.
	1	Low voltage has been detected, so data loss might have occurred, and timeinformation might be compromised. All registers must be initialized. (This setting is retained until a "zero" is written to this bit.)

Nyfea

12.6.5 VDET (Voltage Detection Flag) bit

VDET indicates the retained reliability of temperature compensation.
When VDET is set to "1", it indicates the possibility that the clock stability history has been lost. The factor for VDET is a detected supply voltage drop below 1.95 V (VDET).
VDET is checked at every temperature compensation timing, with a detection speed of approximately 1 ms to 10 ms. Once the VDET value is "1", it is retained until a "0" is written to it.After powering up from 0 V, make sure to set this bit's value to "1".

VDET	Data	Description
Write	0	The VDET bit is cleared to zero to prepare for the next low voltage detection.
	1	Invalid (writing a 1 will be ignored)!
Read	0	Temperature compensation is normal.
	1	Temperature compensation has been stopped.

12.7 Control register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0F or 1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET	R/W

Notes
The default value is the value that is read (or is set internally) after powering up from 0 V.
"o" indicates write-protected bits. A zero is always read from these bits.
"-" indicates no default value has been defined.

This register is used to control interrupt event output from the /INT pin and the stop/start status of clock and calendar operations.

12.7.1 CSEL0 , 1 (Compensation interval Select 0 , 1) bits

The combination of these two bits is used to set the temperature compensation interval.

CSEL0,1	CSEL1 (bit 7)	CSEL0 (bit 6)	Compensation Interval
Write/Read	0	0	0.5 s
	0	1	2.0 s (default)
	1	0	10 s
	1	1	30 s

12.7.2 UIE (Update Interrupt Enable) bit

When a time update interrupt event is generated (when the UF bit value changes from "0" to "1"), this bit specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or not (/INT status remains Hi-Z).
When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event occurs.
When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

Nyfea

UIE	Data	Function
Write/Read	0	When a time update interrupt event occurs, an interrupt signal is notgenerated or is canceled (/INT status changes from low to Hi-Z).
	1	When a time update interrupt event occurs, an interrupt signal is generated(/INT status changes from Hi-Z to low). * When a time update interrupt event occurs, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is "1". This /INT status is automatically cleared(/INT status changes from low to Hi-Z) earliest 7.8 13 ms after the interrupt occurs.

12.7.3 TIE (Timer Interrupt Enable) bit

When a fixed-cycle timer interrupt event occurs (when the TF bit value changes from "0" to "1"), this bit specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or not (/INT status remains Hi-Z).
When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event occurs.
When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

TIE	Data	Function
Write/Read	0	When a fixed-cycle timer interrupt event occurs, an interrupt signal is notgenerated or is canceled (/INT status changes from low to Hi-Z).
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal isgenerated (/INT status changes from Hi-Z to low). * When a fixed-cycle timer interrupt event has been generated low-level output from the /INT pinoccurs only when the value of the control register's TIE bit is "1". Earliest 7.813 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi- Z).

12.7.4 AIE (Alarm Interrupt Enable) bit

When an alarm timer interrupt event occurs (when the AF bit value changes from "0" to "1"), this bit specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or not (/INT status remains Hi-Z).
When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event occurs.
When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

AIE	Data	Function
Write/Read	0	When an alarm interrupt event occurs, an interrupt signal is not generatedor is canceled (/INT status changes from low to Hi-Z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When an alarm interrupt event has been generated low-level output from the /INT pin occursonly when the value of the control register's AIE bit is "1".

Nyfea

12.7.5 RESET bit

RESET bit was prepared for the synchronized starting of time or timer. The detailed function of reset.

For example.
S is the start condition. P is the stop condition. RS is the restart condition.
S — Slave address (w) — ACK1 — 0Fh — ACK2 — 01h — ACK3 — RS — R/W access — P.
The RESET bit is set at ACK3, but RESET does not execute at that point.
After the RESET bit is set, the RESET function executes momentarily at the next P, and the RESET bit clears automatically. The RESET area of the circuit is the countdown chain of 2 Hz from 16 kHz, which is cleared.
Therefore, RESET does not affect the 32 kHz output.
The next update timing of the seconds counter after RESET falls within a range from just 1000 ms to 1000 ms - 30.5 μs. RESET affects the time update interrupt, alarm, and timer.

Note:
RESET is not released by the reception of a RE-START condition before receiving a STOP condition. Unnecessary use of RESET will be the cause of delay error of Calendar and Clock.

12.8 Temperature Data register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
17	TEMP	128	64	32	16	8	4	2	1	READ

Notes
This register can be used to read digital temperature data.
The temperature data are updated during operation of the temperature compensation circuit.
You can make a conversion to a centigrade by temperature data by calculating in the following expression. Temperature[℃] = (TEMP[7:0] * 2 - 187.19) / 3.218

Nyfea

13 I2C Bus Interface

The FRTC8025S supports the I2C protocol. The device that controls the message is called a master, while the devices controlled by the master are referred to as slaves. The bus must be controlled by a master device, which generates the serial clock (SCL), manages bus access, and produces the START and STOP conditions. The FRTC8025S operates as a slave on the I2C bus. Within the bus specifications, a standard mode (100 kHz cycle rate) and a fast mode (400 kHz cycle rate) are defined. The FRTC8025S works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

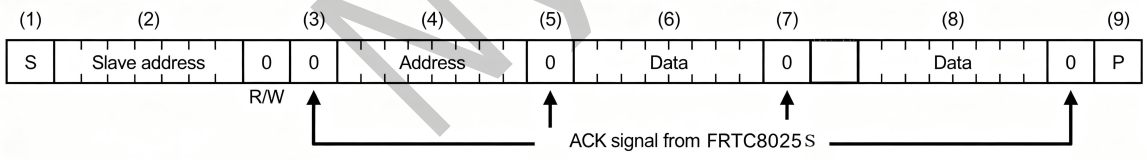
Slave addresses have a fixed length of 7 bits. This RTC's slave address is [0110010]. An R/W bit ("*" above) is appended to each 7-bit slave address during 8-bit transfers.

	Transfer Data	Slave Address							R/W bit
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	65 h	0	1	1	0	0	1	0	1= Read
Write	64 h								0 = Write

13.1 I2C write sequence

Since the FRTC8025S includes an address auto increment function, once the initial address has been specified, the FRTC8025S increments (by one byte) the receive address each time data is transferred.

1. The CPU issues a start condition [S].
2. The CPU transmits the FRTC8025S's slave address with the R/W bit set to write mode.
3. The CPU checks for an ACK signal from the FRTC8025S.
4. The CPU transmits the write address to the FRTC8025S.
5. The CPU checks for an ACK signal from the FRTC8025S.
6. The CPU transfers write data to the address specified in step (4) above.
7. The CPU checks for an ACK signal from the FRTC8025S.
8. Repeat steps (6) and (7) if necessary. Addresses are automatically incremented.
9. The CPU issues a stop condition [P].

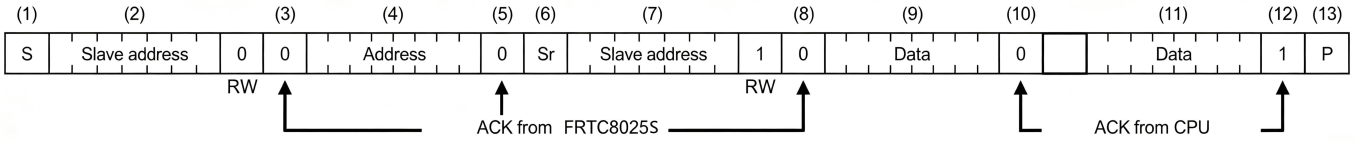


13.2 Address specification read sequence

After using write mode to set the address to be read, switch to read mode to read the actual data.

1. The CPU issues a start condition [S].
2. The CPU transmits the FRTC8025S's slave address with the R/W bit set to write mode.
3. The CPU checks for an ACK signal from the FRTC8025S.
4. The CPU transmits the address to be read from the FRTC8025S.
5. The CPU checks for an ACK signal from the FRTC8025S.
6. The CPU issues a RESTART condition [Sr] (in this case, the CPU does not issue a STOP condition [P]).
7. The CPU transmits the FRTC8025S's slave address with the R/W bit set to read mode.
8. The CPU checks for an ACK signal from the FRTC8025S (from this point on, the CPU is the receiver and the FRTC8025S is the transmitter).
9. The FRTC8025S outputs the data from the address specified in step (4) above.
10. The CPU transmits an ACK signal to the FRTC8025S.
11. Repeat steps (9) and (10) if necessary. Read addresses are automatically incremented.
12. The CPU transmits an ACK signal for "1".
13. The CPU issues a stop condition [P]..

Nyfea



13.2.1 Read sequence when address is not specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address + 1.

(1) CPU transfers start condition [S].

(2) CPU transmits the FRTC8025S's slave address with the R/W bit set to read mode.

(3) Check for ACK signal from FRTC8025S
(from this point on, the CPU is the receiver and the FRTC8025S is the transmitter).

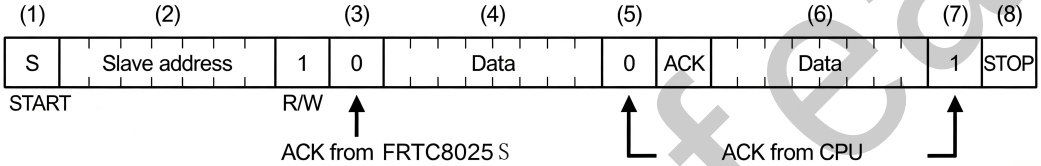
(4) Data is output from the FRTC8025S to the address following the end of the previously accessed address.

(5) CPU transfers ACK signal to FRTC8025S.

(6) Repeat (4) and (5) if necessary.
Read addresses are automatically incremented in the FRTC8025S.

(7) CPU transfers ACK signal for "1".

(8) CPU transfers stop condition [P].



13.2.2 The address auto increment in Read/Write.

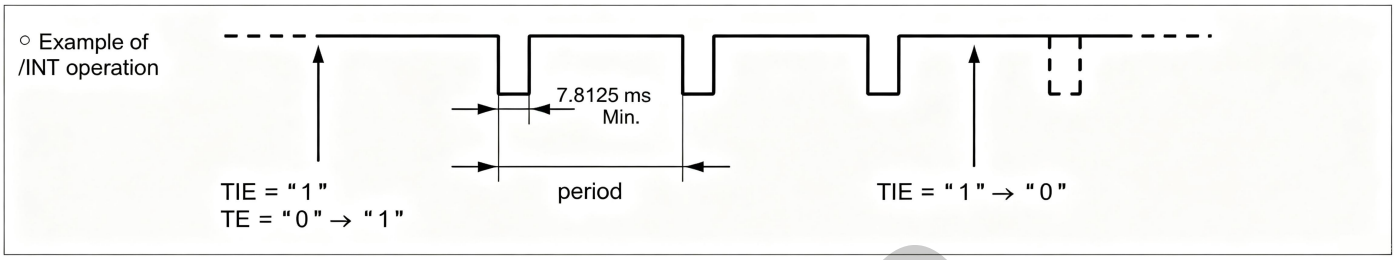
In Basic time and calendar resister.
Address : 08 - 09 - 0A - 0B - 0C - 0D - 0E - 0F - 00 -
01 - 02 - In Extension resister
Address : 18 - 19 - 1A - 1B - 1C - 1D - 1E - 1F - 10 - 11 - 12 -

Nyfea

14 Function Description

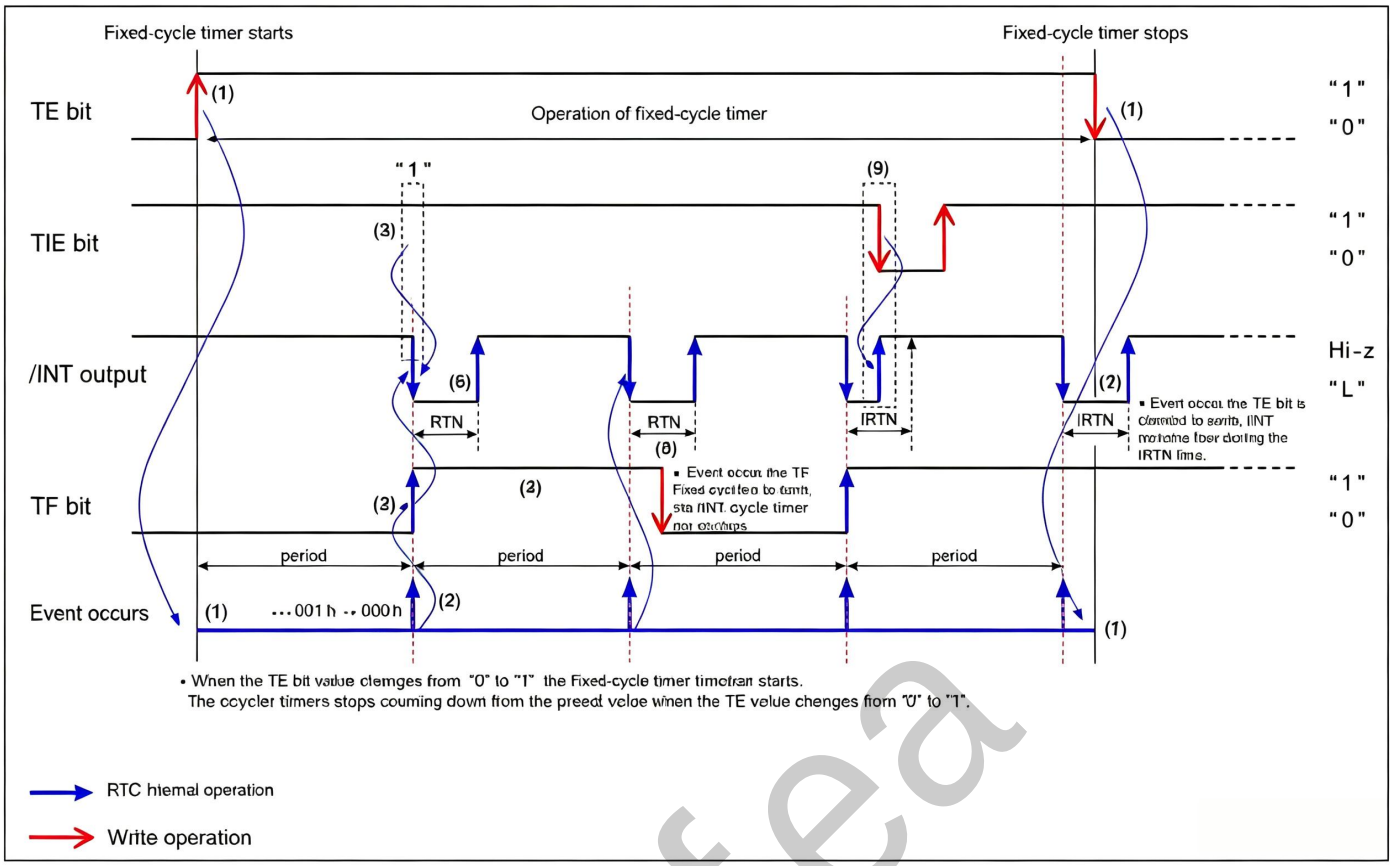
14.1 Fixed Cycle Timer Interrupt Function

This interrupt is released automatically, making it highly suitable for a wakeup timer or an interval operation system.
The fixed-cycle timer interrupt generation function produces an interrupt event periodically at any fixed cycle set between 244.14 μs and 4095 minutes.
When an interrupt event is generated, the /INT pin is driven to a low level and the TF bit is set to "1" to indicate that an event has occurred. However, when a fixed-cycle timer interrupt event is generated, low-level output from the /INT pin occurs only when the value of the control register's TIE bit is "1". At the earliest, 7.813 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low level to Hi-Z).



Nyfea

14.2 Fixed-cycle Timer Interrupt Timing Chart

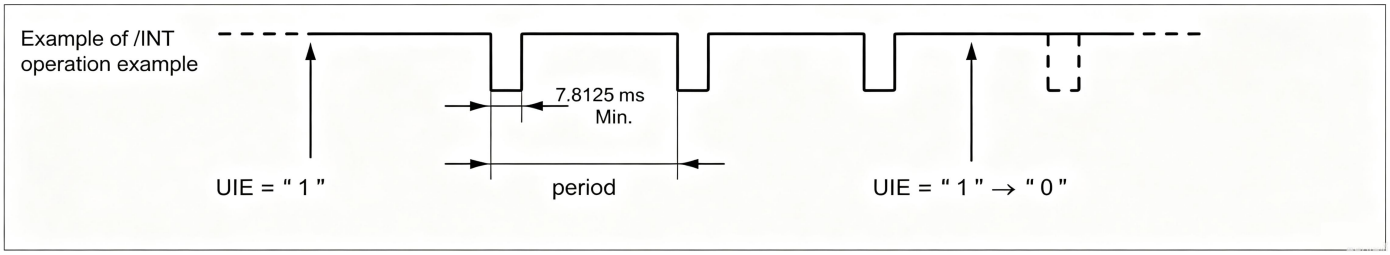


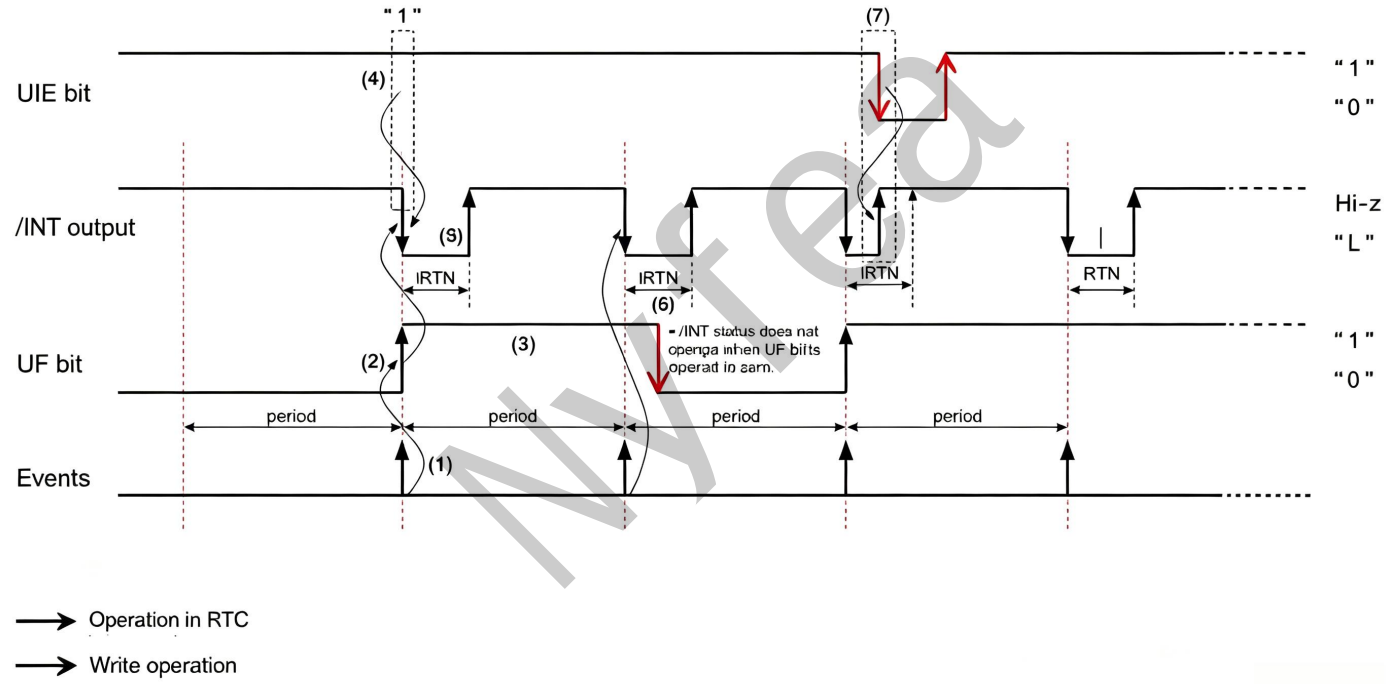
1. When a "1" is written to the TE bit, the fixed-cycle timer countdown starts from the preset value.
2. A fixed-cycle timer interrupt event initiates a countdown based on the countdown period (source clock). After the interrupt event occurs, the counter automatically reloads the preset value and begins counting down again. (Repeated operation)
3. When a fixed-cycle timer interrupt event occurs, "1" is written to the TF bit.
4. When the TF bit = "1", its value is retained until it is cleared to zero.
5. If the TIE bit = "1" when a fixed-cycle timer interrupt occurs, the /INT pin output goes low. If the TIE bit = "0" when a fixed-cycle timer interrupt occurs, the /INT pin output remains Hi-Z.
6. Output from the /INT pin remains low during the tRTN period following each event, after which it is automatically cleared to Hi-Z status. /INT is again set low when the next interrupt event occurs.
7. When a "0" is written to the TE bit, the fixed-cycle timer function stops, and the /INT pin is set to Hi-Z status. When /INT = low, the fixed-cycle timer function stops. The tRTN period is the maximum amount of time before the /INT pin status changes from low to Hi-Z.
8. As long as /INT = low, the /INT pin status does not change when the TF bit value changes from "1" to "0".
9. When /INT = low, the /INT pin status changes from low to Hi-Z as soon as the TIE bit value changes from "1" to "0".

nyfea

14.3 Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock.
When an interrupt event occurs, the UF bit value becomes "1" and the /INT pin is driven to a low level to indicate that an event has occurred. (However, when a time update interrupt event is generated, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is "1".) The /INT status is automatically cleared (/INT status changes from low level to Hi-Z) at the earliest 7.813 ms (a fixed value) after the interrupt occurs.



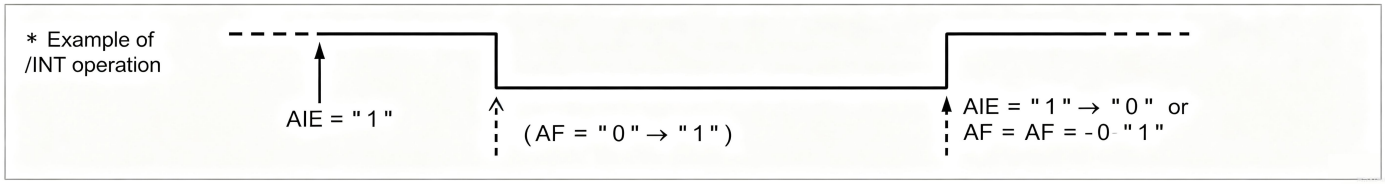


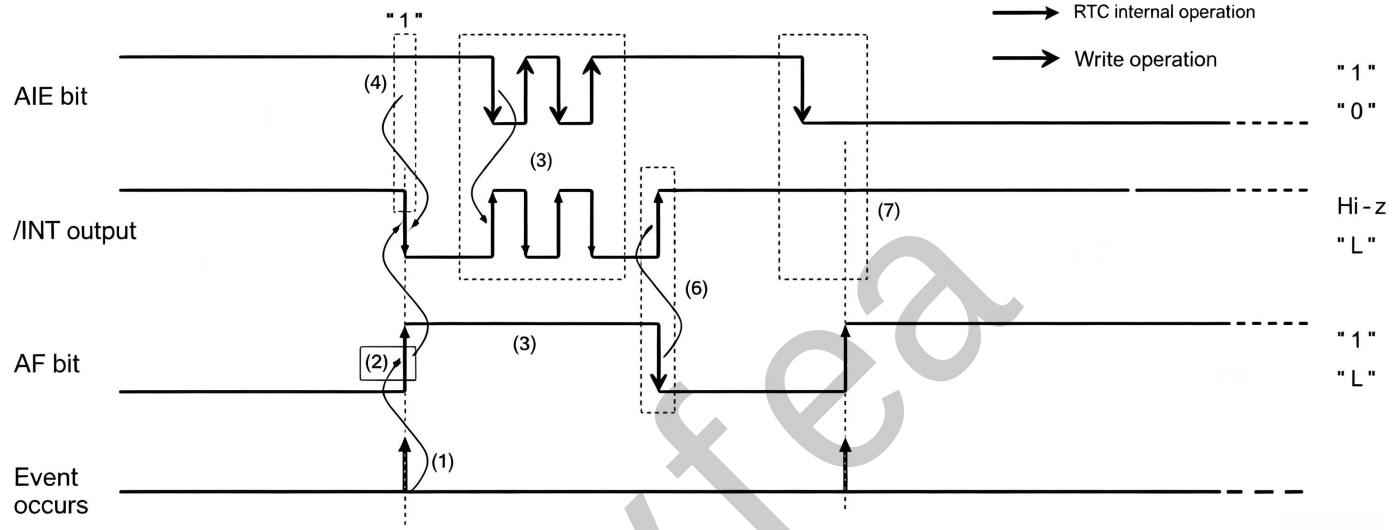
(1) A time update interrupt event occurs when the internal clock's value matches either the second update time or the minute update time. The USEL bit's specification determines whether it is the second update time or the minute update time that must be matched.
(2) When a time update interrupt event occurs, the UF bit value becomes " 1 " .
(3) When the UF bit value is " 1 " its value is retained until it is cleared to zero.
(4) When a time update interrupt occurs, / INT pin output is low if UIE =" 1 " .
If UIE = " 0 " when a timer update interrupt occurs, the / INT pin status remains Hi-Z .
(5) Each time an event occurs, / INT pin output is low only up to the tRTN time (which is fixed as 7 .8 13 ms for time update interrupts) after which it is automatically cleared to Hi-Z.
/ INT pin output goes low again when the next interrupt event occurs.
(6) As long as / INT= low, the / INT pin status does not change, even if the UF bit value changes from " 1 "to "0 " .
(7) When / INT= low, the / INT pin status changes from low to Hi-Z as soon as the UIE bit value changes from " 1 " to "0 " .

Nyrea

14.4 Alarm Interrupt Function

The alarm interrupt generation function produces interrupt events based on alarm settings such as date, day, hour, and minute values.
When an interrupt event occurs, the AF bit value is set to "1" and the /INT pin is driven to a low level to indicate that an event has occurred.





1. The minute, hour, day, and date when an alarm interrupt event is supposed to occur must be set in advance, along with the WADA bit. (Note: Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time—that is, the alarm will occur next time, not immediately.)
2. When an alarm interrupt event occurs, the AF bit value becomes "1".
3. When the AF bit = "1", its value is retained until it is cleared to zero.
4. If AIE = "1" when an alarm interrupt occurs, the /INT pin output goes low. When an alarm interrupt event occurs, the /INT pin output goes low, and this status is then held until it is cleared via the AF bit or the AIE bit.
5. If the AIE value is changed from "1" to "0" while /INT is low, the /INT status immediately changes from low to Hi-Z. After the alarm interrupt occurs and before the AF bit value is cleared to zero, the /INT status can be controlled via the AIE bit.
6. If the AF bit value is changed from "1" to "0" while /INT is low, the /INT status immediately changes from low to Hi-Z.
7. If the AIE bit value is "0" when an alarm interrupt occurs, the /INT pin status remains Hi-Z.

Nyfea

14.5 The interrupt functions via /INT or polling.

How to identify events when an interrupt occurs.
The /INT output pin is a common output terminal for three types of interrupt events (fixed-cycle timer interrupt, alarm interrupt, and time update interrupt).
When /INT is asserted to low, the system can determine which interrupt occurred by checking the status of TF, AF, and UF.
Method for detecting interrupts without using the /INT output:
1. Leave /INT open.
2. Clear the TIE, AIE, and UIE bits to 0.
3. Monitor the TF, AF, and UF bits (polling)..

14.6 Temperature compensation function

During the production process of the RTC, the individual characteristics of the built-in crystal are programmed into the RTC's non-volatile memory. The built-in temperature sensor measures the actual temperature of the module and compensates the oscillation frequency of the crystal oscillator using the stored compensation data. In this way, not only is the time information temperature-compensated, but so is the FOUT signal, even when outputting 32.768 kHz. This function operates within the supply voltage range VTEM.
Even if the supply voltage falls below VTEM and the VDET bit is set to "1", the temperature compensation operation will be performed again once the supply voltage rises above VTEM.

Address [h]	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0F,1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET

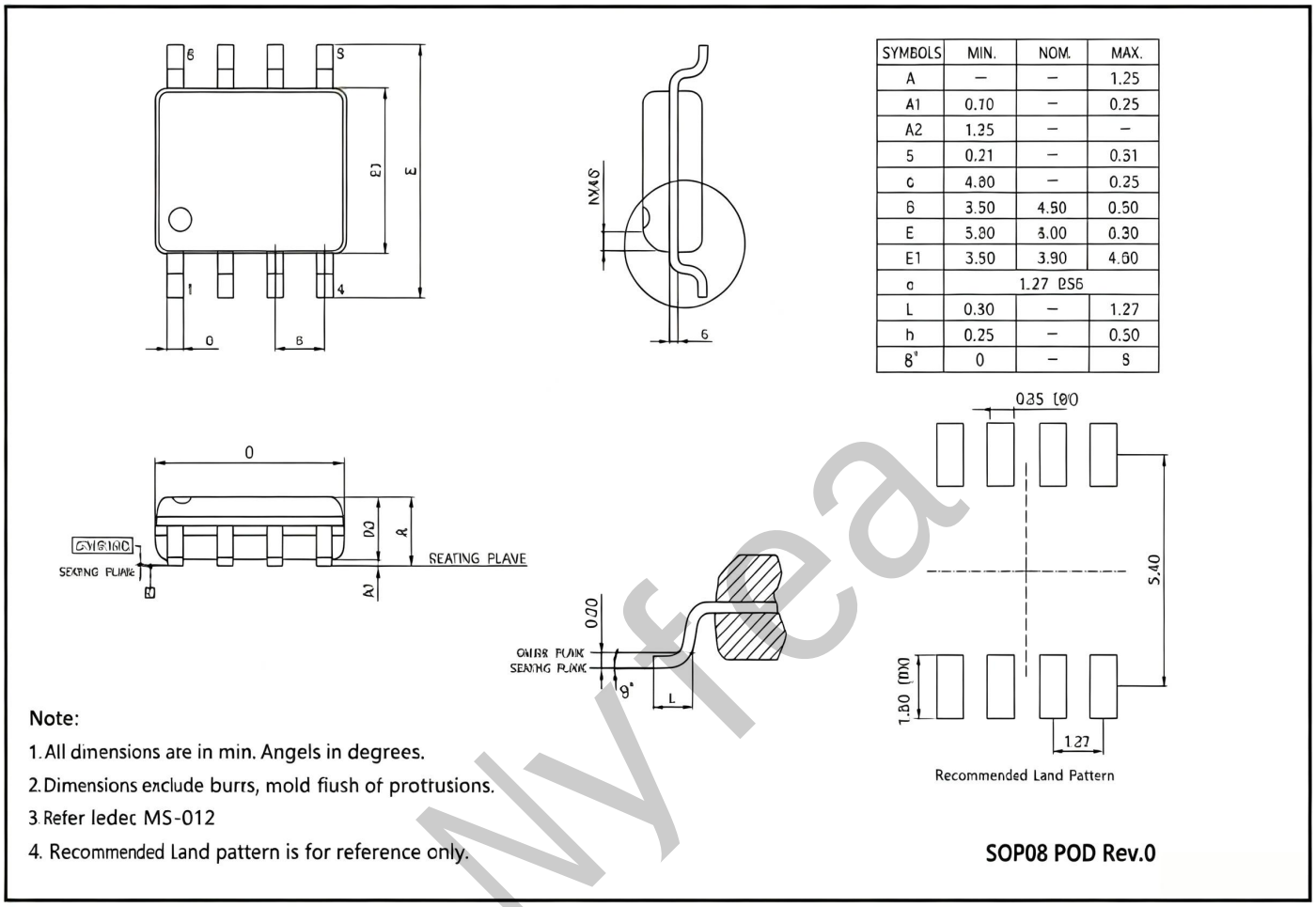
CSEL1, CSEL0 bit (Compensation Interval Select 1,0)
This bit sets an interval of a temperature compensation operation.
Current consumption decreases when increasing the Compensation Interval by means
CSEL1,0.CSEL1,0 is set at the time of initial power-up to ("0","1") .

CSEL1	CSEL0	Compensation Interval
0	0	0.5s
0	1	2.0s
1	0	10s
1	1	30s

Nyfea

15 Package Information

FRTC8025S SOP14 Package



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.25
A1	0.10	—	0.25
A2	1.25	—	—
b	0.21	—	0.31
c	4.80	—	0.25
D	3.50	4.50	0.50
E	5.80	3.00	0.30
E1	3.50	3.90	4.60
e	1.27 BSC		
L	0.30	—	1.27
h	0.25	—	0.50
θ°	0	—	8

Note:

1. All dimensions are in min. Angels in degrees.
2. Dimensions exclude burrs, mold flush of protrusions.
3. Refer Iedec MS-012
4. Recommended Land pattern is for reference only.

SOP08 POD Rev.0

Nyfea