

钍地半导体
Tudi Semiconductor

Product Specification

TUDI- UC2842/UC3842/ UC2843/UC3843 /UC2844/UC3844/UC2845/UC3845

Current Mode PWM Controller

网址 www.sztdbdt.com

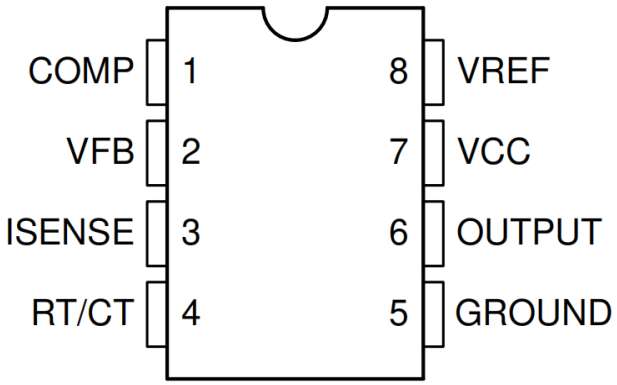
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

FEATURES

- Optimizations have been made for both offline and DC-DC converters.
- Low starting current (<1 mA)
- Automatic feedforward compensation
- Pulse current limitation
- Enhanced load response characteristics
- Under-voltage lock with hysteresis
- Double-pulse inhibition
- High-current totem column output
- Internally adjusted bandgap reference
- Operating frequency up to 500 kHz
- Error amplifier with low output resistance



SOP8 DIP8

DESCRIPTION

The UCx84x series control integrated circuits provide the necessary characteristics for implementing offline or DC/DC fixed-frequency current-mode control schemes, utilizing the minimum number of external components. The internally implemented circuits include a voltage-underoltage lockout (UVLO) featuring a start-up current below 1 mA, along with a precision reference for ensuring accuracy at the error amplifier stage. Other internal components comprise logic for latch operations, a pulse-width modulation (PWM) comparator for current-limiting control, and a totem-pole output stage designed to handle peak current surges. When the output stage is turned off, the output stage responsible for driving N-channel MOSFETs remains at a low level.

The UCx84x series offers various packaging options, temp-erature range specifications, maximum duty cycle selections, turn-on and turn-off thresholds, as well as hysteresis range choices. Devices with high turn-on or turn-off hysteresis are ideal for offline power supplies, while those with a narrow hysteresis range are designed for DC/DC applications. The UC284x series operates from – 40°C to 85°C;and the UC384x series operates from 0°C to 70°C.

APPLICATIONS

- Switching regulator with arbitrary polarity
- Transformer-coupled DC-DC converter

Table 1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	SOIC, PDIP(8)		
COMP	1	O	Error amplifier compensation pin.Connect external compensation components to this pin to modify the error amplifier output.The error amplifier is internally current-limited so the user can command zero duty cycle by externally forcing COMP to GROUND.
VFB	2	I	Inverting input to the internal error amplifier.VFB is used to control the power converter voltage-feedback loop for stability.
ISENSE	3	I	Primary-side current sense pin.Connect to current sensing resistor.The PWM uses this signal to terminate the OUTPUT switch conduction.A voltage ramp can be applied to this pin to run the device with a voltage-mode control configuration.
RT/CT	4	I/O	Fixed frequency oscillator set point.Connect timing resistor, RRT,to VREF and timing capacitor,Cc,to GROUND from this pin to set the switching frequency.For best performance,keep the timing capacitor lead to the device GROUND as short and direct as possible.If possible,use separate ground traces for the timing capacitor andall other functions.The frequency of the oscillator can be estimated with the following equations: $f_{OSC}=\frac{1.72}{R_{RT}*C_{CT}}$ (1) where fosc is in Hertz,RRT is in Ohms and CcT is in Farads. Never use a timing resistor less than 5kΩ.The frequency of the OUTPUT gate drive of the UCx842 and UCx843,fsw,is equal to fosc at up to 100%duty cycle;the frequency of the UCx844 and UCx845 is equal to half of the fosc frequency at up to 50%duty cycle.
GROUND	5	G	Analog ground.For device packages without PWRGND, GROUND functions as both power ground and analog ground .

Table 1. Pin Functions(continued)

PIN		TYPE(1)	DESCRIPTION
NAME	SOIC, PDIP(8)		
OUTPUT	6	O	OUTPUT is the gate drive for the external MOSFET.OUTPUT isthe output of the on-chip driver stage intended to directly drive a MOSFET.Peak currents of up to 1 A are sourced and sunk by this pin.OUTPUT is actively held low when VCC is below the turnon threshold.
VCC	7	I	Analog controller bias input that provides power to the device.Total VCC current is the sum of the quiescent VCC current and the average OUTPUT current.Knowing the switching frequency and the MOSFET gate charge,Qg,the average OUTPUT current can be calculated from: $I_{OUTPUT} = Q_g * f_{SW}$ (2) A bypass capacitor,typically 0.1 µF,connected directly to GROUND with minimal trace length,is required on this pin.An additional bypass capacitor at least 10 times greater than the gate capacitance of the main switching FET used in the design is also required on VCC.
VREF	8	O	5-V reference voltage.VREF is used to provide charging current to the oscillator timing capacitor through the timing resistor.Bypassing VREF to GROUND with a ceramic capacitor connected as close to the pin as possible is important for reference stability.A minimum value of 0.1- µF ceramic is required.Additional VREF bypassing is required for external loads on VREF.

(1) I = Input, O = Output, G = GND

Specifications

Absolute Maximum Rated Value

Measured within the operating temperature range under natural ventilation conditions (unless otherwise specified)(1)

		Least value	Crest value	Unit
V_{VCC}	Low-impedance source		30	V
	Ivcc<30mA	Self limitation		
Simulation input voltage for V VFB and VISENSE		-0.3	6.3	V
V_{VC}	Input voltage,only for Q and D packages		30	V
I_{OUTPUT}	Output Drive Current		±1	A
I_{COMP}	Error amplifier output drive current		10	mA
E_{OUTPUT}	Output Power(Capacitive Load)		5	μJ
T_J	junction temperature		150	℃
T_{stg}	storage temperature	-65	150	℃

(1) Operating beyond the absolute maximum rated value may cause permanent damage to the device. The absolute maximum rated value does not guarantee proper operation of the device under these conditions or under any other conditions outside the recommended operating range. If used beyond the recommended operating conditions but within the absolute maximum rated value range, the device may not function completely properly, which could affect its reliability, functionality, performance, and shorten its lifespan.

ESD Grade

		Price	Unit
$V_{(ESD)}$ Electrostatic discharge	The Human Body Discharge Model(HBM)complies with the ANSI/ESDA/JEDECJS-001standard,covering all pins(1)	±3000	V
	Charging Device Model (CDM)complies with the JEDEC specification JESD22-C101,withallpins(2)	±2000	

(1) The JEDEC document JEP155 states that 500V HBM can be safely manufactured under the standard ESD control process.
(2) The JEDEC document JEP157 states that the system can operate safely under the standard ESD control process at 250 V CDM.

Recommended Operating Conditions

Measured within the operating temperature range under natural ventilation conditions (unless otherwise specified)

		Min	TYP	Max	Unit
V_{VCC} and V_{VC}(1) Power voltage		12		28	V
V_{VFB} input voltage				2.5	V
V_{ISENSE} input voltage				1	V
I_{VCC} Power supply current,external limits				25	mA
I_{OUTPUT} Average Output Current				200	mA
I_{VREF} Reference Output Current				-20	mA
f_{OSC} oscillator frequency			100	500	kHz
T_A Working temperature rangeunder natural ventilation conditions	UC284x	-40		85	℃
	UC384x	0		70	

(1) These recommended voltage values for VC and POWER GROUND apply only to the D package

Thermal Performance Information

Thermal Index(1)		UCx84x		Unit
		D(SOIC)	P(PDIP)	
		8 pin	8 pin	
$R_{\theta JA}$	Junction to ambient thermal resist ance	117.4	74.1	℃/W
$R_{\theta JC(top)}$	Thermal resistance of the junction to the housing (top)	51.5	63.4	℃/W
$R_{\theta JB}$	Thermal resistance of the circuit board	61	50.5	℃/W
ψ_{JT}	Feature Parameters Summary(Top Section)	7.8	34.6	℃/W
Φ_{JB}	Characteristics parameters at the bottom of the graph	60.2	49.2	℃/W
$R_{\theta JC(bottom)}$	connected to the housing(bottom)thermalresistance	—	—	℃/W

Electrical Character

Measured within the operating temperature range under natural ventilation conditions (unless otherwise specified): For UC184x, it is $-55°C \leq T_A \leq 125°C$; for UC284x, it is $-40°C \leq TA \leq 85°C$; for UC384x,$0°C \leq TA \leq 70°C$; V_{VCC} = 15 V (2) ; from VCC to ground: 0.1 µF capacitor; from VREF to ground: 0.1 µF capacitor; R_{RT} = 10 kΩ;C_{CT} = 3.3 nF; T_J = TA.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE SECTION						
V_{VREF} Reference voltage	I_{VREF}=1mA,T_J=25°C	UC184x and UC284x	4.95	5	5.05	V
		UC384x	4.9	5	5.1	
Line regulation	12≤VCC≤25V			6	20	mV
Load regulation	1≤1vREF≤20 mA			6	25	mV
Temperature stability	See(1)(3)			0.2	0.4	mV/°C
Total output variation	Line,load, temperature(1)	UC184x and UC284x	4.9		5.1	V
		UC384x	4.82		5.18	
Output noise voltage	10 Hz≤fosc≤10 kHz,(1)T_J=25°C			50		µV
Long term stability	T_A=125°C,1000 Hrs(1)			5	25	mV
Output short circuit			-30	-100	-180	mA
OSCILLATOR SECTION						
fosc Initial accuracy	T_J=25°C(5)		47	52	57	kHz
Voltage stability	12≤V_{CC}≤25V			0.2%	1%	
Temperature stability	T_{MIN}≤T_A≤T_{MAX}(1)			5%		
$V_{RT/CT}$ Amplitude	Peak-to-peak(1)			1.7		V
ERROR AMPLIFIER SECTION						
V_{VFB} Input voltage	V_{COMP}=2.5V	UC184x and UC284x	2.45	2.5	2.55	V
		UC384x	2.42	2.5	2.58	
I_{VFB} Input bias current		UC184x and UC284x			-1	µA
		UC384x			-2	
A_{VOL}	2≤V_{COMP}≤4V		65	90		dB

Electrical Character(Continued)

Measured within the operating temperature range under natural ventilation conditions (unless otherwise specified): For UC184x, it is $-55°C \leq T_A \leq 125°C$; for UC284x, it is $-40°C \leq TA \leq 85°C$; for UC384x,$0°C \leq TA \leq 70°C$; V_{CC} = 15 V (2) ; from VCC to ground: 0.1 µF capacitor; from VREF to ground: 0.1 µF capacitor; R_{RT} = 10 kΩ;C_{CT} = 3.3 nF; T_J = TA.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Unity gain bandwidth	TJ=25°C(1)	0.7	1		MHz
PSRR Power supply rejection ratio	12≤V_{CC}≤25V	60	70		dB
$I_{(snk)}$ COMP sink current	V_{VFB}=2.7V,V_{COMP}=1.1V	2	6		mA
$I_{(src)}$ COMP source current	V_{VFB}=2.3V,V_{COMP}=5V	-0.5	-0.8		
V_{COMP} High High-level output voltage	V_{VFB}=2.3V,RL=15-kΩ COMP to GROUND	5	6		V
V_{COMP} Low Low-level output voltage	V_{VFB}=2.7V,RL=15-kΩ COMP to VREF		0.7	1.1	
CURRENT SENSE SECTION					
Acs Gain	See(4)(6)	2.85	3	3.15	VN
V_{ISENSE} Maximum input signal	V_{COMP}=5V(4)	0.9	1	1.1	V
PSRR Power supply rejection ratio	12V≤Vvcc≤25V(1)(4)		70		dB
I_{SENSE} Input bias current			-2	-10	µA
t_{DLY} Delay to output	V_{ISENSE} stepped from 0V to 2V(1)		150	300	ns
OUTPUT SECTION					
V_{OUT} Low Low-level OUTPUT voltage	I_{SINK}=20 mA		0.1	0.4	V
	I_{SINK}=200 mA		1.5	2.2	
V_{OUT} High High-level OUTPUT voltage	I_{SOURCE}=20 mA	13	13.5		V
	I_{SOURCE}=200 mA	12	13.5		
t_{RISE} Rise time(1)	C_{OUTPUT}=1nF,T_J=25°C		25	150	ns
t_{FALL} Fall time(1)	C_{OUTPUT}=1nF,T_J=25°C,		25	150	ns
UNDERVOLTAGE LOCKOUT(UVLO)					
V_{CCON} Enable threshold	UC2842/4	15	16	17	V
	UC3842/4	14.5	16	17.5	
	UCx843/5	7.8	8.4	9	
V_{CCOFF} UVLO off threshold	UC2842/4	9	10	11	V
	UC3842/4	8.5	10	11.5	
	UCx843/5	7	7.6	8.2	

Electrical Character(Continued)

Measured within the operating temperature range under natural ventilation conditions (unless otherwise specified): For UC184x, it is $-55°C \leq T_A \leq 125°C$; for UC284x, it is $-40°C \leq TA \leq 85°C$; for UC384x,$0°C \leq TA \leq 70°C$; V_{CC} = 15 V (2) ; from VCC to ground: 0.1 µF capacitor; from VREF to ground: 0.1 µF capacitor; R_{RT} = 10 kΩ;C_{CT} = 3.3 nF; T_J = TA.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM					
D_{MAX} Maximum duty cycle	UCx842/3	92%	97%	100 %	
	UC2844/5	46%	48%	50%	
	UC3844/5	47%	48%	50%	
D_{MIN} Minimum duty cycle				0%	
TOTAL STANDBY CURRENT					
Ivcc Start-up current			0.5	1	mA
Ivcc Operating supply current	$V_{VFB}=V_{ISENSE}=0V$		11	17	
VCC Zener voltage	Ivcc=25 mA	30	39		V

(1)Specified by design. Not production tested.
(2)Adjust VCC above the start threshold before setting at 15 V
(3)Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temp Stability} = \frac{V_{REF(max)} - V_{REF(min)}}{T_{J(max)} - T_{J(min)}}$$

$VREF_{min}$ and $VREF_{max}$ are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.

(4)Parameter measured at trip point of latch with VFB = 0 V.
(5)OUTPUT switching frequency, f_{SW}, equals the oscillator frequency, f_{OSC}, for the UCx842 and UCx843 . OUTPUT switching frequency, f_{SW}, is one half oscillator frequency, f_{OSC}, for the UCx844 and UCx845 .
(6)Gaindefinedas:$A=\Delta V_{COMP}/\Delta V_{ISENSE}$,$0V \leq V_{ISENSE} \leq 0.8V$.

Detailed Description

Overview

The UCx84x series control integrated circuits provide the necessary characteristics for implementing AC/DC or DC/DC fixed-frequency current-mode control schemes, using the minimum number of external components. The protection circuit includes under-voltage lockout (UVLO) and current limiting features. Internally implemented circuits include: a start-up current of less than 1 mA; a precision reference with fine-tuned accuracy at the error amplifier input; logic for verifying latch operations; a pulse-width modulation (PWM) comparator providing current-limiting control; and a totem-pole output stage designed to handle peak currents during pull-up or push-down transitions. When the output stage is turned off, it remains at a low level and is configured to drive N-channel MOSFETs.

The main differences among the members of these series lie in the UVLO threshold, acceptable ambient temperature range, and maximum duty cycle. The UCx842 and UCx844 devices are designed for offline AC/DC applications with a typical UVLO threshold of 16 V(on) and 10 V(off). The UCx843 and UCx845 devices are designed for regulated input voltages used in DC/DC applications, with corresponding typical thresholds of 8.4 V(on) and 7.6 V(off). The operating duty cycles of the UCx842 and UCx843 devices approach 100%.UCx844 and UCx845 achieve a duty cycle range of 0% 50% to by adding an internal switching trigger, and clear the output every clock cycle.

The specified operating temperature range for the UC284x series devices is from - 40°C to 85°C. The specified operating temperature range for the UC384x devices is from 0°C to 70° C.

Functional Block Diagram

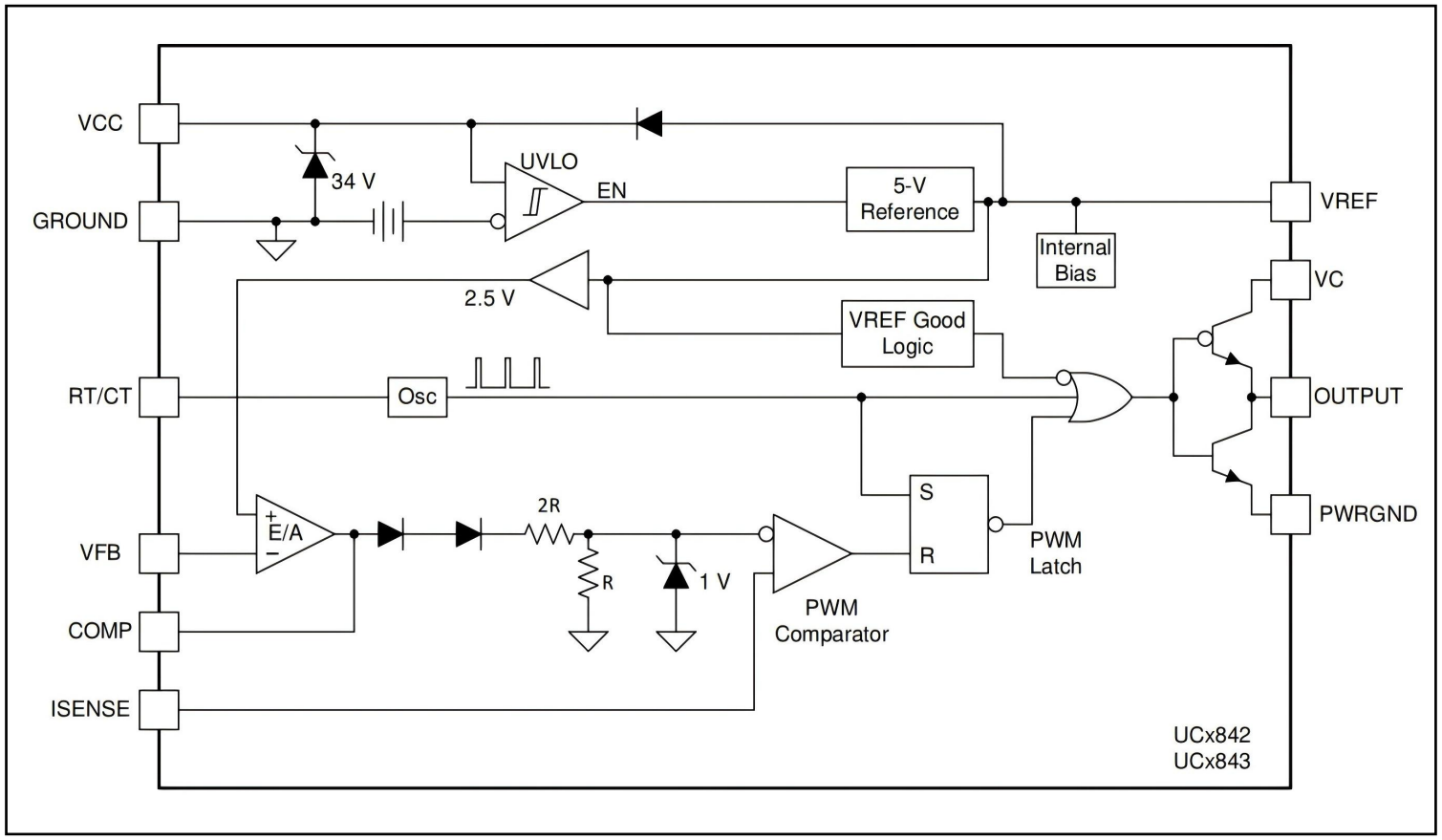


Figure 1. Block Diagrams of UCx842 and UCx843 (without Flip-Flop Triggers)

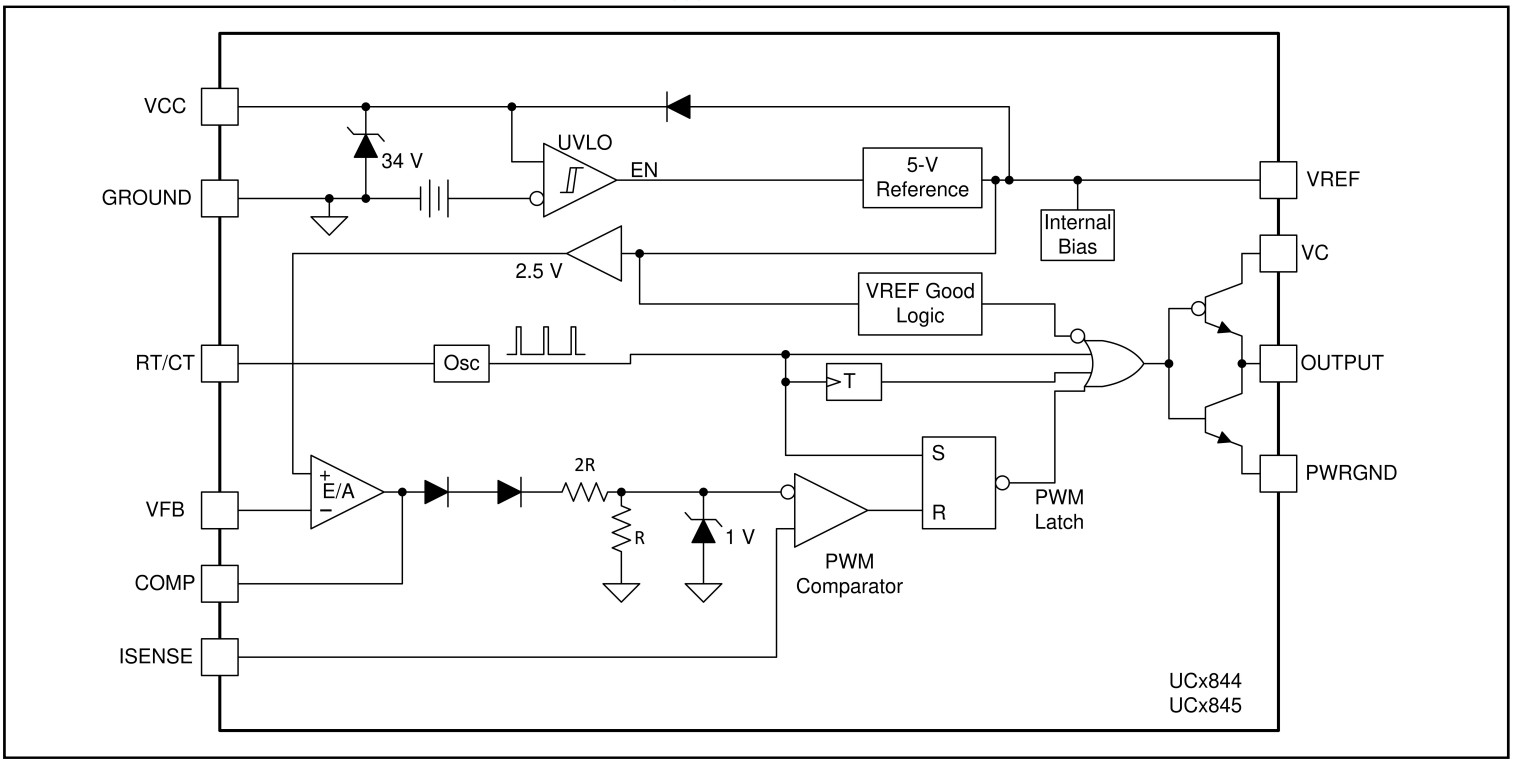


Figure 2. Block Diagrams of UCx844 and UCx845 (with Flip-Flop Triggers)

Feature Descriptio

Pin Descriptions

COMP: The error amplifier in the UCx84x product family is an open-collector configuration shunted by a current source, with a unity-gain bandwidth of 1 MHz. The COMP pin can both source and sink current. The error amplifier is internally current-limited; therefore, forcing the COMP pin to GROUND externally can be used to set the duty cycle to zero.

VFB:VFB is the inverting input of the error amplifier. It is used to control the voltage feedback loop of the power converter to ensure stability. For optimal stability, keep the VFB trace length as short as possible and minimize stray capacitance at the VFB pin.

ISENSE: The UCx84x current-sense input connects to the PWM comparator. Connect ISENSE to the MOSFET source current-sense resistor. The PWM uses this signal to terminate the conduction of the OUTPUTswitch. A voltage ramp can be applied to this pin to operate the device in a voltage-mode control configuration or to add slope compensation. An RC current-sense filter may be required to prevent false triggering due to leading-edge noise. The current-sense amplifier typically has a gain of 3 V/V.

RT/CT:RT/CT is the oscillator timing pin. For fixed frequency operation, set the timing capacitor charging current by connecting a resistor from VREF to RT/CT. Set the frequency by connecting timing capacitor from RT/CT to GROUND. For the best performance, keep the timing capacitor lead to GROUND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

The UCx84x ' s oscillator allows for operation to 500 kHz. The device uses an external resistor to set the charging current for the external capacitor, which determines the oscillator frequency . The recommended range of timing resistor values is between 5 kΩ and 100 kΩ; the recommended range of timing capacitor values is between 1 nF and 100 nF.

$$f_{OSC}=\frac{1.72}{R_{RT}\times C_{CT}} \quad (3)$$

In this equation, the switching frequency, f_{SW} is in Hz, R_{RT} is in Ω, and C_{CT} is in Farads.

GROUND:GROUND is the signal and power return path. TI recommends separating the signal return path from the high-current gate driver path to prevent the signal from being affected by switching currents.

OUTPUT: The high-current bipolar totem-pole output of the UCx84x devices can source or sink peak currents up to 1 A. The OUTPUT pin can directly drive a MOSFET. For the UCx842 and UCx843 devices, the OUTPUT switching frequency is the same as the oscillator frequency, and they can operate at duty cycles approaching 100%. In the UCx844 and UCx845 devices, an internal T flip-flop divides the oscillator frequency by two, resulting in an OUTPUT switching frequency that is half of the oscillator frequency. This limits the maximum duty cycle in the UCx844 and UCx845 to less than 50%. A Schottky diode may be required on the OUTPUT pin to prevent overshoot and undershoot caused by high impedance on the power rail and ground, respectively. A bleeder resistor placed between the MOSFET gate and source can be used to prevent the power switch from being activated by additional leakage current during undervoltage lockout (UVLO). When VCC exceeds the gate voltage rating, external clamping circuitry may be required to prevent overvoltage stress on the MOSFET gate.

VCC:VCC is the power supply input connection for the device. During normal operation, VCC is powered through a current-limiting resistor. Although the static VCC current is only 0.5 mA, the total supply current is higher and depends on the OUTPUT current. The total VCC current is the sum of the static VCC current and the average OUTPUT current. Given the operating frequency and the MOSFET gate charge (Q g), the average OUTPUT current can be calculated using Equation 4.

$$I_{OUTPUT} = Q_g * f_{SW} \quad (4)$$

The typical value of the VCC power voltage clamping for UCx84x is 34 V, but the absolute maximum value of VCC supplied from a low-impedance source is 30 V. For applications where the input voltage exceeds the recommended VCC voltage, connect a resistor in series with VCC to increase the source impedance. The maximum value of this resistor can be calculated using Equation 5.

$$R_{VCC(max)} = \frac{V_{IN\ (min)} - V_{CC(max)}}{I_{VCC} + (Q_g * f_{SW})} \quad (5)$$

In Equation 5, $V_{IN(min)}$ is the minimum voltage that is used to supply VCC, $V_{VCC(max)}$ is the maximum VCC clamp voltage and I_{VCC} is the IC supply current without considering the gate driver current and Q_g is the external power MOSFET gate charge and f_{SW} is the switching frequency. The turn-on and turn-off thresholds vary significantly across the UCx84x product family: for the UCx842 and UCx844, they are 16 V and 10 V, respectively; for the UCx843 and UCx845, they are 8.4V and 7.6 V, respectively. To avoid noise-related issues, filter VCC using an electrolytic capacitor and bypass it to ground with a ceramic capacitor. Keep the capacitors close to the IC pins.

VREF:VREF is the voltage reference for the error amplifier as well as for many other internal circuits within the IC. High-speed switching logic uses VREF as its logic supply. The 5-V reference in the UCx84x product family has a tolerance of ±2%, and the output short-circuit current is 30 mA. To ensure reference stability and prevent noise issues caused by high-speed switching transients, bypass VREF to ground using a ceramic capacitor located close to the IC package. A minimum of 0.1 µF ceramic capacitance is required. External loads on the reference require additional VREF bypassing; electrolytic capacitors may be used in addition to ceramic capacitors. When VCC is greater than 1 V but below the UVLO threshold, a 5-kΩ resistor pulls VREF to ground. VREF can be used as a logic output to indicate the status of the power system, as it remains low when VCC is below the UVLO threshold.

Cycle-by-Cycle Current Limiting: The current-mode control scheme inherently provides cycle-by-cycle current limiting. The peak current limit is established simply by clamping the error voltage. Precise current limiting allows for the optimization of magnetic and power semiconductor components while ensuring reliable power supply operation.

Current Sensing: An external series resistor, RCS , senses the current and converts it into a voltage, which serves as the input to the ISENSE pin. The ISENSE pin is the non-inverting input of the PWM comparator. The ISENSE input is compared against a signal proportional to the error amplifier output voltage; the current-sense amplifier typically has a gain of 3 V/V. The peak ISENSE current is determined by Equation 6:

$$I_{SENSE} = \frac{V_{ISENSE}}{R_{CS}} \quad (6)$$

The typical value of VISENSE is 1 V. A small RC filter (RCSF and CCSF) may be required to suppress switching transients caused by reverse recovery of the secondaryside diode, equivalent capacitive loads, or parasitic circuit impedance. The time constant of this filter can besignificantly smaller than the converter's switching cycle.

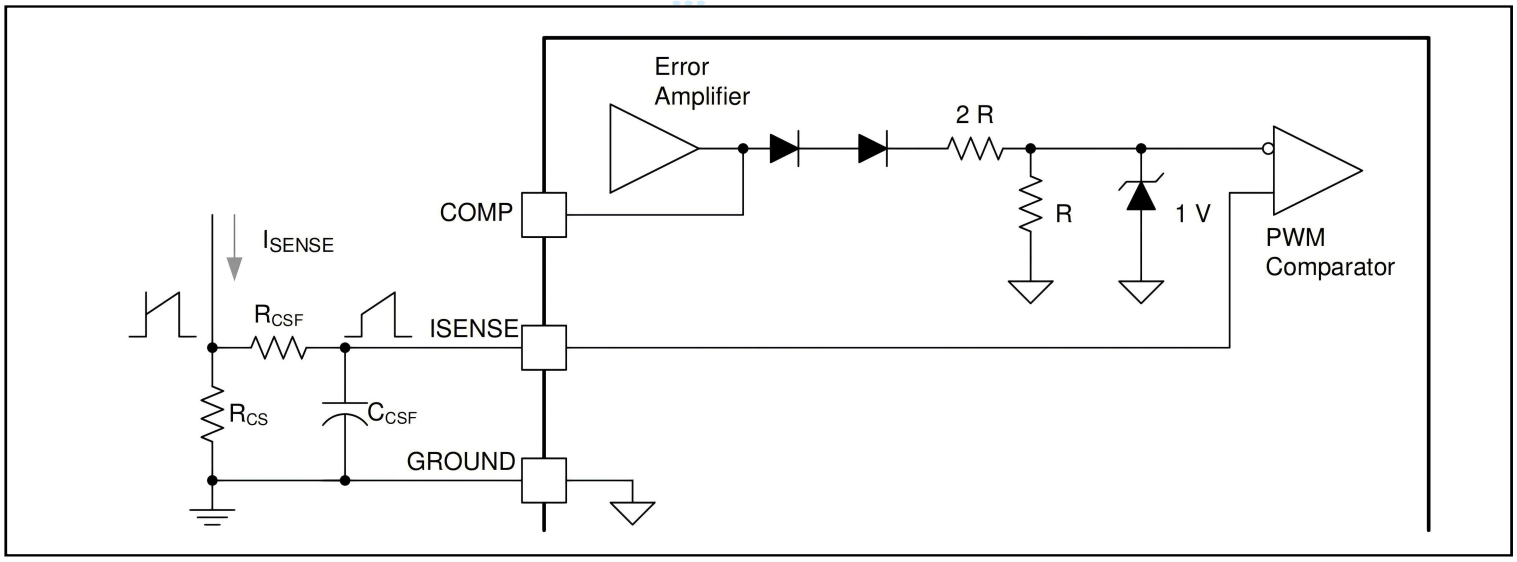


Figure 3. Schematic Diagram of the Current Detection Circuit

Error Amplifier With Low Output Resistance: The error amplifier output serves as an open-circuit collector connected in parallel with the current source. Due to its low output resistance, the compensation pin input for the error amplifier feedback can utilize various impedance networks . The error amplifier output COMP is commonly employed as a control port for secondary-side regulation by incorporating an external adjustable regulator (e.g.,TL431), enabling the transmission of error signals across the isolation boundary between the secondary and primary sides via an optical isolator; in this configuration, the COMP pin is directly connected to the optical isolator feedback. On the primary side, the inverting input VFB of the UCx48x error amplifier must be connected to GROUND. When VFB is connected to GROUND, the error amplifier output COMP is forced to emain at a high level, drawing a current typically of 0.8 mA. The optical isolator must overcome the source current capability to maintain the COMP pin voltage below the error amplifier's high-level output VOH.

For primary-side regulation, the inverting input of the error amplifier VFB is connected to a resistor divider configuration to provide a signal proportional to the regulated converter output voltage. A voltage loop compensation element is added between VFB and COMP. The internal non-inverting input of the error amplifier is set to 2.5 V. For optimal stability, the lead length of VFB should be kept as short as possible, and the stray capacitance on VFB should be minimized. The internal resistor dividers on COMP maintain a R:2R ratio, and the specific values of these internal resistors are not critical in any application.

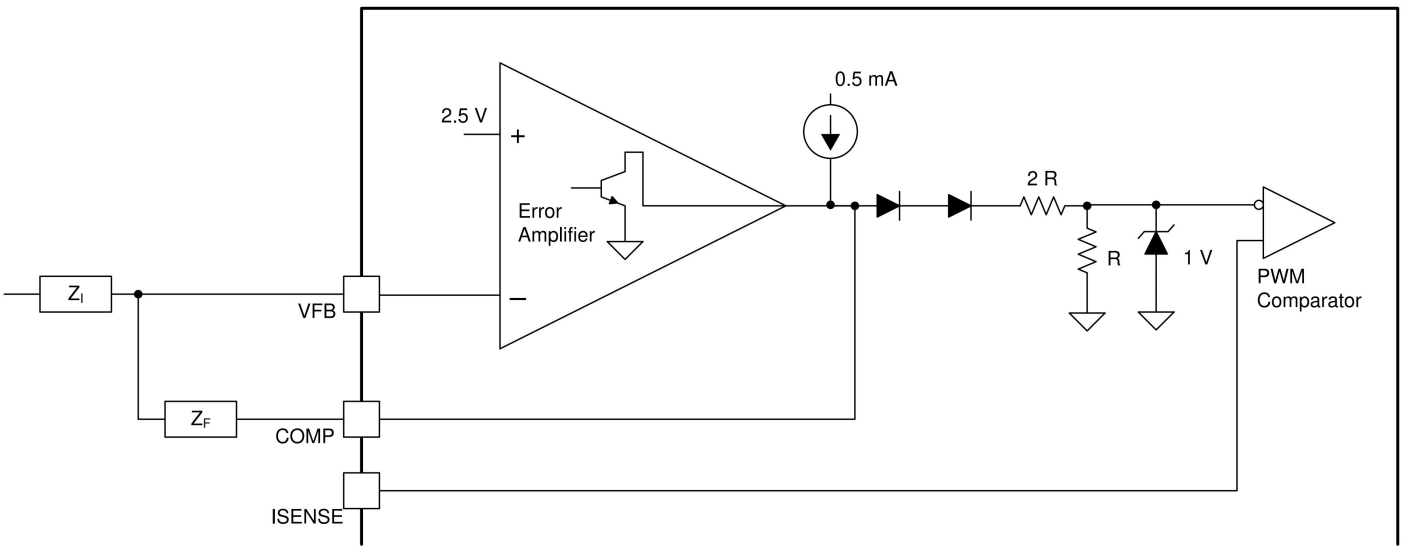
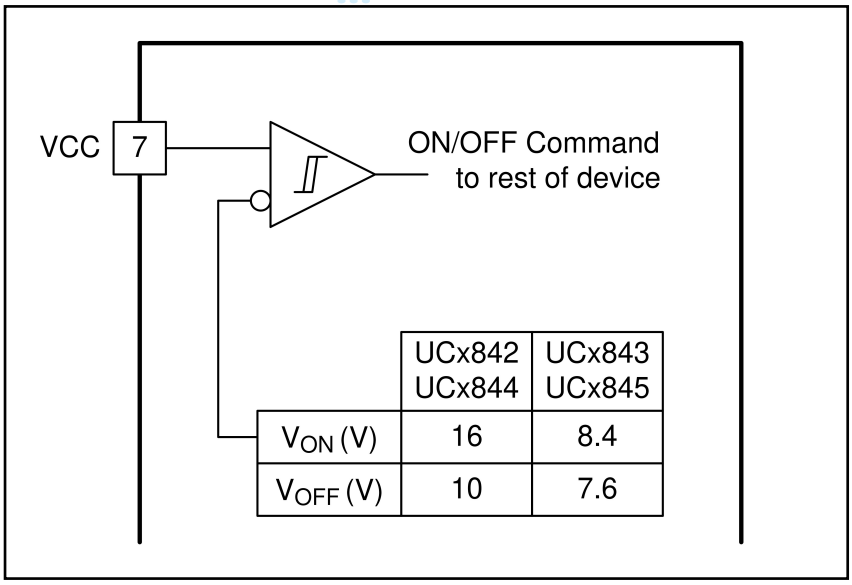


Figure 4. Schematic Diagram of Error Amplifier Configuration

Undervoltage Lockout

The UCx84x devices feature undervoltage lockout protection circuits for controlled operation during power-up and power-down sequences. The UVLO circuit insures that VCC is adequate to make the UCx84x fully operational before enabling the output stage. Undervoltage lockout thresholds for the UCx842, UCx843, UCx844, and UCx845 devices are optimized for two groups of applications: off-line power supplies and DC-DC converters. The 6-V hysteresis in the UCx842 and UCx844 devices prevents VCC oscillations during power sequencing. This wider $V_{CC_{ON}}$ to $V_{CC_{OFF}}$ range, make these devices ideally suited to off-line AC input applications. The UCx843 and UCx845 controllers have a much narrower $V_{CC_{ON}}$ to $V_{CC_{OFF}}$ hysteresis and can be used in DC to DC applications where the input is considered regulated.

Start-up current is less than 1 mA for efficient bootstrapping from the rectified input of an off-line converter, as illustrated by Figure 7. During normal circuit operation, VCC is developed from auxiliary winding N_A with D_{BIAS} and C_{VCC}. At start-up, however, C_{VCC} must be charged to 16 V through R_{START}. With a start-up current of 1 mA, R_{START} can be as large as 100 kΩ and still charge C_{VCC} when V_{AC} = 90 V RMS (low line). Power dissipation in R_{START} is then be less than 350 mW even under high line (V_{AC}= 130 V RMS) conditions.



	UCx842 UCx844	UCx843 UCx845
V_{ON} (V)	16	8.4
V_{OFF} (V)	10	7.6

Figure 5. UVLO Threshold

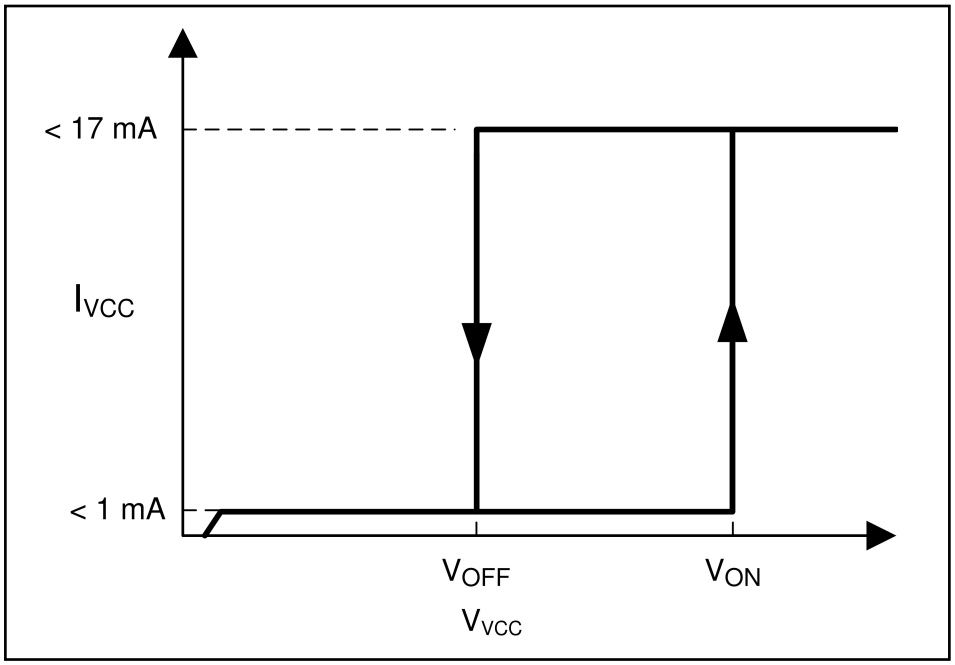


Figure 6. UVLO ON and OFF Profile

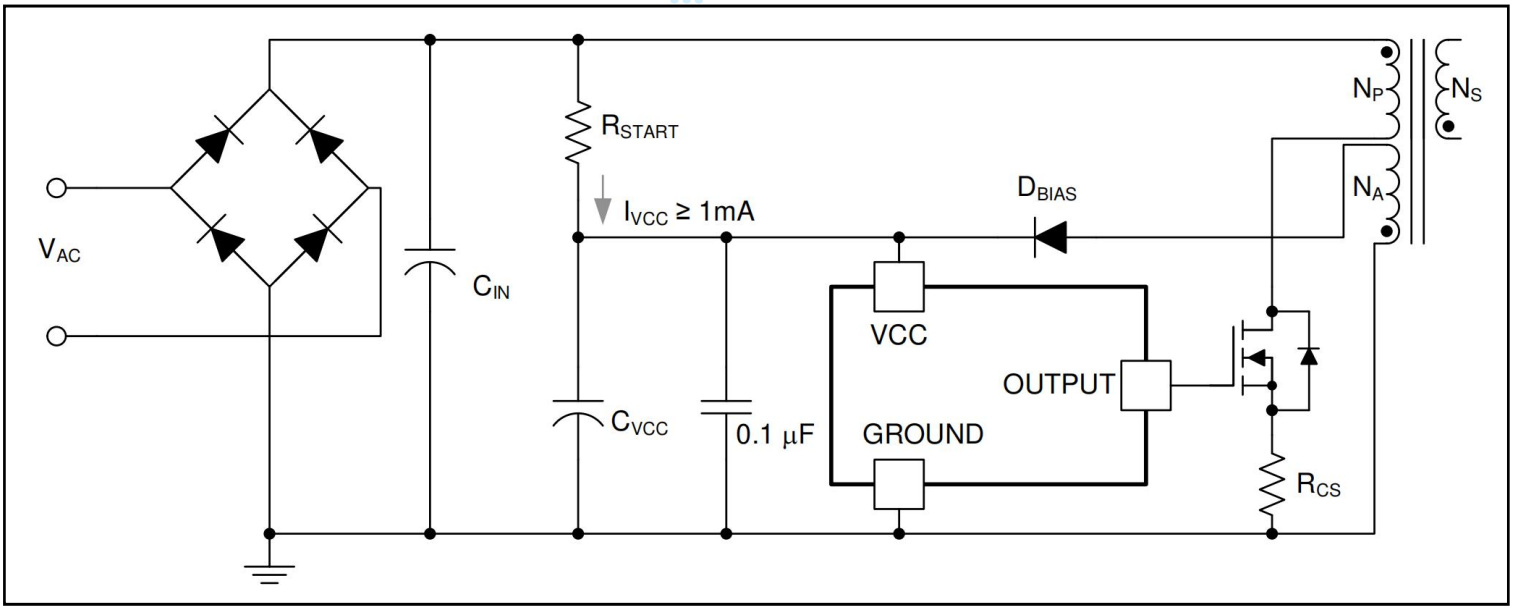


Figure 7. Powering the UCx84x

Oscillator: The oscillator allows for up to 500-kHz switching frequency. The OUTPUT gate drive is the same frequency as the oscillator in the UCx842 and UCx843 devices and can operate near 100% duty cycle. In the UCx844 and UCx845 devices, the frequency of OUTPUT is one-half that of the oscillator due to an internal T flipflop that blanks the output off every other clock cycle, resulting in a maximum duty cycle for these devices of < 50% of the switching frequency. An external resistor, R_{RT}, connected from VREF to RT/CT sets the charging current for the timing capacitor, C_{CT}, which is connected from RT/CT to GROUND. An R_{RT} value greater than 5 kΩ is recommended on RT/CT to set the positive ramp time of the internal oscillator. Using a value of 5 kΩ or greater for R_{RT} maintains a favorable ratio between the internal impedance and the external oscillator set resistor and results in minimal change in frequency over temperature. Using a value of less the recommended minimum value can result in frequency drift over temperature, part tolerances, or process variations.

The peak-to-peak amplitude of the oscillator waveform is 1.7 V in UCx84x devices. The UCx842 and UCx843 have a maximum duty cycle of approximately 100%, whereas the UCx844 and UCx845 are clamped to 50% maximum by an internal toggle flip flop. This duty cycle clamp is advantageous in most flyback and forward converters. For optimum IC performance the dead-time can not exceed 15% of the oscillator clock period. The discharge current, typically 6 mA at room temperature, sets the dead time. During the discharge, or *dead* time, the internal clock signal blanks the output to the low state. This limits the maximum duty cycle D_{MAX} to:

$$D_{MAX} = 1\ F : t_{DEADTIME} \times f_{OSC}\ ; \quad (7)$$

Equation 8 applies to UCx842 and UCx843 units because the OUTPUT switches at the same frequency as the oscillator and the maximum duty cycle can be as high as 100%.

$$D_{MAX} = 1-(I_{tDEADTIME}*\frac{f_{OSC}}{2}) \quad (8)$$

Equation 8 applies to UCx844 and UCx845 units because the OUTPUT switches at half the frequency as the oscillator and the maximum duty cycle can be as high as 50%.

When the power transistor turns off, a noise spike is coupled to the oscillator RT/CT terminal. At high duty cycles, the voltage at RT/CT is approaching the threshold level (approximately 2.7 V, established by the internal oscillator circuit) when this spike occurs. A spike of sufficient amplitude prematurely trips the oscillator. To minimize the noise spike, choose CCT as large as possible, remembering that dead time increases with CCT. CCT is recommended to never be less than approximately 1000 pF. Often the noise which causes this problem is caused by the OUTPUT being pulled below ground at turnoff by external parasitics. This is particularly true when driving MOSFETs. A Schottky diode clamp from GROUND to OUTPUT prevents such output noise from feeding to the oscillator.

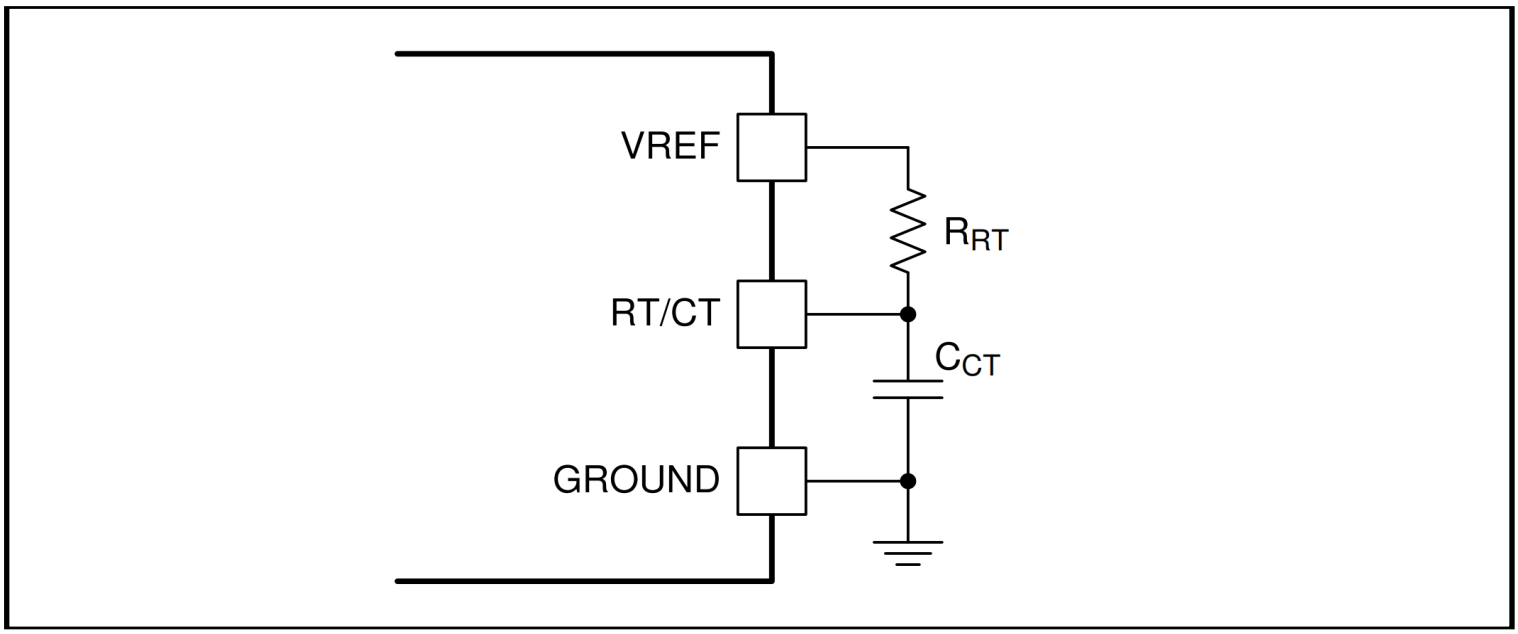


Figure 8. Schematic Diagram of the Oscillator Section

For R_{RT} > 5 kΩ: $f_{OSC}=\frac{1.72}{R_{RT}*C_{CT}}$

Synchronization

The simplest method for forced synchronization involves using a timing capacitor C_{CT} in near-standard configurations. Instead of grounding C_{CT} directly, a small resistor is connected in series with C_{CT} and grounded. This resistor serves as the input for the synchronization pulse, raising the C_{CT} voltage above the internal upper threshold of the oscillator. This allows the PWM to operate at the frequency set by R_{RT} and C_{CT} until the synchronization pulse occurs. This approach offers several advantages, including the ability to implement a local ramp for slope compensation. The UC3842/3/4/5 oscillator must be set to a frequency lower than that of the synchronization pulse stream (typically) and a 0.5 V pulse should be applied across the resistor.

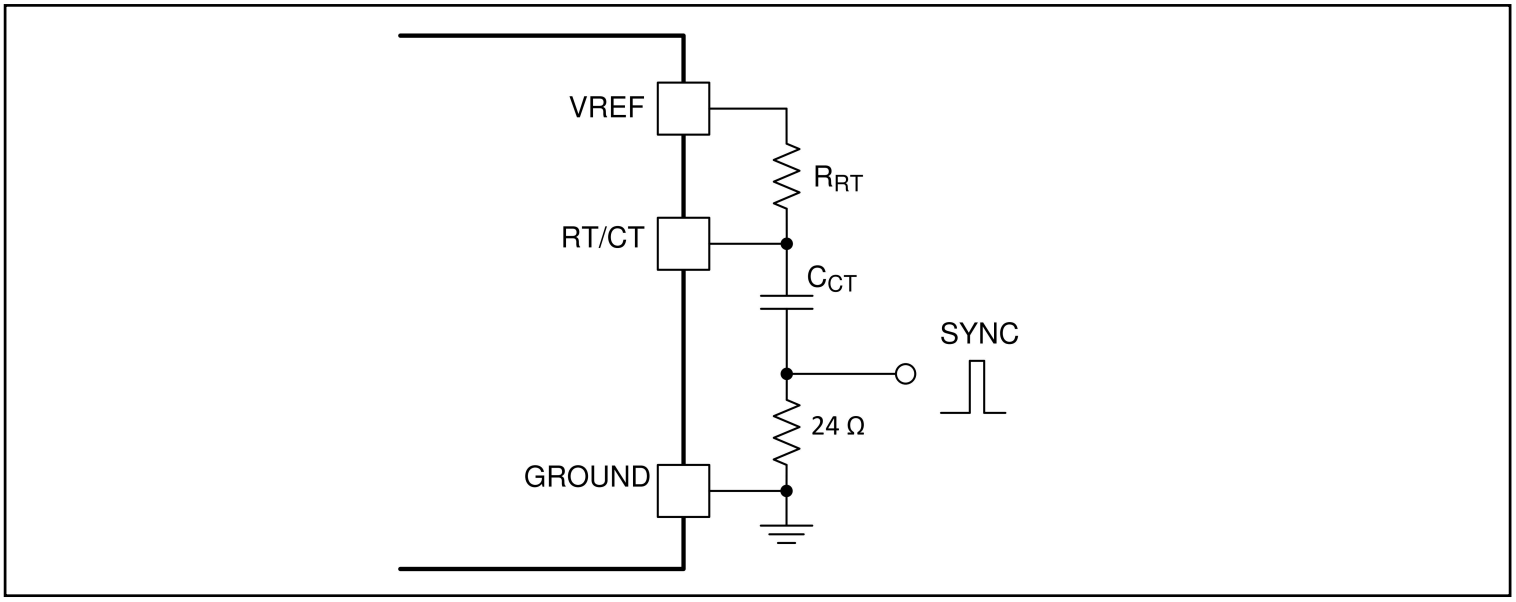


Figure 9. Synchronous Oscillator

Turn-off Technology

The PWM controller (see Figure 10) can be turned off in two ways: either by raising the voltage at ISENSE above 1 V, or by pulling the COMP terminal below the voltage corresponding to the voltage drop across two diodes connected to ground. Both methods will set the output of the PWM comparator to a high level (see Figure 10). The PWM latch is primarily reset so that its output remains low until the next clock cycle after the shutdown conditions at COMP or ISENSE are removed. In one example, external latch shutdown can be achieved by adding an SCR, which is reset by cycling VCC below the lower UVLO threshold. At this point, the reference is turned off, allowing the SCR to reset.

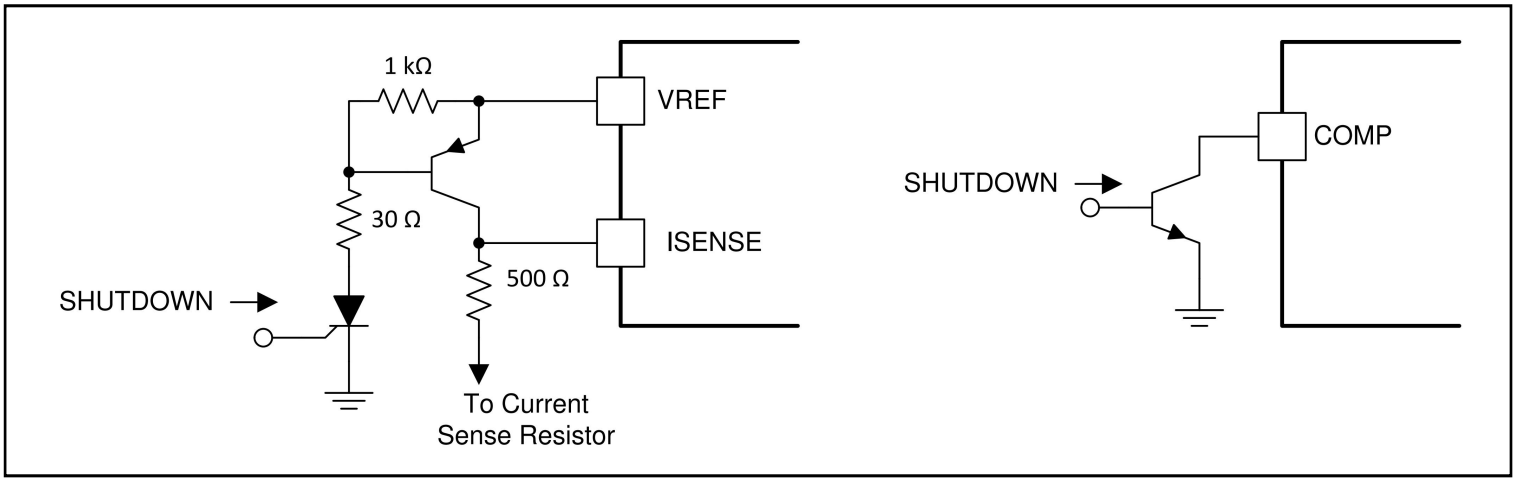


Figure 10. Power-off Technology

Slope Compensation

A portion of the oscillator slope can be combined with the current detection signal via resistor addition to provide slope compensation for converters with a duty cycle exceeding (see Figure 11).Note that the capacitor CCSF and RCSF form a filter to suppress switching spikes at the edge.

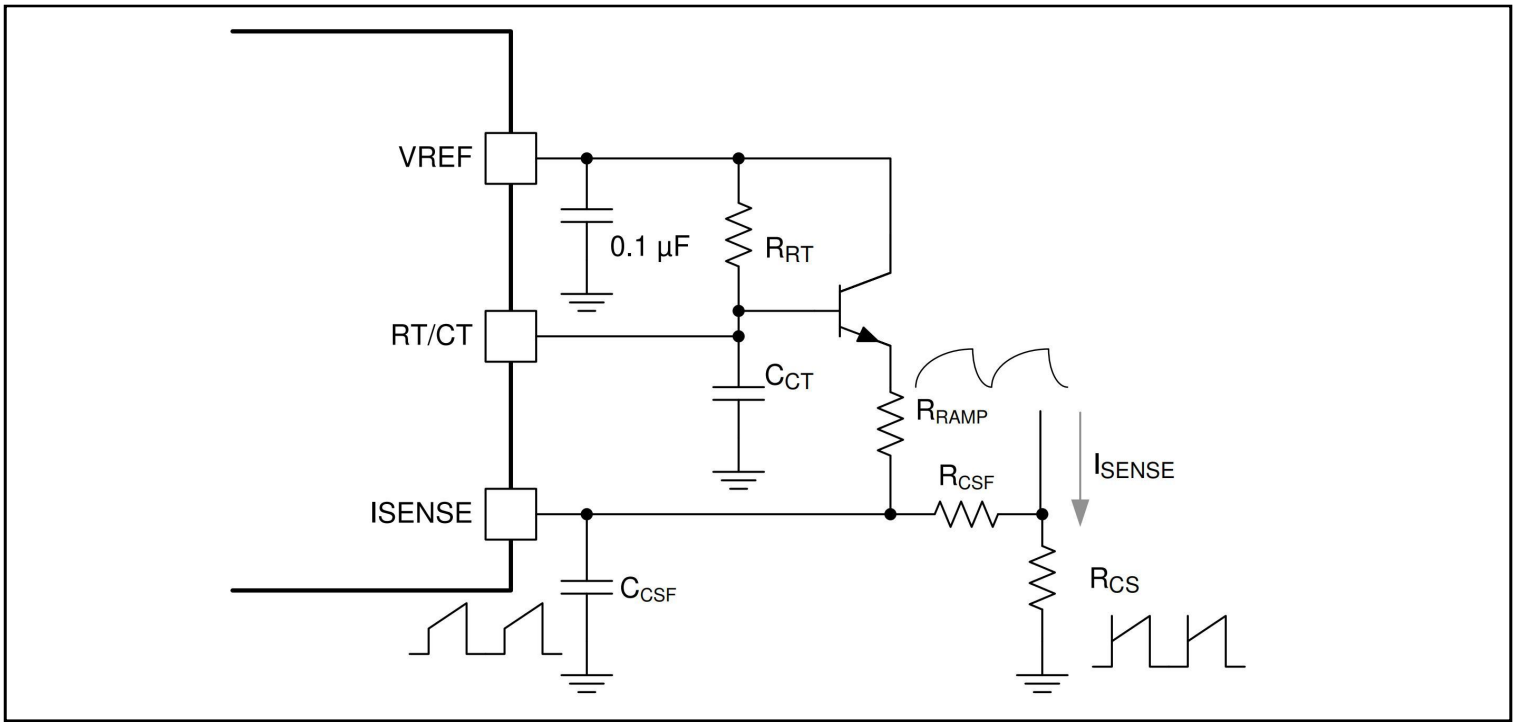


Figure 11. Slope Compensation

Soft Start: After power-on, it is advisable to gradually increase the PWM pulse width starting from zero dutycycle. The UCX84X device lacks built-in soft-start control, but this can be easily implemented externally using three components. A R/C network provides the time constant required to regulate the error amplifier's output. Additionally, transistors are employed to isolate the circuit from any operational node. These transistors also amplify the signal through their gain, thereby minimizing the load's impact on the RT/CT time constant.

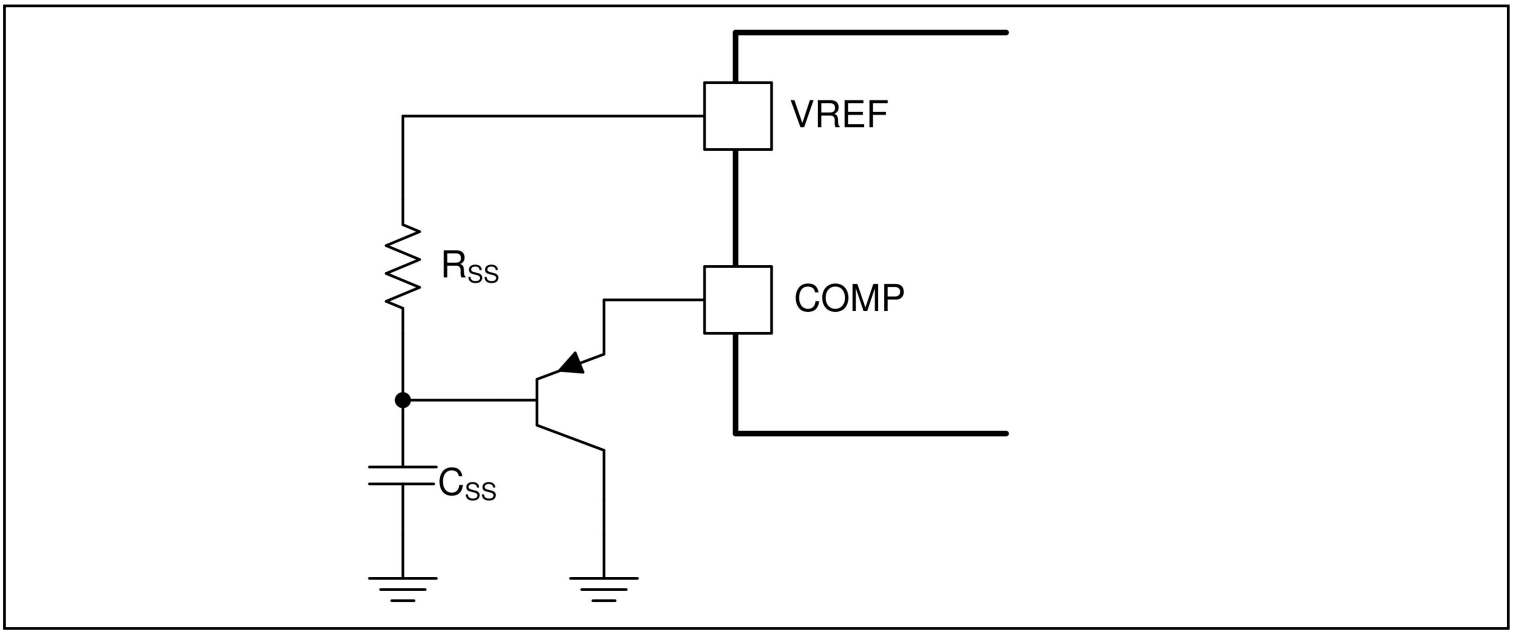


Figure 12. Soft-Start Circuit

Voltage Mode: In duty cycle control (voltage mode), pulse width modulation is achieved by comparing the output of the error amplifier with a manual ramp. The oscillator timing capacitor CCT generates a sawtooth waveform on the current or voltage mode IC. To utilize UCx 84x in the voltage mode configuration, this sawtooth waveform is fed to the current detection input ISENSE for comparison with the error voltage at the PWM comparator. In this approach, the sawtooth signal determines the pulse width rather than the actual primary current. Due to the difference between the low-output-resistance voltage amplifier in UCx84x and the transconductance (current)-type amplifier used in conventional voltage-mode controllers, loop compensation follows similar principles with minor variations.

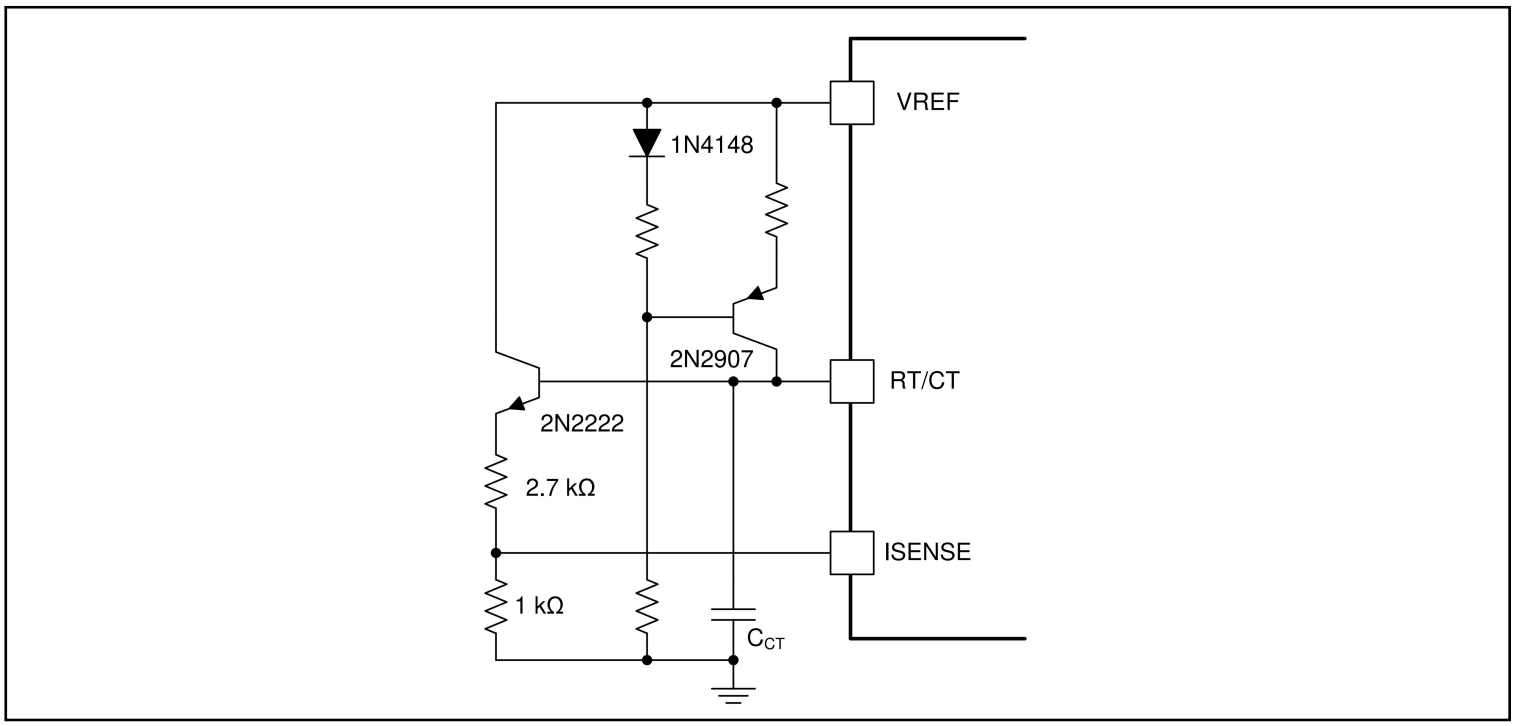


Figure 13. Current-Mode PWM Used as Voltage-Mode PWM

Device Function Mode

Normal Operation: During normal operation, the IC can be employed for peak current mode or voltage mode control. When the converter operates in peak current mode, the controller regulates both the peak current and duty cycle. In voltage mode controlusing the IC, the controller adjusts the po wer converter' s duty cycle. By integrating an error amplifier with an external feedback circuit, precise regulation of both the system's peak current and duty cycle is achieved.

UVLO Mode: During system startup, the VCC voltage begins to rise from 0V. Until the VCC voltage reaches the corresponding conduction threshold, the IC operates in UVLO mode. In this mode, no voltage is generated at the VREF pin. When VCC exceeds 1V but remains below the conduction threshold, the VREF pin is actively pulled to a low level by a 5kΩ resistor. Thus,VREF can serve as a logic signal indicating UVLO mode. If the bias voltage across VCC falls below the UVLO cutoff threshold, the PWM switch stops, and VREF returns to 0V. The device can be restarted by applying a voltage greater than the UVLO conduction threshold to the VCC pin.

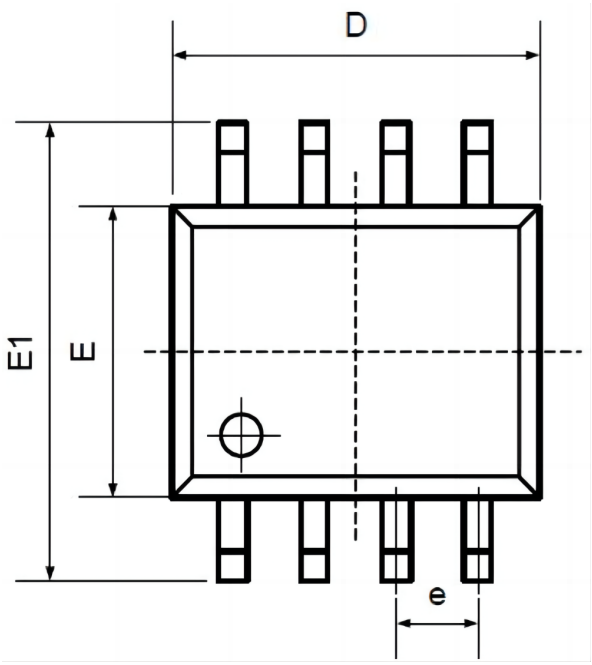
Order information

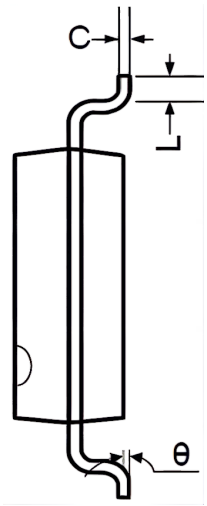
Order Number	Package	Package Quantity	Marking On The park	Temperature
UC2842D8TR-TUDI	SOP8	Tape,Reel,4000	UC2842	-40℃ to 85℃
UC2842N-TUDI	DIP8	Tube,50,A box of 2000	UC2842N	
UC2843D8TR-TUDI	SOP8	Tape,Reel,4000	UC2843	
UC2843N-TUDI	DIP8	Tube,50,A box of 2000	UC2843N	
UC2844D8TR-TUDI	SOP8	Tape,Reel,4000	UC2844	
UC2844N-TUDI	DIP8	Tube,50,A box of 2000	UC2844N	
UC2845D8TR-TUDI	SOP8	Tape,Reel,4000	UC2845	
UC2845N-TUDI	DIP8	Tube,50,A box of 2000	UC2845N	
UC3842D8TR-TUDI	SOP8	Tape,Reel,4000	UC3842	0℃ to 70℃
UC3842N-TUDI	DIP8	Tube,50,A box of 2000	UC3842N	
UC3843D8TR-TUDI	SOP8	Tape,Reel,4000	UC3843	
UC3843N-TUDI	DIP8	Tube,50,A box of 2000	UC3843N	
UC3844D8TR-TUDI	SOP8	Tape,Reel,4000	UC3844	
UC3844N-TUDI	DIP8	Tube,50,A box of 2000	UC3844N	
UC3845D8TR-TUDI	SOP8	Tape,Reel,4000	UC3845	
UC3845N-TUDI	DIP8	Tube,50,A box of 2000	UC3845N	

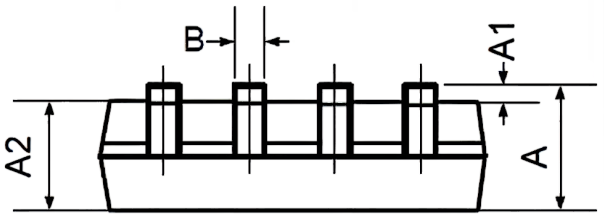
Revision history

	Date	Revision	Page
V1.0	2020/5	New	1-11
V1.1	2025/3	Update model and PDF template	1-27

Package SOP8

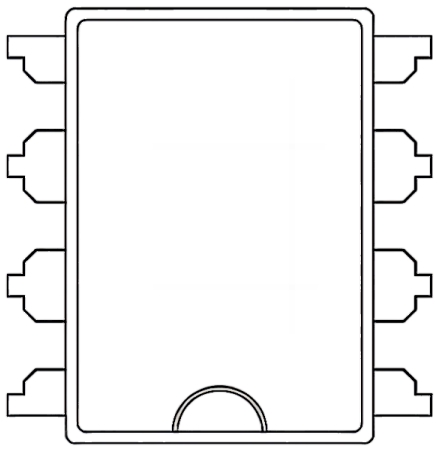


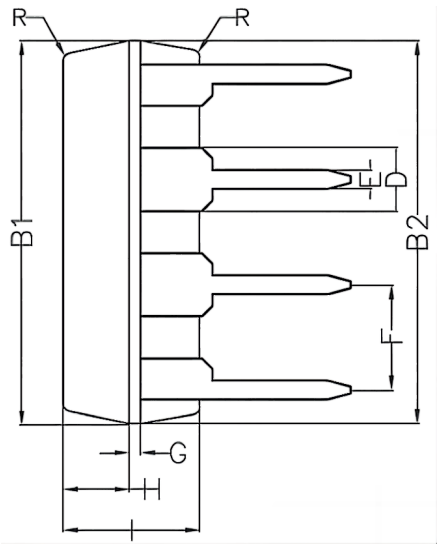


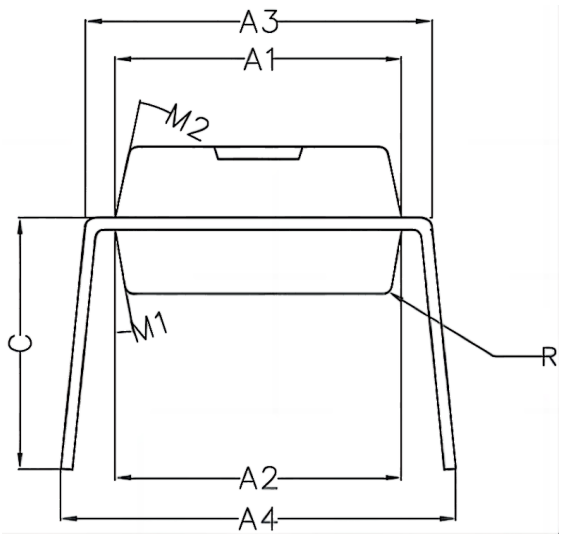


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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