

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-TL2842, TL2843, TL2844, TL2845
TL3842, TL3843, TL3844, TL3845

Current-Mode PWM Controllers

网址 www.sztdbdt.com

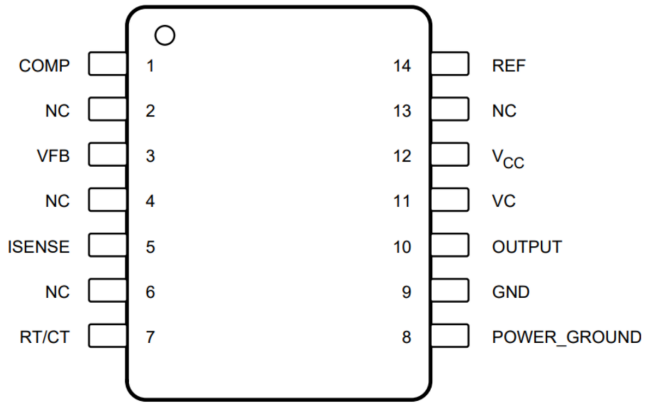
用芯智造·卓越品质

semiconductor device manufacturer

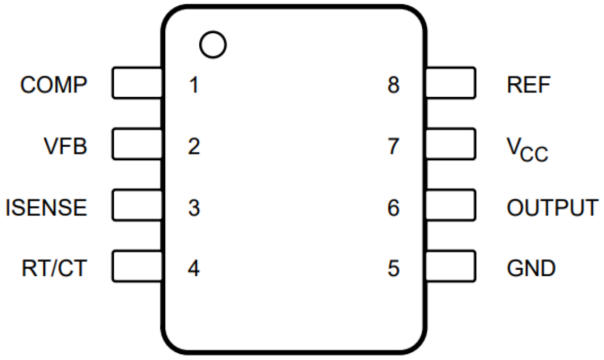
- Design
- research and development
- production
- and sales

Features

- Optimized for off-line and DC-to-DC converters
- Low start-up current (< 1mA)
- Automatic feed-forward compensation
- Pulse-by-pulse current limiting
- Enhanced load-response, characteristics
- Undervoltage lockout with hysteresis
- Double-pulse suppression
- High-current totem-pole output
- Internally trimmed bandgap reference
- 500kHz operation
- Error amplifier with low output resistance
- Designed to be interchangeable with UC2842 and UC3842 series



SOP14



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Applications

- Switching regulators of any polarity
- Transformer-coupled DC/DC convertors

Description

The TL284x and TL384x series of control integrated circuits provide the features that are necessary to implement off-line or DC-to-DC fixed-frequency current-mode control schemes, with a minimum number of external components. Some of the internally implemented circuits are an undervoltage lockout (UVLO), featuring a start-up current of less than 1mA, and a precision reference trimmed for accuracy at the error amplifier input. Other internal circuits include logic to ensure latched operation, a pulse-width modulation (PWM) comparator (that also provides current-limit control), and a totem-pole output stage designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the off state.

Table 1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	D	D or P		
COMP	1	1	I/O	Error amplifier compensation pin
GND	9	5	—	Device power supply ground terminal
ISENSE	5	3	I	Current sense comparator input
NC	2,4,6,13	—	—	Do not connect
OUTPUT	10	6	O	PWM Output
POWERGROUND	8	—	—	Output PWM ground terminal
REF	14	8	O	Oscillator voltage reference
RT/CT	7	4	I/O	Oscillator RC input
VC	11	—	—	Output PWM positive voltage supply
V_{CC}	12	7	—	Device positive voltage supply
VFB	3	2	I	Error amplifier input

(1) I = Input; O = Output; I/O = Input or Output

ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model(HBM),per ANSIESDAJEDEC JS-001,allpins(1)	±3000	V
	Charged device model (CDM),per JEDEC specification JESD22-C101,all ins(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage(2)	Self limiting		—
V_I	Analog input voltage range,VFB and ISENSE	-0.3	6.3	V
V_O	Output Voltage		35	V
V_I	Input Voltage,VC and D Package only		35	V
I_{CC}	Supply current		30	mA
I_O	Output current		± 1	A
	error amplifier output sink current		10	mA
T_J	Virtual junction temperature		150	℃
	Output energy(capacitive load)		5	μJ
T_{stg}	Storage temperature	-65	150	℃

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to the device GND pin.

Thermal Information

THERMAL METRIC(1)		TLx84x			UNIT
		D (SOIC)	D (SOIC)	P(PDIP)	
		8 PINS	14 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.4	87.9	74.1	℃/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{CC} and VC(1)	Supply Voltage				30	V
V_I,RT/CT	Input Voltage		0		5.5	V
V_I,VFB and ISENSE	Input Voltage		0		5.5	V
V_O,OUTPUT	Output voltage		0		30	V
V_O,POWER GROUND(1)	Output voltage		-0.1		1	V
I_{CC}	Supply current,externally limited				25	mA
I_O	Average output current				200	mA
$I_{O(ref)}$	Reference output current				-20	mA
f_{OSC}	Oscillator frequency			100	500	kHz
T_A	Operating free-air temperature	TL284x	-40		85	℃
		TL384x	0		70	

(1) These recommended voltages for VC and POWER GROUND apply only to the D package.

Electrical Characteristics

over operating free-air temperature range, V_{CC} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF (unless otherwise noted)

PARAMETER	TEST CONDITIONS(2)	TL284x			TL384x			UNIT
		MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
Reference Section								
Output voltage	I_O=1 mA,T_A=25℃	4.95	5	5.05	4.9	5	5.1	V
Line regulation	V_{CC}=12V to 25V		6	20		6	20	mV
Load regulation	I_O=1 mA to 20 mA		6	25		6	25	mV
Temperature coefficient of output voltage			0.2	0.4		0.2	0.4	mV/℃
Output voltage with worst-case variation	V_{CC}=12V to 25V, I_O=1mA to 20 mA	4.9		5.1	4.82		5.18	V

Electrical Characteristics(continued)

over operating free-air temperature range, V_{CC} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF (unless otherwise noted)

PARAMETER	TEST CONDITIONS(2)	TL284x			TL384x			UNIT
		MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
Output noise voltage	f=10 Hz to 10 kHz, T_A=25°C		50			50		μV
Output-voltage long-term drift	After 1000h at T_A=25 °C		5	25		5	25	mV
Short-circuit output current		-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Oscillator frequency(3)	T_A=25°C	47	52	57	47	52	57	kHz
Frequency change with supply voltage	V_{CC}=12V to 25V		2	10		2	10	Hz/ kHz
Frequency change with temperature			50			50		Hz/ kHz
peak-to-peak amplitude at RT/CT			1.7			1.7		V
Error-Amplifier Section								
Feedback input voltage	COMP at 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input bias current			-0.3	-1		-0.3	-2	μA
Open-loop voltage amplification	V_O=2V to 4V	65	90		65	90		dB
Gain-bandwidth product		0.7	1		0.7	1		MHz
Supply-voltage rejection ratio	V_{CC}=12V to 25V	60	70		60	70		dB
Output sink current	VFB,at 2.7 V,COMP at 1.1v	2	6		2	6		mA
Output source current	VFB,at 2.3 V,COMP at 5V	-0.5	-0.8		-0.5	-0.8		mA
Hihg-level output voltage	VFB,at 2.3 V,R_L=15kΩ to GND	5	6		5	6		V
Low-level output voltage	VFB,at 2.7 V,R_L=15kΩ to GND		0.7	1.1		0.7	1.1	V

Electrical Characteristics(continued)

over operating free-air temperature range, V_{CC} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF (unless otherwise noted)

PARAMETER		TEST CONDITIONS (2)	TL284x			TL384x			UNIT
			MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
Current-sense Section									
Voltage amplification		See(4)(5)	2.85	3	3.13	2.85	3	3.15	VN
Current-sense comparator threshold		COMP at 5V,see(4)	0.9	1	1.1	0.9	1	1.1	V
Supply-voltage rejection ratio		V_{CC}=12V to 25V, see(4)		70			70		dB
Input bias current				-2	-10		-2	-10	μA
Delay time to output				150	300		150	300	ns
Output Section									
High-level output voltage		I_{OH}=-20 mA	13	13.5		13	13.5		V
		I_{OH}=-200 mA	12	13.5		13	13.5		
Low-level output voltage		I_{OH}=20 mA		0.1	0.4		0.1	0.4	V
		I_{OH}=200 mA		1.5	2.2		1.5	2.2	
Rise time		C_L=1nF,T_A=25°C		25	150		25	150	ns
fall time		C_L=1nF,T_A=25°C		25	150		25	150	ns
Undervoltage-Lockout Section									
Start threshold voltage	TLx842, TLx844		15	16	17	14.5	16	17.5	V
	TLx843, TLx845		7.8	8.4	9	7.8	8.4	9	
Minimum operating voltage after startup	TLx842, TLx844		9	10	11	8.5	10	11.5	V
	TLx843, TLx845		7	7.6	8.2	7	7.6	8.02	
Pulse-Width-Modulator Section									
Maximum duty cycle	TLx842, TLx843		92%	97%	100%	92%	97%	100%	
	TLx844, TLx845		46%	48%	50%	46%	48%	50%	
Minimum duty cycle					0%			0%	

Electrical Characteristics(continued)

over operating free-air temperature range, V_{CC} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF (unless otherwise noted)

PARAMETER	TEST CONDITIONS (2)	TL284x			TL384x			UNIT
		MIN	TYP(2)	MAX	MIN	TYP(2)	MAX	
Supply Voltage								
Start-up current			0.5	1		0.5	1	mA
Operating supply current	VFB and ISENSE at 0V		11	17		11	17	mA
Limiting voltage	I_{CC}=25 mA		39			39		V

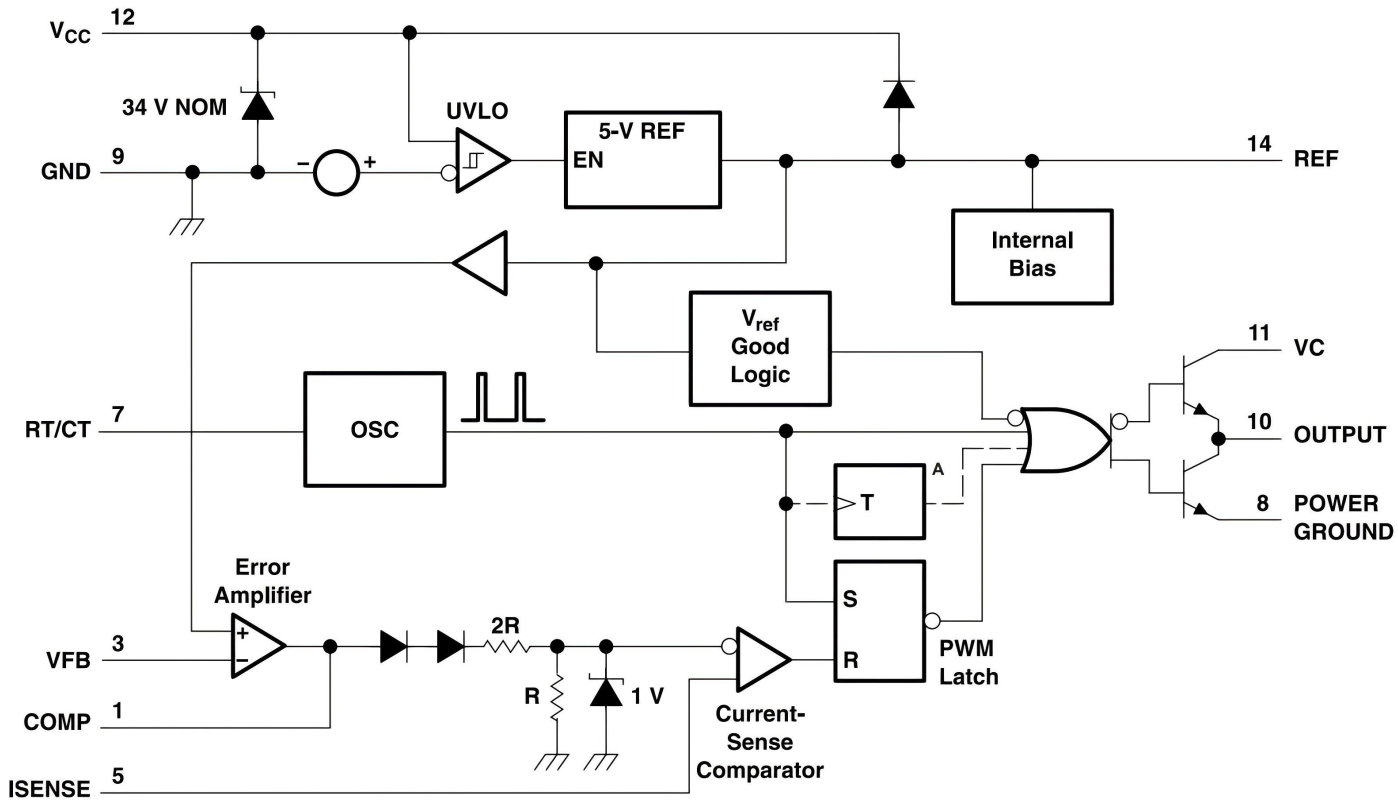
(1) Adjust VCC above the start threshold before setting it to 15 V.
(2) All typical values are at TA = 25°C.
(3) Output frequency equals oscillator frequency for the TLx842 and TLx843. Output frequency is one-half the oscillator frequency for the TLx844 and TLx845.
(4) These parameters are measured at the trip point of the latch, with VFB at 0 V.
(5) Voltage amplification is measured between ISENSE and COMP, with the input changing from 0 V to 0.8 V.

Detailed Description

Overview

The TL284x and TL384x series of control integrated circuits provide the features that are necessary to implement off-line or DC-to-DC fixed-frequency current-mode control schemes, with a minimum number of external components. Some of the internally implemented circuits are an undervoltage lockout (UVLO), featuring a start-up current of less than 1 mA, and a precision reference trimmed for accuracy at the error amplifier input. Other internal circuits include logic to ensure latched operation, a pulse-width modulation (PWM) comparator (that also provides current -limit control), and a totem-pole output stage designed to source or sink high-peak current. The output stage, suitable for driving N-channel MOSFETs, is low when it is in the off state.
Major differences between members of these series are the UVLO thresholds and maximum duty-cycle ranges. Typical UVLO thresholds of 16 V (on) and 10 V (off) on the TLx842 and TLx844 devices make them ideally suited to off-line applications. The corresponding typical thresholds for the TLx843 and TLx845 devices are 8.4 V (on) and 7.6 V (off). The TLx842 and TLx843 devices can operate to duty cycles approaching 100%. A duty-cycle range of 0 to 50% is obtained by the TLx844 and TLx845 by the addition of an internal toggle flip-flop, which blanks the output off every other clock cycle.
The TL284x-series devices are characterized for operation from -40°C to +85°C. The TL384x devices are characterized for operation from 0°C to 70°C.

Functional Block Diagram



A. The toggle flip-flop is present only in TL2844, TL2845, TL3844, and TL3845. Pin numbers shown are for the D (14-pin) package.

Feature Description

Pulse-by-Pulse Current Limiting：Pulse-by-pulse limiting is inherent in the control scheme. An upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation

Error Amplifier With Low Output Resistance：With a low output resistance, various impedance networks may be used on the compensation pin input for error amplifier feedback.

High-Current Totem-Pole Output：The output of the TLx84x devices can sink or source up to 1 A of current

Device Functional Modes

Shutdown Technique

The PWM controller (see Figure 1) can be shut down by two methods: either raise the voltage at ISENSE above 1 V or pull the COMP terminal below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (see Functional Block Diagram). The PWM latch is reset dominant so that the output remains low until the next clock cycle after the shutdown condition at the COMP or ISENSE terminal is removed. In one example, an externally latched shutdown can be accomplished by adding an SCR that resets by cycling VCC below the lower UVLO threshold. At this point, the reference turns off, allowing the SCR to reset.

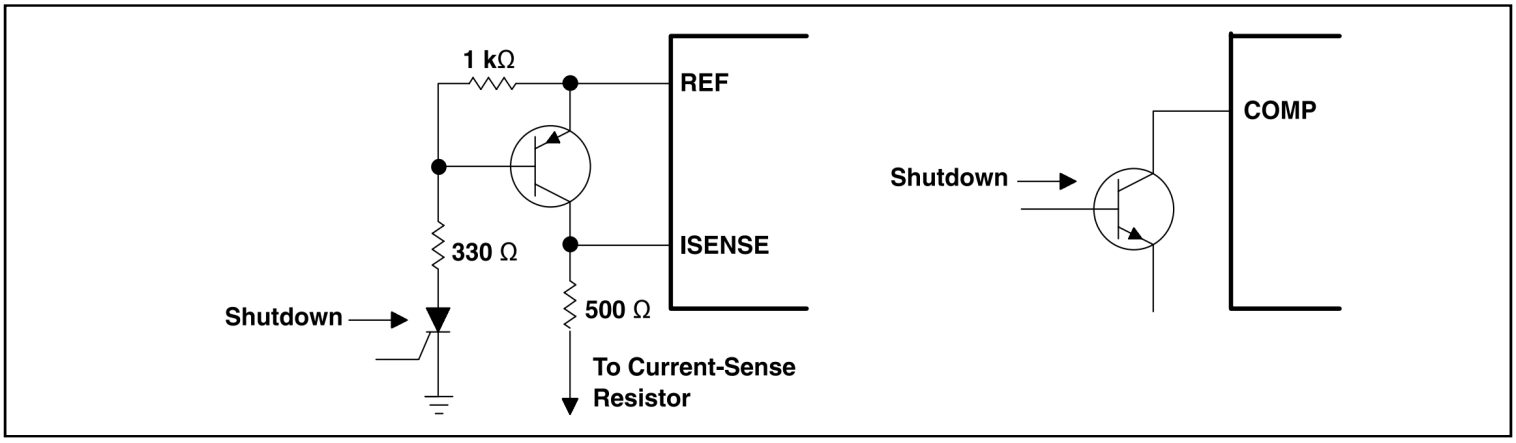


Figure 1. Shutdown Techniques

Slope Compensation

A fraction of the oscillator ramp can be summed resistively with the current-sense signal to provide slope compensation for converters requiring duty cycles over 50% (see Figure 2)

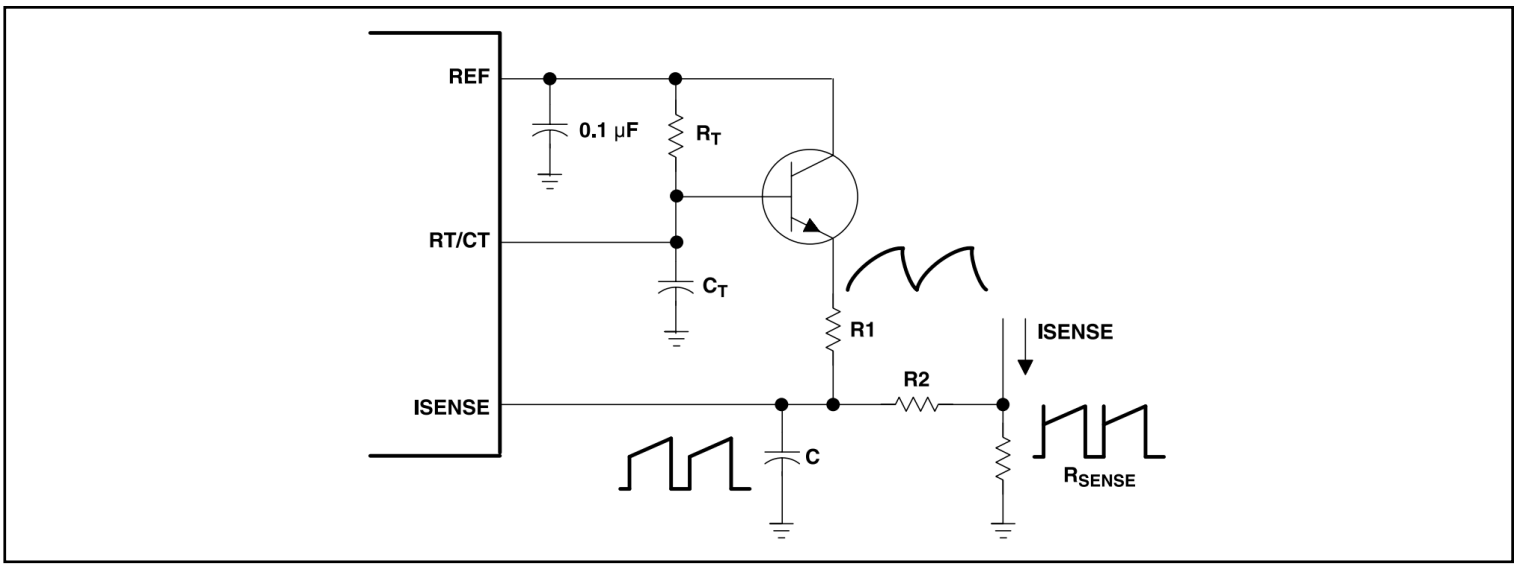


Figure 2. Slope Compensation

Application and Implementation

Typical Application

The following application is an open-loop laboratory test fixture. This circuit demonstrates the setup and use of the TL284x and TL384x devices and their internal circuitry.
In the open-loop laboratory test fixture (see Figure 3), high peak currents associated with loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to the GND terminal in a single-point ground. The transistor and 5-kΩ potentiometer sample the oscillator waveform and apply an adjustable ramp to the ISENSE terminal.

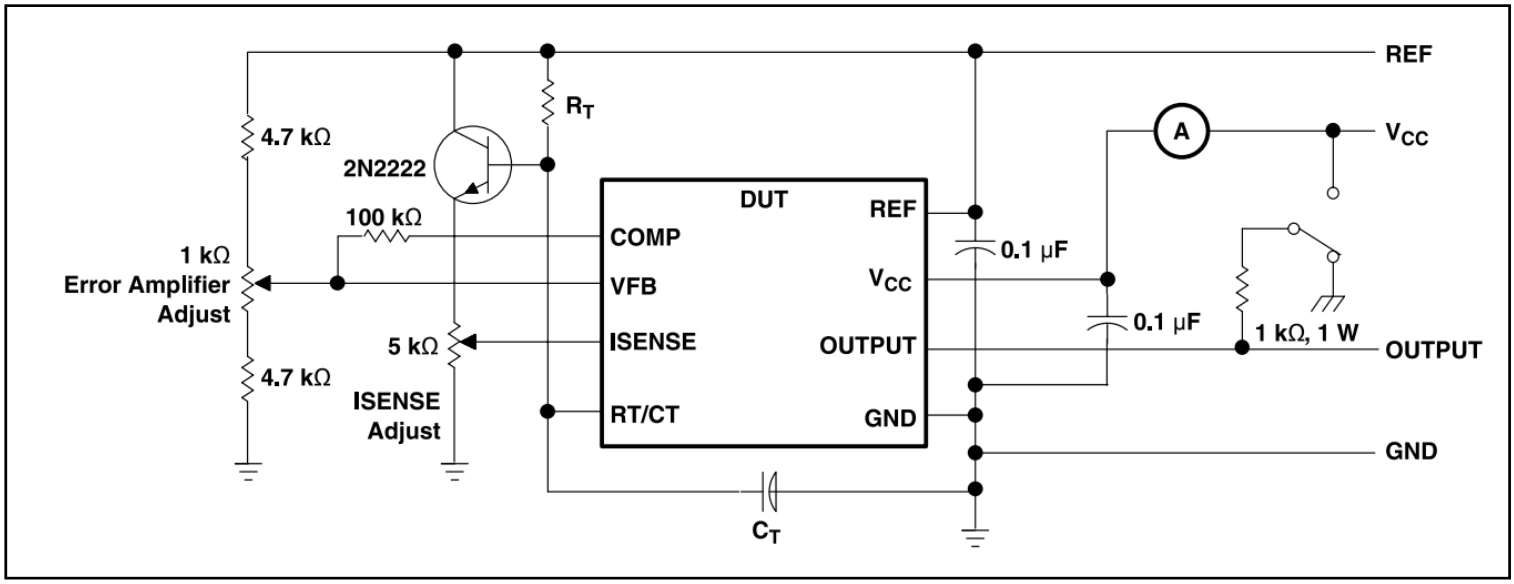


Figure 3. Open-Loop Laboratory Test Fixture

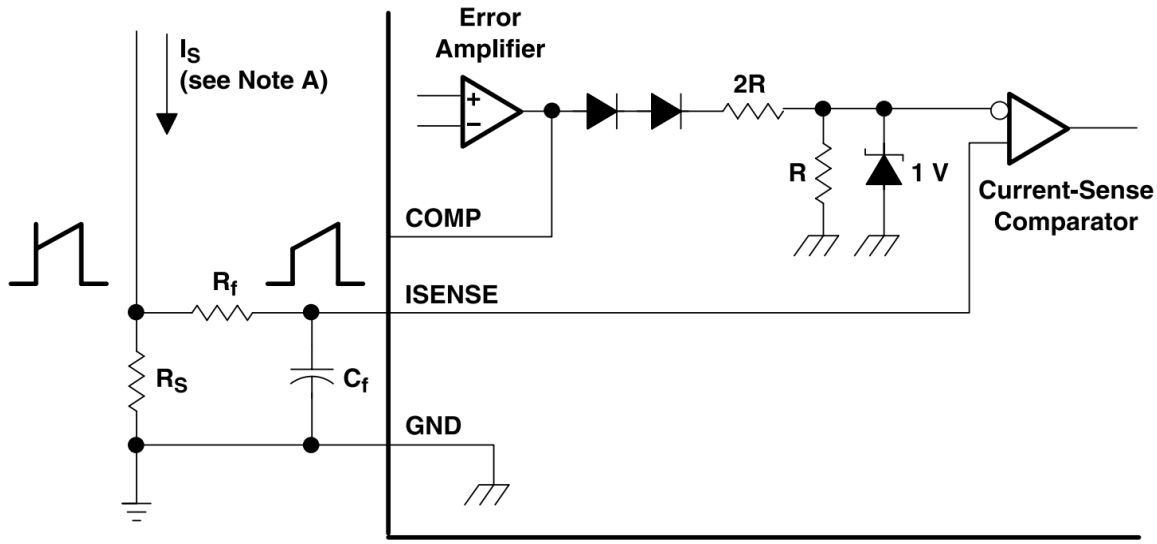
Design Requirements

The design techniques in the following sections may be used for power supply PWM applications which fall within the following requirements.

- 500-kHz or lower operation
- 30-V or less output voltage
- 200-mA or less output current

Detailed Design Procedure

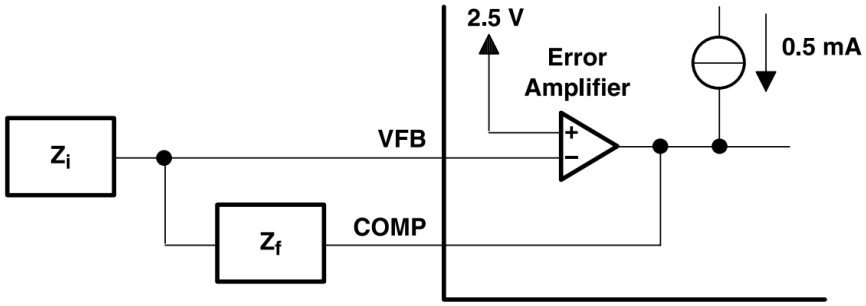
Current-Sense Circuit



A. Peak current (IS) is determined by the formula: $I_{S(max)} = \frac{1\ V}{R_S}$ A small RC filter formed by resistor Rf and capacitor Cf may be required to suppress switch transients

Figure 4. Current-Sense Circuit Schematic

Error-Amplifier Configuration



A. Error amplifier can source or sink up to 0.5 mA.

Figure 5. Error-Amplifier Configuration Schematic

Oscillator Section

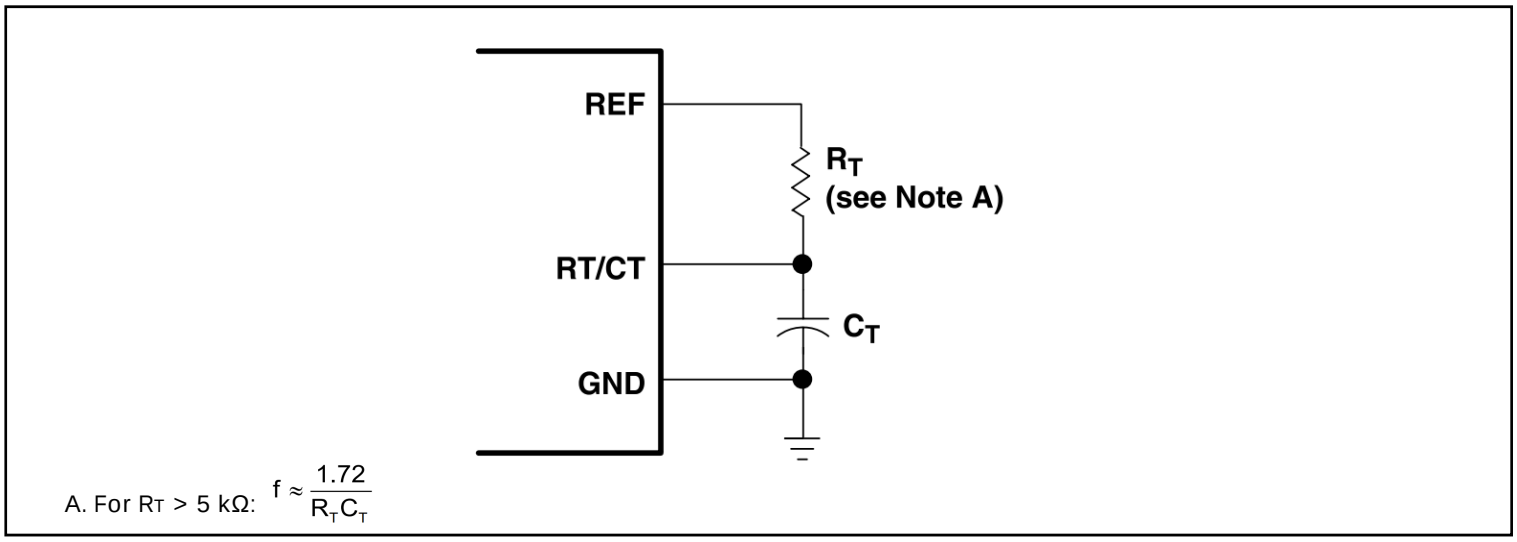


Figure 6. Oscillator Section Schematic

Power Supply Recommendations

See Recommended Operating Conditions for the recommended power supply voltages for the TL284x and TL384x devices. TI also recommends to have a decoupling capacitor on the output of the device's power supply to limit noise on the device input.

Layout

Layout Guidelines

Always try to use a low EMI inductor with a ferrite type closed core. Some examples would be toroid and encased E core inductors. Open core can be used if they have low EMI characteristics and are located a bit more away from the low power traces and components. Make the poles perpendicular to the PCB as well if using an open core. Stick cores usually emit the most unwanted noise

Feedback Traces

Try to run the feedback trace as far from the inductor and noisy power traces as possible. Also, keep the feedback trace to be as direct as possible and somewhat thick. These two sometimes involve a trade-off, but keeping it away from inductor EMI and other noise sources is the more critical of the two. Run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

Input/Output Capacitors

When using a low value ceramic input filter capacitor, it should be located as close to the V_{CC} pin of the IC as possible. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. Some designs require the use of a feed-forward capacitor connected from the output to the feedback pin as well, usually for stability reasons. In this case it should also be positioned as close to the IC as possible. Using surface mount capacitors also reduces lead length and lessens the chance of noise coupling into the effective antenna created by through-hole components.

Compensation Components

External compensation components for stability should also be placed close to the IC. Surface mount components are recommended here as well for the same reasons discussed for the filter capacitors. These should not be located very close to the inductor either

Traces and Ground Planes

Make all of the power (high current) traces as short, direct, and thick as possible. It is good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per Ampere. The inductor, output capacitors, and output diode should be as close to each other possible. This helps reduce the EMI radiated by the power traces due to the high switching currents through them. This will also reduce lead inductance and resistance as well, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors.
The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) should be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This will reduce noise as well by reducing ground loop errors as well as by absorbing more of the EMI radiated by the inductor. For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are) and the signal plane (where the feedback and compensation and components are) for improved performance. On multi-layer boards the use of vias will be required to connect traces and different planes. It is good practice to use one standard via per 200 mA of current if the trace will need to conduct a significant amount of current from one plane to the other.
Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states. One state when the switch is on and one when the switch is off. During each state there will be a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.

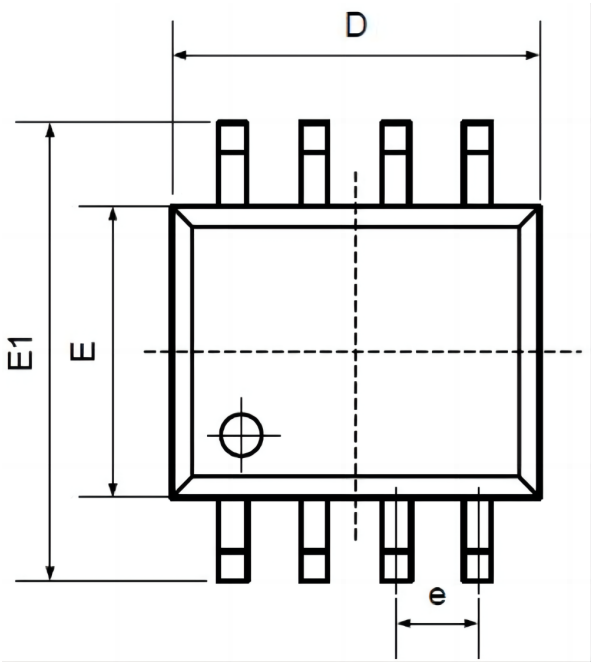
Order information

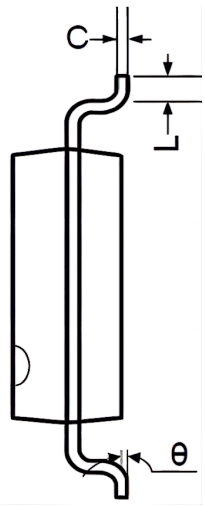
Order Number	Package	Package Quantity	Marking On The park	Temperature
TL2842DR-8-TUDI	SOP8	Tape,Reel,4000	TL2842	-40℃ to 85℃
TL2842P-TUDI	DIP8	Tube,50,A box of 2000	TL2842P	
TL2843DR-8-TUDI	SOP8	Tape,Reel,4000	TL2843	
TL2843P-TUDI	DIP8	Tube,50,A box of 2000	TL2843P	
TL2844DR-8-TUDI	SOP8	Tape,Reel,4000	TL2844	
TL2844P-TUDI	DIP8	Tube,50,A box of 2000	TL2844P	
TL2845DR-8-TUDI	SOP8	Tape,Reel,4000	TL2845	
TL2845P-TUDI	DIP8	Tube,50,A box of 2000	TL2845P	
TL3842DR-8-TUDI	SOP8	Tape,Reel,4000	TL3842	0℃ to 70℃
TL3842P-TUDI	DIP8	Tube,50,A box of 2000	TL3842P	
TL3843DR-8-TUDI	SOP8	Tape,Reel,4000	TL3843	
TL3843P-TUDI	DIP8	Tube,50,A box of 2000	TL3843P	
TL3844DR-8-TUDI	SOP8	Tape,Reel,4000	TL3844	
TL3844P-TUDI	DIP8	Tube,50,A box of 2000	TL3844P	
TL3845DR-8-TUDI	SOP8	Tape,Reel,4000	TL3845	
TL3845P-TUDI	DIP8	Tube,50,A box of 2000	TL3845P	

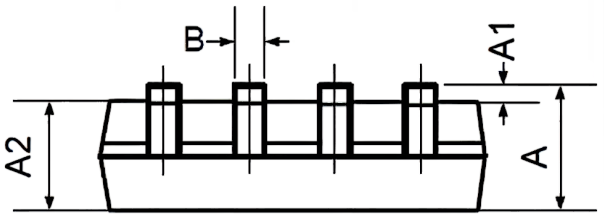
Revision history

	Date	Revision	Page
V1.0	2023/4	New	1-11
V1.1	2025/3	Update model and PDF template	1-18

Package SOP8

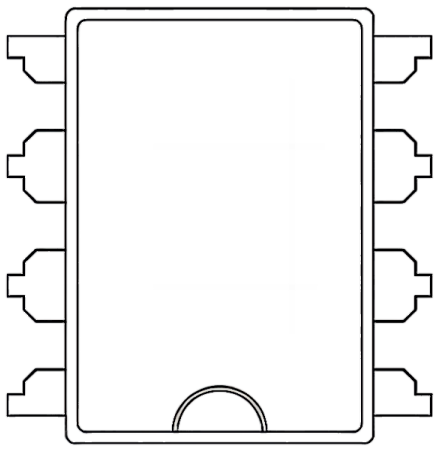


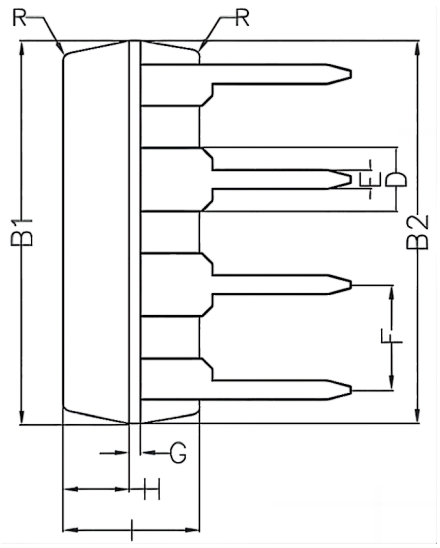


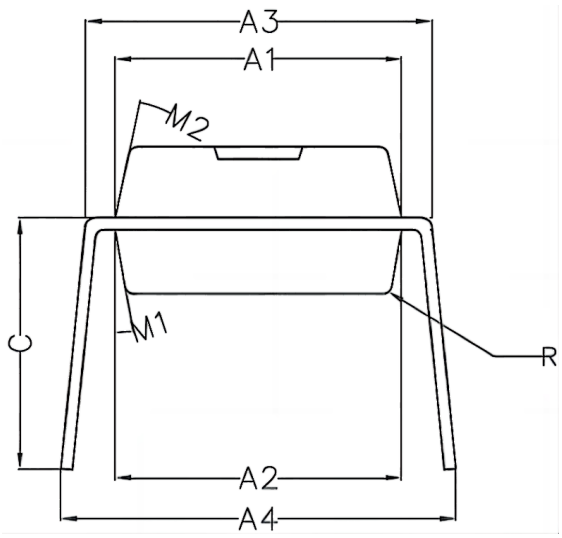


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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