Data Sheet

ADSP1802

SHARC Processor

FEATURES

- High performance 32-bit/40-bit floating-point processor for high performance audio processing
- SIMD computational architecture
- On-chip memory
  - 5 Mb L1 on-chip RAM
  - 8 Mb L2 RAM
- Maximum instruction rate up to 400 MHz
- Supports VISA
- Supports FIR, IIR, FFT accelerator
- DAI
  - 8 SPORTs
  - 4 PCGs
  - 1 S/PDIF transceiver
  - 4 ASRCs with −140 dB SNR performance
  - 1 IDP/PDAP
  - 1 DAI SRU
- DPI
  - 2 SPIs
  - 1 UART
  - 12 flags
  - 1 TWI
  - 3 PWM modules (PWM1, PWM2, and PWM3)
  - 2 general-purpose timers
  - 1 DPI SRU2
- 1 thermal diode
- AEC-Q100 qualified for automotive applications

APPLICATIONS

- Audio and acoustic processing in cabin, including active sound design, advanced chime, hands free and voice preprocessing, active noise cancellation, and audio path management
- Audio processing in consumer applications, including UI communication, professional audiovisual, hearables, and home theaters
- Intelligent buildings with security and surveillance

GENERAL DESCRIPTION

The ADSP1802 is a digital signal processor (DSP) that features Analog Devices, Inc. Super Harvard Architecture Single-Chip Computer (SHARC). The ADSP1802 is a 32-bit/40-bit floating point processor optimized for high performance audio applications with large on-chip RAM, multiple internal buses to eliminate I/O bottlenecks, and features an innovative digital applications interface (DAI).

FUNCTIONAL BLOCK DIAGRAM

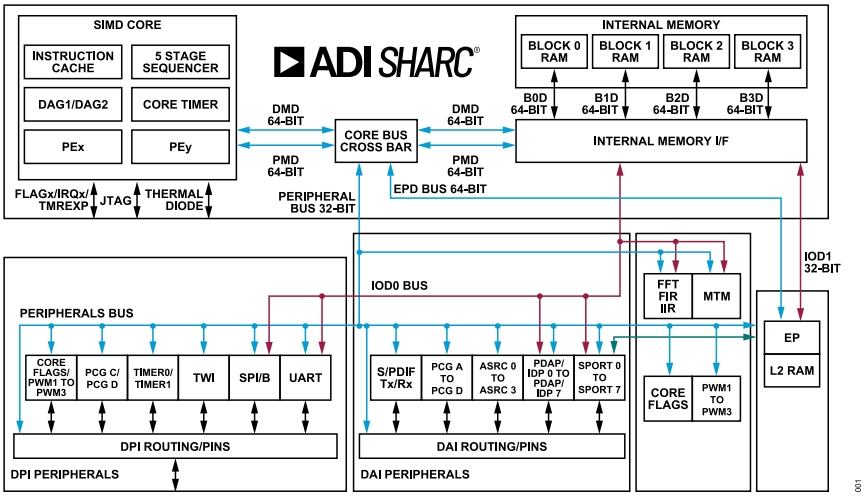

Figure 1. Functional Block Diagram

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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4/2024—Revision 0: Initial Version

SPECIFICATIONS

OPERATING CONDITIONS

Table 1. Operating Conditions

Parameter[1]	Description	Min	Typ	Max	Unit
V_{DD_INT}	Internal (Core) Supply Voltage	1.05	1.1	1.15	V
V_{DD_EXT}	External (I/O) Supply Voltage	3.13		3.47	V
V_{DD_THD}	Thermal Diode Supply Voltage	3.13		3.47	V
V_{IH}[2]	High Level Input Voltage at V_{DD_EXT} = Max	2.2			V
V_{IL}	Low Level Input Voltage at V_{DD_EXT} = Min	−0.3		+1.0	V
V_{IH_CLKIN}[3]	High Level Input Voltage at V_{DD_EXT} = Max	2.6			V
V_{IL_CLKIN}	Low Level Input Voltage at V_{DD_EXT} = Min	−0.3		+1.0	V
CONSUMER GRADE					
T_J	Junction Temperature 88-Lead Lead Frame Chip Scale Package (LFCSP)	0		105	°C
AUTOMOTIVE GRADE					
T_J	Junction Temperature 88-Lead Lead Frame Chip Scale Package (LFCSP)	−40		+125	°C

1 Specifications subject to change without notice.

2 Applies to input and bidirectional pins: FLAG0 to FLAG3, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{\text{RUNRSTIN}}$, $\overline{\text{RESET}}$, TCK, TMS, TDI, and $\overline{\text{TRST}}$.

3 Applies to input pins CLKIN.

ELECTRICAL CHARACTERISTICS

Table 2. Electrical Characteristics

Parameter[1]	Description	Conditions	Min	Typ	Max	Unit
V_{OH}[2]	High-Level Output Voltage	V_{DD_EXT} = min, I_{OH} = −1.0 mA[3]	2.4			V
V_{OL}[2]	Low-Level Output Voltage	V_{DD_EXT} = min, I_{OL} = 1.0 mA			0.4	V
I_{IH}[4, 5]	High-Level Input Current	V_{DD_EXT} = max, V_{IN} = V_{DD_EXT} max			10	µA
I_{IL}[4]	Low-Level Input Current	V_{DD_EXT} = max, V_{IN} = 0 V			10	µA
I_{ILPU}[5]	Low-Level Input Current Pull-Up	V_{DD_EXT} = max, V_{IN} = 0 V			200	µA
I_{OZH}[6, 7]	Three-State Leakage Current	V_{DD_EXT} = max, V_{IN} = V_{DD_EXT} max			10	µA
I_{OZL}[6]	Three-State Leakage Current	V_{DD_EXT} = max, V_{IN} = 0 V			10	µA
I_{OZLPU}[7]	Three-State Leakage Current Pull-Up	V_{DD_EXT} = max, V_{IN} = 0 V			200	µA
I_{DD_INT}	Supply Current (Internal)	V_{DD_INT} = 1.1 V, T_J = 25°C, 400 MHz, read/write ratio = 50:50		114		mA
C_{IN}[8]	Input Capacitance	T_J = 25°C			5	pF

1 Specifications subject to change without notice.

2 Applies to output and bidirectional pins: FLAG0 to FLAG3, DAI_Px, DPI_Px, $\overline{\text{EMU}}$, TDO, and $\overline{\text{RESETOUT/RUNRSTIN}}$.

3 See Output Drive Currents section for typical drive current capabilities.

4 Applies to input pins: BOOT_CFGx, CLK_CFGx, TCK, $\overline{\text{RESET}}$, and CLKIN.

5 Applies to input pins with internal pull-ups: $\overline{\text{TRST}}$, TMS, and TDI.

6 Applies to three statable pin TDO.

7 Applies to three statable pins with pull-ups: DAI_Px and DPI_Px.

8 Applies to all signal pins. Guaranteed, but not tested.

TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases.

SPECIFICATIONS

Consequently, it is not meaningful to add parameters to derive longer times. Switching characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor does in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Power-Up Sequencing

The timing requirements for processor startup are shown in Table 3. While no specific power-up sequencing is required between V_{DD_EXT} and V_{DD_INT}, review the following system design considerations:

- No power supply must be powered up for an extended period of time (>200 ms) before another supply starts to ramp up.
- If the V_{DD_INT} power supply comes up after the V_{DD_EXT}, any pin, such as $\overline{\text{RESETOUT}}$ and $\overline{\text{RESET}}$, may actually drive momentarily until the V_{DD_INT} rail has powered up. Systems sharing these signals on the board must determine if there are any issues that must be addressed based on this behavior.

Note that during power-up, when the V_{DD_INT} power supply comes up after V_{DD_EXT}, a leakage current of the order of three-state leakage current pull-up, even if that is an input only (for example the $\overline{\text{RESET}}$ pin) until the V_{DD_INT} rail has powered up.

Table 3. Power-Up Sequencing Timing Requirements (Processor Startup)

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DD_EXT} or V_{DD_INT} On	0		ms
$t_{IVDDEVDD}$	V_{DD_INT} On Before V_{DD_EXT}	–200	+200	ms
t_{CLKVDD}[1]	CLKIN Valid After V_{DD_INT} and V_{DD_EXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20[3]		µs
SWITCHING CHARACTERISTICS				
$t_{CORERST}$[4,5]	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	4096 × t_{CK} + 2 × t_{CCLK}		

1 Valid V_{DD_INT} and V_{DD_EXT} assume that the supplies are fully ramped to their nominal values (it does not matter which supply comes up first). Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

2 Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

3 Based on CLKIN cycles.

4 Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

5 The 4096 cycle count depends on t_{SRST} specification in Table 5. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

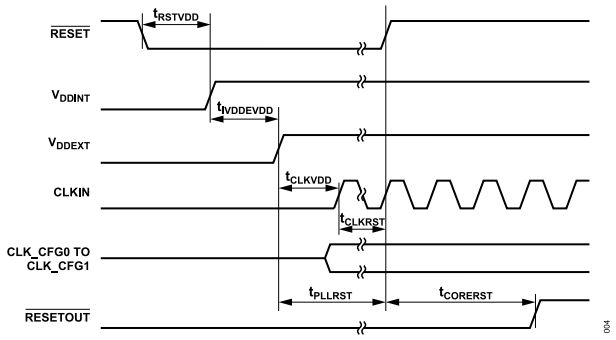

Figure 2. Power-Up Sequencing

SPECIFICATIONS

Clock Input

Table 4. Clock Input

Parameter	Description	400 MHz Min	400 MHz Max	Unit
TIMING REQUIREMENTS				
t_{CK}[1]	CLKIN Period	20[2]	100[3]	ns
t_{CKL}	CLKIN Width Low	10	45	ns
t_{CKH}	CLKIN Width High	10	45	ns
t_{CKRF}[4]	CLKIN Rise/Fall (0.4 V to 2.0 V)		3	ns
t_{CCLK}[5]	CCLK Period	2.5	10	ns
f_{VCO}	VCO Frequency	500	1500	MHz
t_{CKJ}[6]	CLKIN Jitter Tolerance	−250	+250	ps

1 Default value for PLL control bits in PMCTL.

2 Applies only for CLK_CFG1to CLK_CFG0 = 00

3 Applies only for CLK_CFG1to CLK_CFG0 = 01

4 Guaranteed by simulation but not tested on silicon.

5 Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.

6 Actual input jitters must be combined with AC specifications for accurate timing analysis. Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

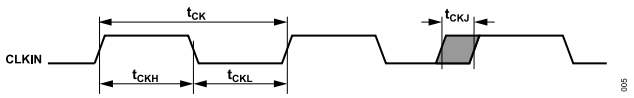

Figure 3. Clock Input

Reset

Table 5. Reset

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{WRST}[1]	$\overline{\text{RESET}}$ Pulse Width Low	4 × t_{CK}		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN high	8		ns

1 Applies after the power-up sequence is complete. At power-up, the internal PLL of the processor requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including the startup time of external clock oscillator).

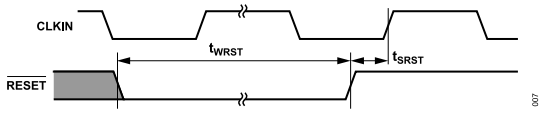

Figure 4. Reset

Running Reset

The following timing specification applies to the $\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$ pin when it is configured as $\overline{\text{RUNRSTIN}}$.

Table 6. Running Reset

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
$t_{WRUNRST}$	Running $\overline{\text{RESET}}$ Pulse Width Low	4 × t_{CK}		ns

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Table 6. Running Reset (Continued)

Parameter	Description	Min	Max	Unit
$t_{SRUNRST}$	Running $\overline{RESET}$ Setup Before CLKIN Low	8		ns

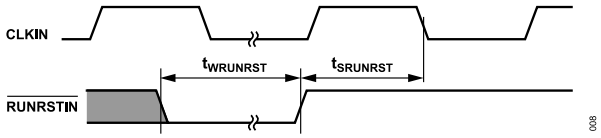

Figure 5. Running Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$ interrupts, as well as the DAI_P1 to DAI_P20 and DPI_P1 to DPI_P14 pins when they are configured as interrupts.

Table 7. Interrupts

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENT				
t_{IPW}	$\overline{IRQx}$ Pulse Width	$2 \times t_{PCLK} + 2$		ns

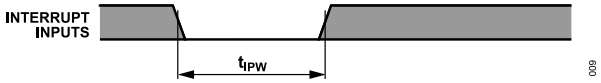

Figure 6. Interrupt

Core Timer

Table 8. Core Timer

Parameter	Description	Min	Max	Unit
SWITCHING CHARACTERISTIC				
t_{WCTIM}	TMREXP Pulse Width	$4 \times t_{CCLK} - 1$		ns

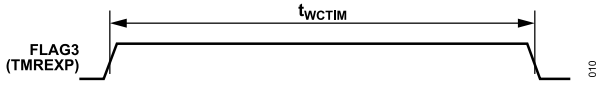

Figure 7. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer0 and Timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P1 to DPI_P14 pins through the digital peripheral interface (DPI) signal routing unit (SRU). Therefore, the timing specification provided in Table 9 is valid at the DPI_P1 to DPI_P14 pins.

Table 9. Timer PWM_OUT Timing

Parameter	Description	Min	Max	Unit
SWITCHING CHARACTERISTIC				
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 1.2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

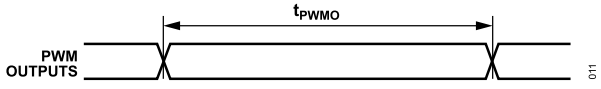

Figure 8. Timer PWM_OUT Timing

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Timer WDTH_CAP Timing

The following timing specification applies to Timer0 and Timer1, and in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P1 to DPI_P14 pins through the SRU. Therefore, the timing specification provided in Table 10 is valid at the DPI_P1 to DPI_P14 pins.

Table 10. Timer Width Capture Timing

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENT				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns



Figure 9. Timer Width Capture Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example DAI_PB01_I to DAI_PB02_O).

Table 11. DAI/DPI Pin to Pin Routing

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENT				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid	1.5	12	ns

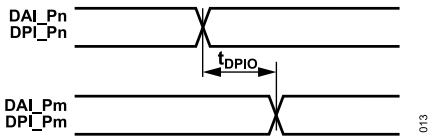

Figure 10. DAI/DPI Pin to Pin Routing

Precision Clock Generators (PCGs) (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the PCG takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 to DAI_P20)

Table 12. PCG (Direct Pin Routing)

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{PCGIW}	Input Clock Period	$t_{PCLK} \times 4$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
SWITCHING CHARACTERISTICS				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$[1]	$10 + ((2.5 + D - PH) \times t_{PCGIP})$[1]	ns
t_{PCGOW}[2]	Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

[1] D = FSxDIV means divisor for frame sync of PCG A, PCG B, PCG C, and PCG D. PH = FSxPHASE means phase for frame sync of PCG A, PCG B, PCG C, and PCG D.

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[2] Normal mode of operation.

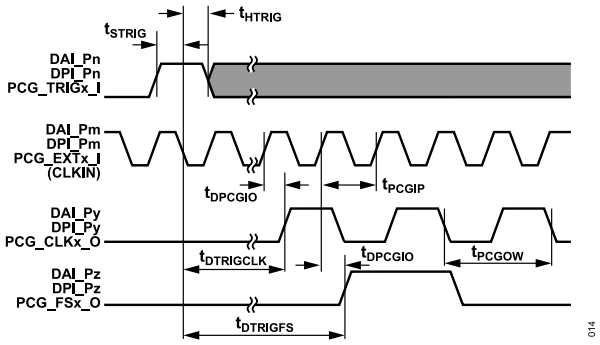

Figure 11. PCG (Direct Pin Routing)

Flags

The timing specifications provided in Table 13 apply to the DPI_P1 to DPI_P14 and FLAG0 to FLAG3 pins when configured as flags.

Table 13. Flags

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENT				
t_{FIPW}[1]	FLAG0 to FLAG3 Input Pulse Width	2 × t_{PCLK} + 3		ns
SWITCHING CHARACTERISTIC				
t_{FOPW}[1]	FLAG0 to FLAG3 Output Pulse Width	2 × t_{PCLK} − 3		ns

[1] This is applicable when the flags are connected to DPI_P1 to DPI_P14 and FLAG0 to FLAG3 pins.

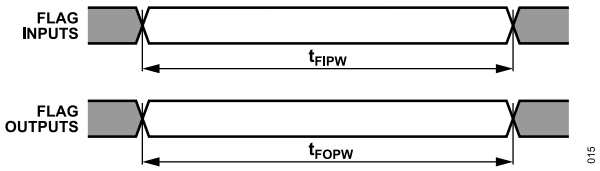

Figure 12. Flags

Serial Ports (SPORTs)

In subordinate transmitter mode and main receiver mode, the maximum SPORT frequency is $f_{PCLK}/8$. In main transmitter mode and subordinate receiver mode, the maximum SPORT clock frequency is $f_{PCLK}/4$. To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed:

- Frame sync delay and frame sync setup and hold
- Data delay and data setup and hold
- SCLK width

SPORT signals (SCLK, frame sync, Data Channel A, and Data Channel B) are routed to the DAI_P1 to DAI_P20 pins using the SRU. Therefore, the timing specifications provided in Table 14, Table 15, Table 16, Table 17, and Table 18 are valid at the DAI_P1 to DAI_P20 pins.

Table 14. SPORTs—External Clock

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{SFSE}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5		ns

SPECIFICATIONS

Table 14. SPORTs—External Clock (Continued)

Parameter	Description	Min	Max	Unit
t_{HFSE}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	1.9		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 1.5$		ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$		ns
SWITCHING CHARACTERISTICS				
t_{DFSE}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)		10.25	ns
t_{HOFSE}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)	2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		9	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		ns

[1] Referenced to sample edge.

[2] Referenced to drive edge.

Table 15. SPORTs—Internal Clock

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	7		ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		ns
SWITCHING CHARACTERISTICS				
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		4	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	−1		ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		9.75	ns
t_{HOFSR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	−1		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3.25	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	−2		ns
t_{SCKLIW}	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to sample edge.

[2] Referenced to drive edge.

SPECIFICATIONS

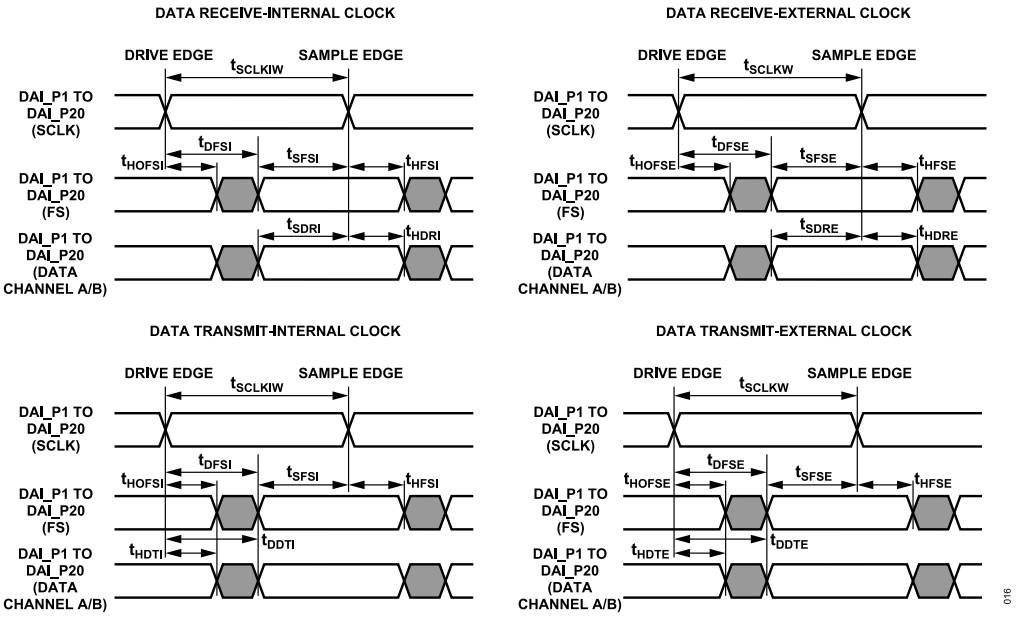

Figure 13. SPORTs

Table 16. SPORTs—External Late Frame Sync

Parameter	Description	Min	Max	Unit
SWITCHING CHARACTERISTICS				
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0		8.5	ns
$t_{DDTENFS}$	Data Enable for MCE = 1, MFD = 0	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified, as well as DSP serial mode, and MCE = 1, MFD = 0.

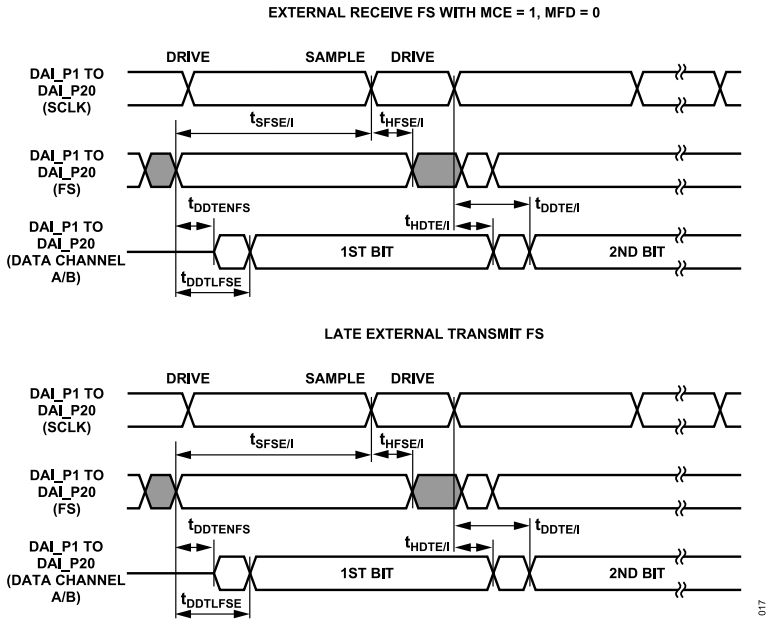

Figure 14. External Late Frame Sync (Reflects Changes Made to Support Left-Justified Mode)

SPECIFICATIONS

Table 17. SPORTs—Enable and Three-State

Parameter	Description	Min	Max	Unit
SWITCHING CHARACTERISTICS				
t_{DDTEN}[1]	Data Enable from External Transmit SCLK	2		ns
t_{DDTTE}[1]	Data Disable from External Transmit SCLK		11.5	ns
t_{DDTIN}[1]	Data Enable from Internal Transmit SCLK	−1.5		ns

[1] Referenced to drive edge.

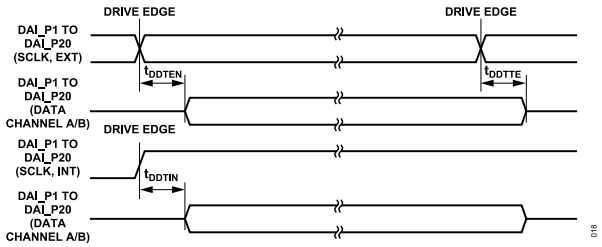

Figure 15. SPORTs—Enable and Three-State

The SPORTx_TDV_O output signal (routing unit) becomes active in SPORT multichannel mode. During transmit slots (enabled with active channel selection registers) the SPORTx_TDV_O is asserted for communication with external devices.

Table 18. SPORTs—Transmit Data Valid (TDV)

Parameter	Description	Min	Max	Unit
SWITCHING CHARACTERICTICS[1]				
t_{DRDVEN}	TDV Assertion Delay from Drive Edge of External Clock	3		ns
t_{DFDVEN}	TDV Deassertion Delay from Drive Edge of External Clock		8	ns
t_{DRDVIN}	TDV Assertion Delay from Drive Edge of Internal Clock	−1		ns
t_{DRDVIN}	TDV Deassertion Delay from Drive Edge of Internal Clock		2	ns

[1] Referenced to drive edge

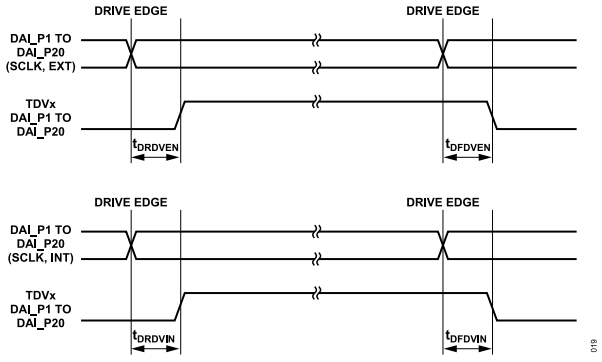

Figure 16. SPORTs—TDM Internal and External Clock

Input Data Port (IDP)

IDP signals are routed to the DAI_P1 to DAI_P20 pins using the SRU. Therefore, the timing specifications provided in Table 19 are valid at the DAI_P1 to DAI_P20 pins.

Table 19. Serial Ports—Input Data Port (IDP)

Parameter	Description	Min	Max	Unit
SWITCHING CHARACTERISTICS				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3.8		ns

SPECIFICATIONS

Table 19. Serial Ports—Input Data Port (IDP) (Continued)

Parameter	Description	Min	Max	Unit
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	2.5		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	2.5		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG input can be either the CLKIN pin or any of the DAI pins.

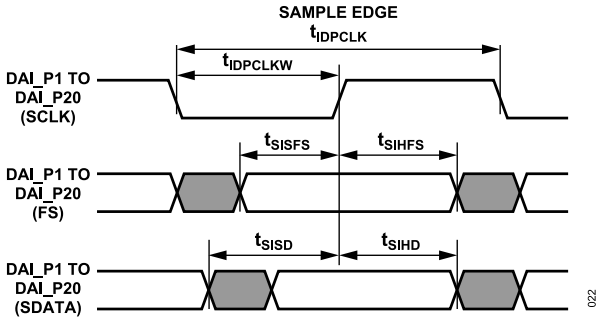

Figure 17. IDP Main Timing

Parallel Data Acquisition Port (PDAP)

PDAP is the parallel mode operation of Channel 0 of the IDP.

Table 20. PDAP

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{SPHOLD}[1]	PDAP_HOLD Setup Before PDAP_CLK Sample Edge	2.5		ns
t_{HPHOLD}[1]	PDAP_HOLD Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDSD}[1]	PDAP_DAT Setup Before PDAP_CLK Sample Edge	3.85		ns
t_{PDHD}[1]	PDAP_DAT Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDCLKW}	Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$		ns
t_{PDCLK}	Clock Period	$t_{PCLK} \times 4$		ns
SWITCHING CHARACTERISTICS				ns
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} + 3$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1.5$		ns

[1] Source pins of PDAP_DATA are DAI pins. Source pins for PDAP_CLK and PDAP_HOLD are DAI pins, CLKIN through PCG, and DAI pins through PCG.

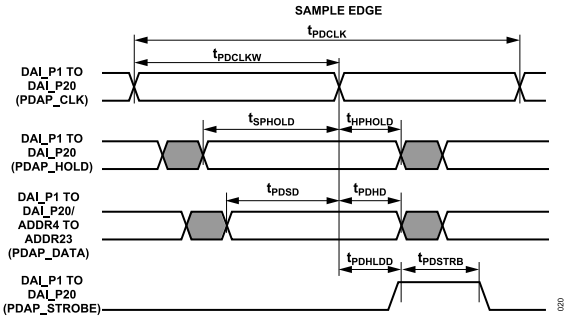

Figure 18. PDAP Timing

SPECIFICATIONS

Sample Rate Converter (SRC)—Serial Input Port

The asynchronous sample rate converter (ASRC) input signals are routed from the DAI_P1 to DAI_P20 pins using the SRU. Therefore, the timing specifications provided in Table 21 are valid at the DAI_P1 to DAI_P20 pins.

Table 21. ASRC, Serial Input Port

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{SRCSFS} [1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS} [1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
t_{SRCSD} [1]	Data Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHD} [1]	Data Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG input can be either CLKIN or any of the DAI pins.

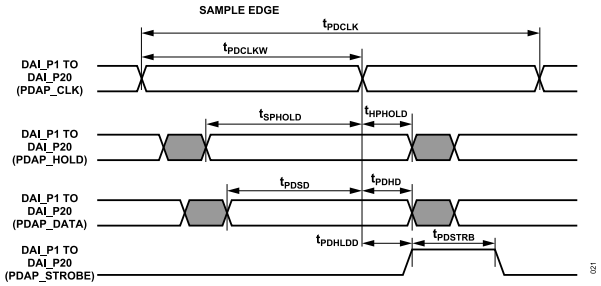

Figure 19. ASRC Serial Input Port Timing

SRC—Serial Output Port

For the serial output port, the frame sync is an input, and it must meet setup and hold times about SCLK on the output port. The serial data output has a hold time and delay specification about serial clock. Note that serial clock rising edge is the sampling edge, and the falling edge is the drive edge.

Table 22. ASRC, Serial Output Port

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{SRCSFS} [1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS} [1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns
SWITCHING CHARACTERISTICS				
t_{SRCTDD} [1]	Transmit Data Delay After Serial Clock Falling Edge		9.9	ns
t_{SRCTDH} [1]	Transmit Data Hold After Serial Clock Falling Edge	1		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG input can be either CLKIN or any of the DAI pins.

SPECIFICATIONS

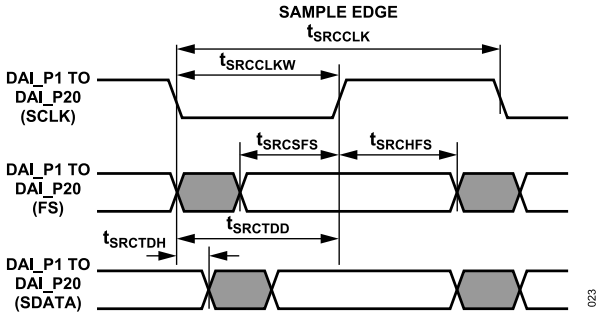

Figure 20. ASRC Serial Output Port Timing

PWM Generators

The following timing specifications apply when the DPI_P1 to DPI_P14 pins are configured as PWM.

Table 23. PWM Timing

Parameter	Description	Min	Max	Unit
SWITCHING CHARACTERISTICS				
t_{PWMW}	PWM Output Pulse Width	t_{PCLK} − 2	$(2^{16} - 2) \times t_{PCLK}$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK}$ − 1.5	$(2^{16} - 1) \times t_{PCLK}$	ns

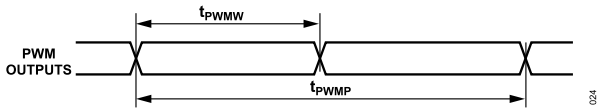

Figure 21. PWM Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left-justified, I²S, or right-justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

In the right-justified mode, the frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The most significant bit (MSB) is delayed the minimum in 24-bit output mode or the maximum in 16-bit output mode from a frame sync transition. Therefore, when there are 64 serial clock periods per frame sync period, the least significant bit (LSB) of the data is right-justified to the next frame sync transition.

Table 24. S/PDIF Transmitter Right-Justified Mode

Parameter	Description	Nominal	Unit
TIMING REQUIREMENT			
t_{RJD}	Frame Sync to MSB Delay in Right-Justified Mode		
	16-Bit Word Mode	16	SCLK
	18-Bit Word Mode	14	SCLK
	20-Bit Word Mode	12	SCLK
	24-Bit Word Mode	8	SCLK

SPECIFICATIONS

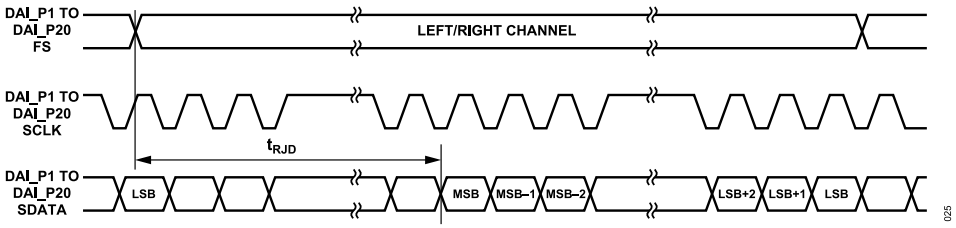

Figure 22. Right-Justified Mode

In the default I²S-justified mode, the frame sync is low for the left channel and high for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition but with a delay.

Table 25. S/PDIF Transmitter I²S Mode

Parameter	Description	Nominal	Unit
TIMING REQUIREMENT			
t_{I2SD}	Frame Sync to MSB Delay in I²S Mode	1	ACLK

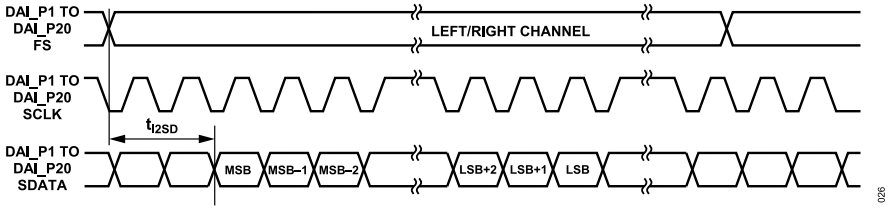

Figure 23. I²S-Justified Mode

In the left-justified mode, the frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition with no delay.

Table 26. S/PDIF Transmitter Left-Justified Mode

Parameter	Description	Nominal	Unit
TIMING REQUIREMENT			
t_{LJD}	Frame Sync to MSB Delay in Left-Justified Mode	0	SCLK

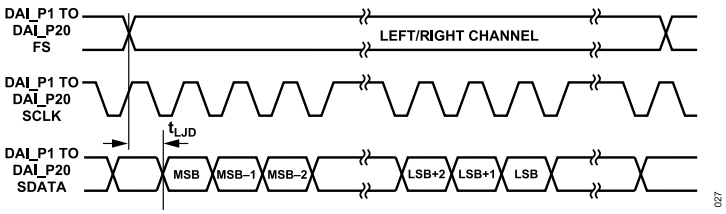

Figure 24. Left-Justified Mode

S/PDIF Transmitter Input Data Timing

Input signals are routed to the DAI_P1 to DAI_P20 pins using the SRU. Therefore, the timing specifications provided in Table 27 are valid at the DAI_P1 to DAI_P20 pins.

Table 27. S/PDIF Transmitter Input Data Timing

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	3		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		ns

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Table 27. S/PDIF Transmitter Input Data Timing (Continued)

Parameter	Description	Min	Max	Unit
$t_{SISCLKW}$	Clock Width	36		ns
t_{SISCLK}	Clock Period	80		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		ns
$t_{SITXCLK}$	Transmit Clock Period	20		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG input can be either the CLKIN pin or any of the DAI pins.

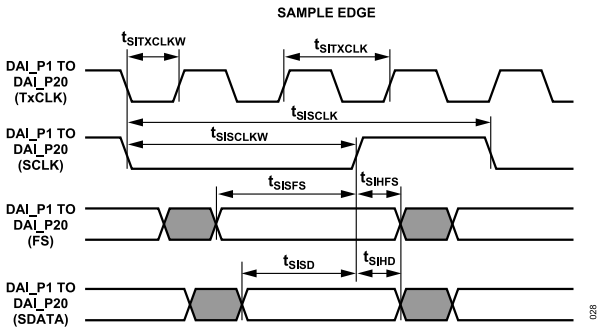


Figure 25. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

Table 28. Oversampling Clock (TxCLK) Switching Characteristics

Parameter	Max	Unit
Frequency for TxCLK = 384 × Frame Sync	Oversampling Ratio × Frame Sync ≤ $1/t_{SITXCLK}$	MHz
Frequency for TxCLK = 256 × Frame Sync	49.2	MHz
Frame Rate (FS)	192.0	kHz

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital PLL mode, the internal PLL (digital PLL) generates the 512 × FS clock.

Table 29. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter	Description	Min	Max	Unit
SWITCHING CHARACTERISTICS				
t_{DFSI}	Frame Sync Delay After Serial Clock		5	ns
t_{HOFSI}	Frame Sync Hold After Serial Clock	−2		ns
t_{DDTI}	Transmit Data Delay After Serial Clock		5	ns
t_{HDTI}	Transmit Data Hold After Serial Clock	−2		ns
t_{SCLKIW}[1]	Transmit Serial Clock Width	$8 \times t_{PCLK} - 2$		ns

[1] SCLK frequency is 64 × FS, where FS = the frequency of frame sync.

SPECIFICATIONS

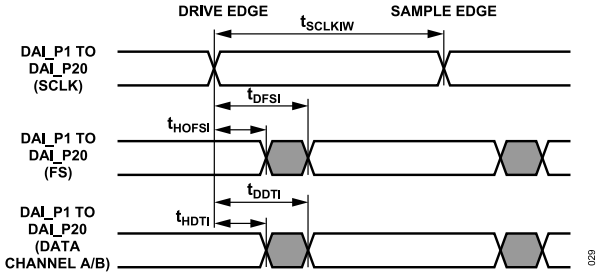


Figure 26. S/PDIF Receiver Internal Digital PLL Mode Timing

Serial Peripheral Interface (SPI)—Main

The ADSP1802 contains two SPI ports. The timing provided applies to both.

Table 30. SPI Interface Protocol—Main Switching and Timing Specifications

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	8.2		ns
t_{HSPIDM}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
SWITCHING CHARACTERISTICS				
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		2.5	ns
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	DPI Pin (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK Edge to DPI Pin (SPI Device Select) High	$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1.2$		ns

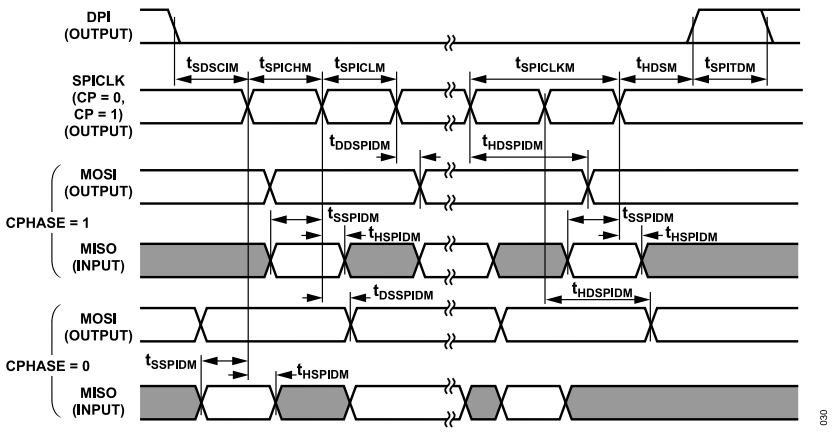


Figure 27. SPI Main Timing

SPI Interface—Subordinate

The processor contains two SPI ports. The timing provided applied to both.

Table 31. SPI Interface Protocol—Subordinate Switching and Timing Specifications

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				

SPECIFICATIONS

Table 31. SPI Interface Protocol—Subordinate Switching and Timing Specifications (Continued)

Parameter	Description	Min	Max	Unit
$t_{SPICLKS}$	Serial Clock Cycle	$4 \times t_{PCLK} - 2$		ns
t_{SPICHS}	Serial Clock High Period	$2 \times t_{PCLK} - 2$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{PCLK} - 2$		ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge, CPHASE = 0, CPHASE = 1	$2 \times t_{PCLK}$		ns
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0	$2 \times t_{PCLK}$		ns
t_{SSPIDS}	Data Input Valid to SPICLK edge (Data Input Setup Time)	2		ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE = 0)	$2 \times t_{PCLK}$		ns
SWITCHING CHARACTERISTICS				ns
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	0	7.5	ns
t_{DSOE}[1]	$\overline{SPIDS}$ Assertion to Data Out Active (SPI2)	0	7.5	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	0	10.5	ns
t_{DSDHI}[1]	$\overline{SPIDS}$ Deassertion to Data High Impedance (SPI2)	0	10.5	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Delay Time)		9.5	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Hold Time)	$2 \times t_{PCLK}$		ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$5 \times t_{PCLK}$	ns

[1] The timing for these parameters applies when the SPI is routed through the signal routing unit.

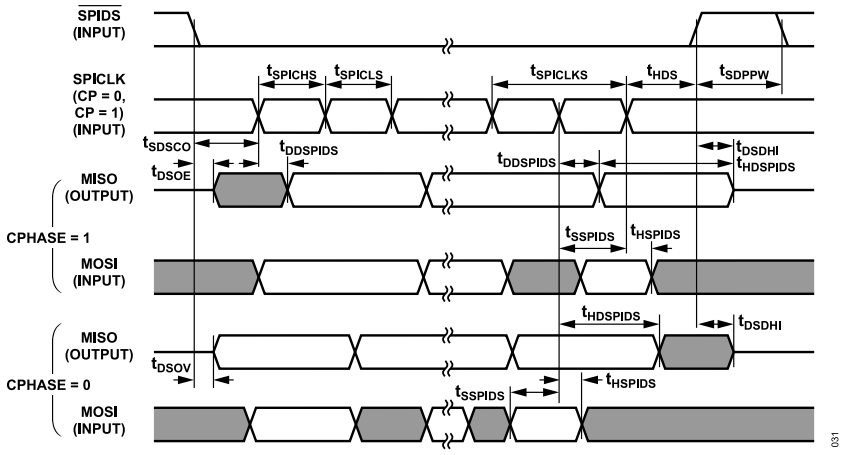


Figure 28. SPI Subordinate Timing

Joint Test Action Group (JTAG) Test Access Port and Emulation

Table 32. JTAG Test Access Port and Emulation

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width	$4 \times t_{CK}$		ns
SWITCHING CHARACTERISTICS				
t_{DTDO}	TDO Delay from TCK Low		10	ns

SPECIFICATIONS

Table 32. JTAG Test Access Port and Emulation (Continued)

Parameter	Description	Min	Max	Unit
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{TCK} \div 2 + 7$	ns

[1] System Inputs = CLK_CFG0, CLK_CFG1, $\overline{\text{RESET}}$, BOOT_CFG1 to BOOT_CFG0, DAI_Px, DPI_Px, and FLAG0 to FLAG3.

[2] System Outputs = DAI_Px, DPI_Px, FLAG0 to FLAG3, and $\overline{\text{EMU}}$.

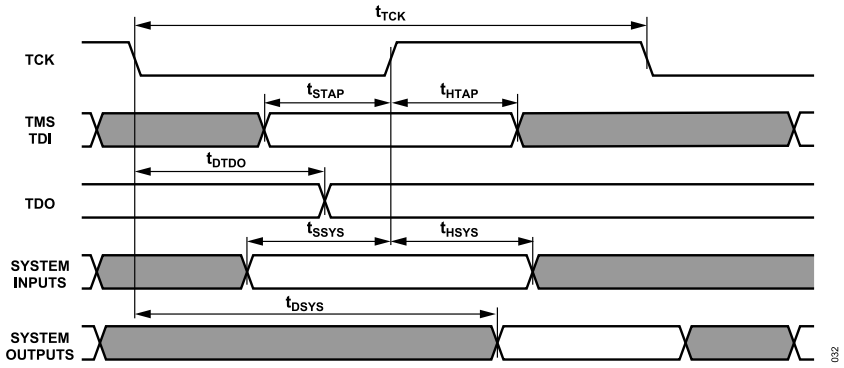


Figure 29. IEEE 1149.1 JTAG Test Access Port

THERMAL DIODE

The ADSP1802 incorporates a thermal diode to monitor the die temperature. The thermal diode is a grounded collector, PNP bipolar junction transistor (BJT). The THD_P pin is connected to the emitter and the THD_M pin is connected to the base of the transistor. These pins can be used by an external temperature sensor (such as the ADM1021A or LM86 or others) to read the die temperature of the chip.

The technique used by the external temperature sensor is to measure the change in V_{BE} when the thermal diode is operated at two different currents. This is shown in the following equation:

$$\Delta V_{BE} = n \times (kT \div q) \times ln(N) \quad (1)$$

where:
n = multiplication factor close to 1, depending on process variations.
k = Boltzmann constant.
T = temperature (°C).
q = charge of the electron.
N = ratio of the two currents.

The two currents are usually in the range of 10 mA to 300 mA for the common temperature sensor chips available.

Table 33 contains the thermal diode specifications using the transistor model.

Table 33. Thermal Diode Parameters – Transistor Model

Symbol[1]	Parameter	Min	Typ	Max	Unit
I_{FW}[2]	Forward Bias Current	10		300	µA
I_E	Emitter Current	10		300	µA
n_Q[3, 4]	Transistor Ideality	1.012	1.015	1.020	
R_T[3, 5]	Series Resistance	0.640	0.672	0.717	Ω

[1] See the Engineer-to-Engineer Note "Using the On-Chip Thermal Diode on Analog Devices Processors" (EE-346).

[2] Analog Devices does not recommend operation of the thermal diode under reverse bias.

[3] Specified by design characterization.

[4] The ideality factor, n_Q, represents the deviation from ideal diode behavior as exemplified by the diode equation: $I_C = I_S \times (e^{qVBE/nqkT} - 1)$ where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the diode, k = Boltzmann constant, and T = absolute temperature (Kelvin).

[5] The series resistance (R_T) can be used for more accurate readings as needed.

ABSOLUTE MAXIMUM RATINGS

Table 34. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DD_INT})	−0.3 V to +1.21 V
External (I/O) Supply Voltage (V_{DD_EXT})	−0.5 V to +3.6 V
Thermal Diode Supply Voltage (V_{DD_THD})	−0.5 V to +3.6 V
Input Voltage	−0.5 V to +3.6 V
Output Voltage Swing	−0.5 V to V_{DD_EXT} + 0.5 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

The ADSP1802 processor is rated for performance over the temperature range specified in the Operating Conditions section.

The JESD51 package thermal characteristics in this section are provided for package comparison and estimation purposes only. They are not intended for accurate system temperature calculation. System thermal simulation is required for accurate temperature analysis that accounts for all specific 3D system design features, including, but not limited to other heat sources, use of heatsinks, and the system enclosure. Contact Analog Devices for package thermal models that are intended for use with thermal simulation tools.

Table 35 shows the thermal characteristics values.

Table 35. Thermal Characteristics for 88-Lead LFCSP

Parameter	Typical	Unit
θ_{JA}	23	°C/W
θ_{JC}	8.4	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

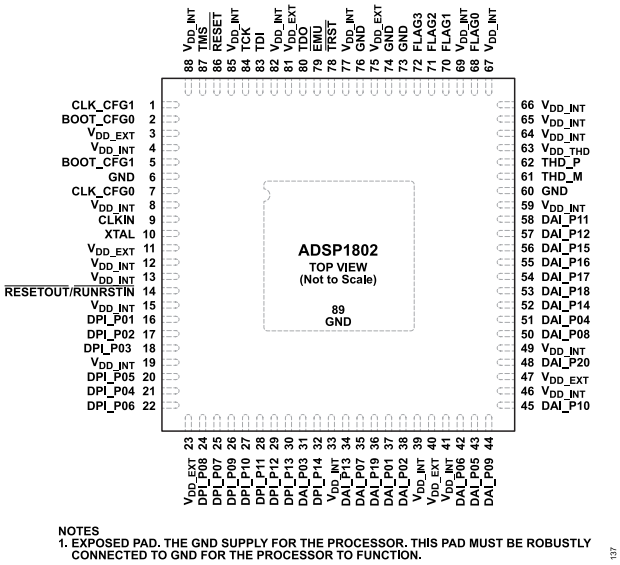


Figure 30. Pin Configuration

Table 36. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 7	CLK_CFG1, CLK_CFG0	I	Core to CLKIN Ratio Control. These pins set the startup clock frequency. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset. The allowed values are: 00 = 8:1, 01 = 32:1, 10 = 16:1, 11 = reserved.
2, 5	BOOT_CFG0, BOOT_CFG1	I	Boot Configuration Select. These pins select the boot mode for the processor. The BOOT_CFG pins must be valid before $\overline{\text{RESET}}$ (hardware and software) is asserted.
3, 11, 23, 40, 47, 75, 81	V_{DD_EXT}	P	I/O Power Supply.
4, 8, 12, 13, 15, 19, 33, 39, 41, 46, 49, 59, 64 to 67, 69, 77, 82, 85, 88	V_{DD_INT}	P	Internal Power Supply.
6, 60, 73, 74, 76	GND	G	Ground.
9	CLKIN	I	Local Clock In. Used in conjunction with XTAL. CLKIN is the clock input. It configures the processor to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processor to use the external clock source such as an external clock oscillator. CLKIN must not be halted, changed, or operated below specified frequency.
10	XTAL	O	Crystal Oscillator Terminal. Used in conjunction with CLKIN to drive an external crystal.
14	$\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$	I (IPU)	Reset Out/Running Reset In. The default setting on this pin is reset out. This pin also has a second function as $\overline{\text{RUNRSTIN}}$, which is enabled by setting bit 0 of the RUNRSTCTL register.
16 to 18[2], 20 to 22[2], 24 to 30[2], 32[2]	DPI_P01 to DPI_P14	I/O/T (IPU)	DPI. These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the output enable of the pin. The configuration registers of these peripherals then determine the exact behavior of the pin. Any input or output signal present in the DPI SRU can be routed to any of these pins.
31[2], 34 to 38[2], 42 to 45[2], 48, 50 to 58[2]	DAI_P01 to DAI_P20	I/O/T (IPU)	DAI. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audio centric peripheral inputs or outputs connected to the pin and to the output enable of the pin. The configuration registers of these peripherals then determine the exact behavior of the pin. Any signal present in the DAI SRU can be routed to any of these pins.
61	THD_M	O	Thermal Diode Cathode. When not used, this pin can be left floating.
62	THD_P	I	Thermal Diode Anode. When not used, this pin can be left floating.
63	V_{DD_THD}	P	Thermal Diode Power Supply. When not used, this pin can be left floating.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 36. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
68[3]	FLAG0	I/O (IPU)	FLAG0/Interrupt Request0.
70[4]	FLAG1	I/O (IPU)	FLAG1/Interrupt Request1
71[5]	FLAG2	I/O (IPU)	FLAG2/Interrupt Request2.
72[6]	FLAG3	I/O (IPU)	FLAG3/Timer Expired.
78	$\overline{\text{TRST}}$	I (IPU)	Test Reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor.
79[2]	$\overline{\text{EMU}}$	O (O/D, IPU)	Emulation Status. Must be connected to the Analog Devices DSP Tools product line of JTAG emulators target board connector only.
80[2]	TDO	O/T	Test Data Output (JTAG). Serial scan output of the boundary scan path.
83	TDI	I (IPU)	Test Data Input (JTAG). Provides serial data for the boundary scan logic.
84	TCK	I	Test Clock (JTAG). Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP1802.
86	$\overline{\text{RESET}}$	I	Processor Reset. Resets the processor to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
87	TMS	I (IPU)	Test Mode Select (JTAG). Used to control the test state machine.
89	EPAD	G	Exposed Pad. The GND supply for the processor. This pad must be robustly connected to GND for the processor to function.

[1] The following symbols appear in the type column of the table: A = asynchronous, I = input, O = output, S = synchronous, A/D = active drive, O/D = open drain, T = three-state, and IPU = internal pull-up resistor. The IPU resistors are designed to hold the internal path from the pins at the expected logic levels. To pull up the external pads to the expected logic levels, use external resistors. The IPU resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an IPU resistor can be between 27 kΩ to 65 kΩ. The three-state voltage of IPU pads cannot reach the full V_{DD_EXT} level. In this table, all pins are compliant with low voltage transistor-transistor logic (LVTTL) except for the thermal diode pins.

[2] State during/after reset: High-Z

[3] State during/after reset: FLAG [0] INPUT.

[4] State during/after reset: FLAG [1] INPUT.

[5] State during/after reset: FLAG [2] INPUT.

[6] State during/after reset: FLAG [3] INPUT.

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT DRIVE CURRENTS

The typical current vs. voltage characteristics for the output drivers of the ADSP1802 are shown in Figure 31. The pins associated include FLAG0 to FLAG3, $\overline{\text{EMU}}$, TDO, $\overline{\text{RESETOUT}}$, DPI1 to DPI14, and DAI1 to DAI20. The curves represent the current drive capability of the output drivers as a function of output voltage.

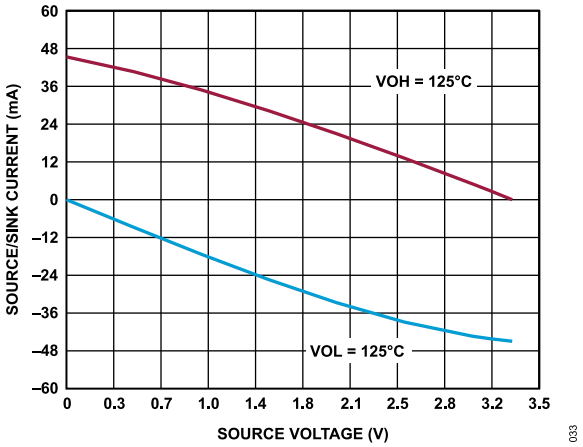


Figure 31. Typical Drive at Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

CAPACITIVE LOADING

Figure 32 and Figure 33 show the typical rise and fall time vs. load capacitance. Figure 34 and Figure 35 show graphically how output delays and holds vary with load capacitance.

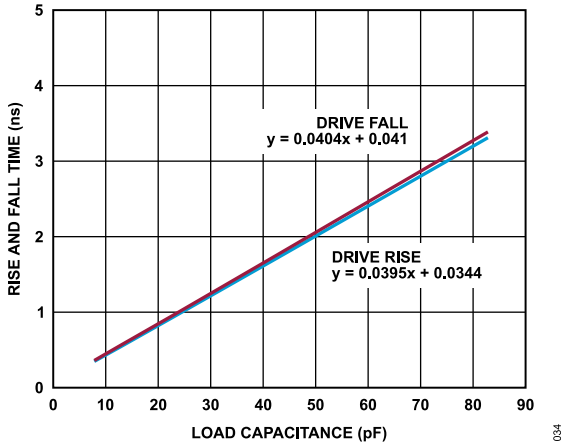


Figure 32. Typical Output Rise/Fall Time (30% to 70%, V_{DD_EXT} = Max)

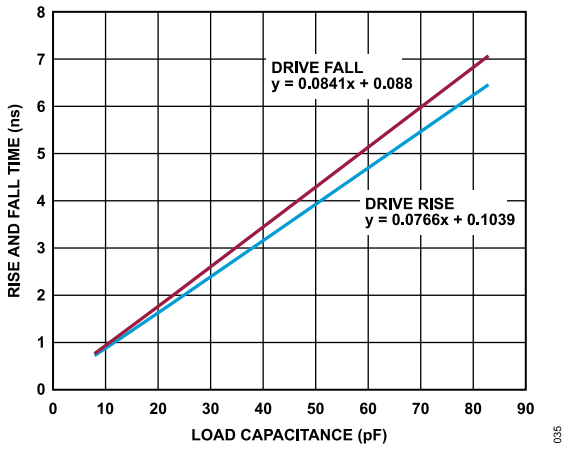


Figure 33. Typical Output Rise/Fall Time (30% to 70%, V_{DD_EXT} = Min)

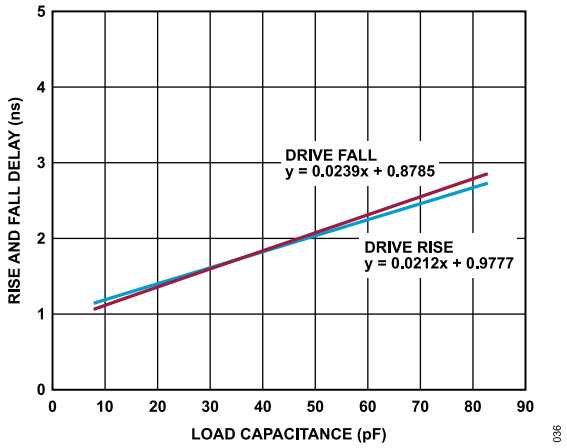


Figure 34. Typical Output Rise/Fall Delay (V_{DD_EXT} = Max)

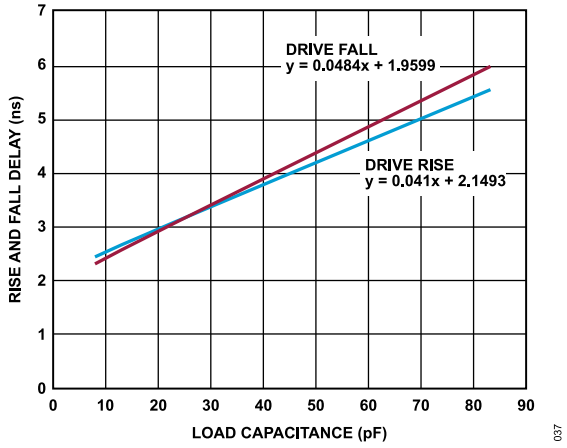


Figure 35. Typical Output Rise/Fall Delay (V_{DD_EXT} = Min)

THEORY OF OPERATION

Table 37 shows performance benchmarks for the ADSP1802 processor. Table 38 show the features of the ADSP1802.

Table 37. Processor Benchmarks (L1 RAM)

Benchmark Algorithm	Speed (At 400 MHz)
1024 Point Complex Fast Fourier Transform (FFT) (Radix 4, with Reversal)	23 µs
Finite Impulse Response (FIR) Filter (per Tap)[1]	1.25 ns
Infinite Impulse Response (IIR) Filter (per Biquad)[1]	5 ns
Matrix Multiply (Pipelined)	
[3 × 3] × [3 × 1]	11.25 ns
[4 × 4] × [4 × 1]	20 ns
Divide (y/x)	7.5 ns
Inverse Square Root	11.25 ns

[1] Assumes two files in multichannel single instruction, multiple data (SIMD) mode.

Table 38. ADSP1802 Features

Feature	ADSP1802
Maximum Instruction Rate	400 MHz
L1 RAM	5 Mb
L2 RAM	8 Mb
Max SPORTs Clock	50 MHz
Direct Memory Access (DMA) from SPORTs to L2 RAM	Yes
PWM	3 units
SPORTs	8 groups
FIR, IIR, FFT Accelerator	Yes
IDP/PDAP	Yes
Universal Asynchronous Receiver Transmitter (UART)	1
Flexible Signal Routing Unit (DAI SRU/(DPI SRU2)	Yes
S/PDIF Transceiver	Yes
SPI	2
Two Wire Interface (TWI)	1
SRC Performance	−140 dB
Thermal Diode	Yes
Variable Instruction Set Architecture (VISA) Support	Yes
Package	88-lead LFCSP

Figure 1 shows the two clock domains that make up the ADSP1802 processor. The core clock domain contains the following features:

- Two processing elements (PEx, PEy), each of which comprises an arithmetic/logic unit (ALU), multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- Program memory (PM) and data memory (DM) buses capable of supporting 2× 64-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (5 Mb), L2 RAM (8 Mb)
- JTAG test access port for emulation and boundary scan

The JTAG provides software debug through user breakpoints that allow flexible exception handling.

Figure 1 also shows the peripheral clock domain (also known as the I/O processor) that contains the following features:

- Peripheral DMA (IOD0) and external port DMA (IOD1) buses for 32-bit data transfers
- Peripheral and external port buses for core connection
- External port with an L2 RAM controller
- Three PWM units for PWM control
- One memory to memory (MTM) unit for internal to internal memory transfers
- DAI that includes four PCGs, an IDP/PDAP for serial and parallel interconnects, an S/PDIF receiver/transmitter, four asynchronous sample rate converters, eight SPORTs, and a DAI SRU
- DPI that includes two timers, a TWI, one UART, two SPIs, two PCGs, PWM, and a DPI SRU2

CORE CLOCK REQUIREMENTS

The ADSP1802 internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, the processor core, and the serial ports. During reset, program the ratio between the processor internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG0 and CLK_CFG1 pins.

The processor internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor internal clock.

THEORY OF OPERATION

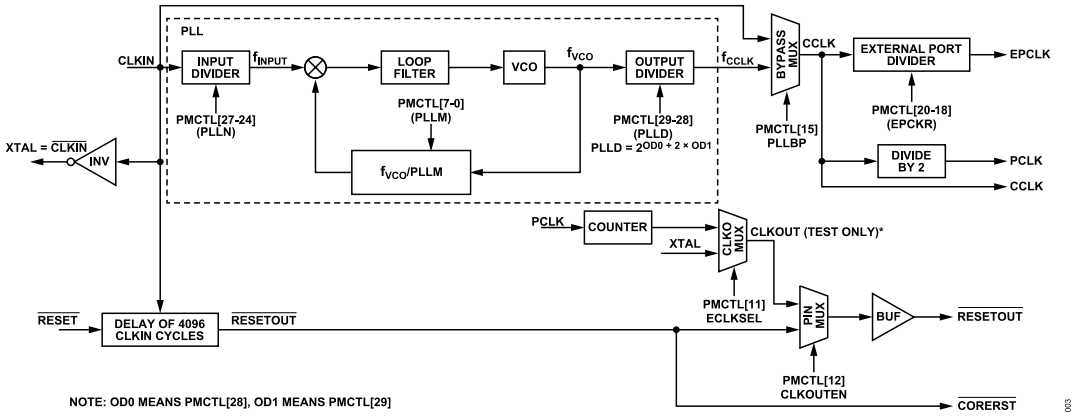


Figure 36. Core Clock and System Clock Relationship to CLKIN

Voltage Controlled Oscillator (VCO)

In application designs, the PLL multiplier value must be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in Table 11. The product of CLKIN, PLLN, and PLLM must never exceed f_{VCO} (max).

The PLL output frequency is calculated as follows:

$$f_{VCO} = f_{CCLKIN} \times PLLM \div PLLN \quad (2)$$

$$f_{CCLK} = f_{CCLKIN} \times PLLM \div PLLN \div PLLD \quad (3)$$

where:
f_{VCO} = VCO output.
PLLM = multiplier value programmed in the power management control (PMCTL) register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.
PLLN = input divider programmed in PMCTL register.
PLLD = output divider programmed in PMCTL register.

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in Table 39. All of the timing specifications for the ADSP1802 peripherals are defined in relation to t_{PCLK}. See the peripheral specific section for the timing information of each peripheral.

Table 39. Clock Periods

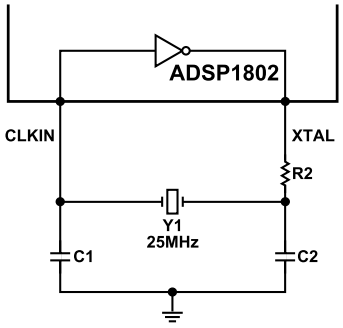
Timing Requirements	Description
t_{CK}	CLKIN Clock Period
t_{CCLK}	Processor Core Clock Period
t_{PCLK}	Peripheral Clock Period = 2 × t_{CCLK}
t_{EPCLK}	External Port Clock Period = (t_{CCLK}) × EPCKR

Figure 36 shows core to CLKIN relationships with external oscillator or crystal.

CLOCK SIGNALS

The ADSP1802 can use an external clock or a crystal. See the CLKIN pin description in Table 36. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL pins.

Figure 37 shows the component connections used for a crystal operating in fundamental mode. R2, C1, and C2 value can be chosen based on the crystal manufacturer specifications and the AN-1260 Application Note. Note that the clock rate is achieved using a 25 MHz crystal and a PLL multiplier ratio 16:1 (CCLK: CLKIN achieves a clock speed of 400 MHz).



NOTES:
1. CHOOSE C1 AND C2 BASED ON THE CRYSTAL Y1. R2 SHOULD BE CHOSEN TO LIMIT CRYSTAL DRIVE POWER. REFER TO CRYSTAL MANUFACTURER'S SPECIFICATIONS.

900

Figure 37. Recommended Circuit for Fundamental Mode Crystal Operation

THEORY OF OPERATION

CORE ARCHITECTURE

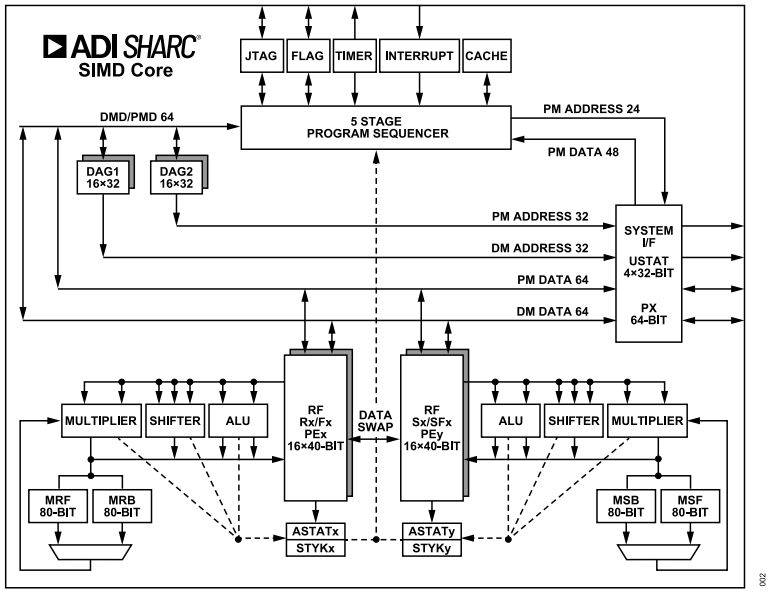


Figure 38. SHARC Core Block Diagram

SIMD Computational Engine

The ADSP1802 contains two computational processing elements that operate as an SIMD engine. The processing elements are referred to as PEx and PEy, and each contains an ALU, multiplier, shifter, and register file. PEx is always active, and PEy can be enabled by setting the PEYEN mode bit in the MODE1 register. SIMD mode allows the processor to execute the same instruction in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

SIMD mode also affects the way data is transferred between memory and the processing elements because twice the data bandwidth is required to sustain computational operation in the processing elements. Therefore, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each memory or register file access.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an ALU, multiplier and shifter. These units perform all operations in a single cycle and are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single precision floating point, 40-bit extended precision floating point, and 32-bit fixed point data formats.

Timer

The processor contains a core timer that can generate periodic software interrupts. The core timer can be configured to use FLAG3 as a timer expired signal.

Data Register File

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the enhanced Harvard architecture of the ADSP1802, allow unconstrained data flow between computation units and internal memory. The registers in PEx are referred to as R0 to R15 and in PEy as S0 to S15.

Context Switch

Many of the ADSP1802 registers have secondary registers that can be activated during interrupt servicing for a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result registers all have secondary registers. The primary registers are active at reset, while the secondary registers are activated by control bits in a mode control register.

Universal Registers

The universal registers can be used for general-purpose tasks. The USTAT (4) registers allow easy bit manipulations (set, clear, toggle, test, XOR) for all peripheral registers (control/status).

THEORY OF OPERATION

The data bus exchange register (PX) permits data to be passed between the 64-bit PM data bus and the 64-bit DM data bus, or between the 40-bit register file and the PM/DM data bus. These registers contain hardware to handle the data width difference.

Single Cycle Fetch of Instruction and Four Operands

The ADSP1802 features an enhanced Harvard architecture in which the DM bus transfers data and the PM bus transfers both instructions and data. With its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The processor includes an on-chip instruction cache that enables three bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data access are cached. This cache allows full speed execution of core, looped operations such as digital filter multiply accumulates, and FFT butterfly processing.

Data Address Generators With Zero Overhead Hardware Circular Buffer Support

The two DAGs are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing and are commonly used in digital filters and Fourier transforms.

The two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the processor can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory, all in a single instruction.

VISA

In addition to supporting the standard 48-bit instructions, the ADSP1802 supports new instructions of 16 bits and 32 bits. This feature, called VISA, drops redundant/unused bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from L1 RAM and L2 RAM. Source modules must be built using the VISA option, to allow code generation tools to create these more efficient opcodes.

On-Chip Memory

The ADSP1802 processor contain 5 Mb of internal RAM (see Table 40). The ADSP1802 supports 8 Mb L2 RAM. Each memory block supports single cycle, independent accesses by the core processor and I/O processor.

On-Chip Memory Bandwidth

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks (assuming there are no block conflicts). The total bandwidth is realized using the DMD (data memory data) and PMD (program memory data) buses (2 × 64-bit, CCLK speed) and the IOD0/IOD1 buses (2 × 32-bit, PCLK speed).

L1 RAM (5 Mb)

The SRAM of the ADSP1802 can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5 Mb. All the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that can be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM and PM buses, with one bus dedicated to a memory block, assures single cycle execution with two data transfers. In this case, the instruction must be available in the cache.

The memory maps in Table 40 display the internal memory address space of the processor. The 48-bit space section describes what this address range looks like to an instruction that retrieves 48-bit memory. The 32-bit section describes what this address range looks like to an instruction that retrieves 32-bit memory.

THEORY OF OPERATION

Table 40. Internal Memory Space (L1 RAM 5 Mb, IOP Register 0x0000 0000 to Register 0x0003 FFFF)

Long Word (LW, 64 Bits)	Extended Precision Normal or Instruction Word (INS, 48 Bits)	Normal Word (NW, 32 Bits)	Short Word (SW, 16 Bits)
Block 0 SRAM 0x0004 9000 to 0x0004 EFFF	Block 0 SRAM 0x0008 C000 to 0x0009 3FFF	Block 0 SRAM 0x0009 2000 to 0x0009 DFFF	Block 0 SRAM 0x0012 4000 to 0x0013 BFFF
Reserved 0x0004 F000 to 0x0004 FFFF	Reserved 0x0009 4000 to 0x0009 FFFF	Reserved 0x0009 E000 to 0x0009 FFFF	Reserved 0x0013 C000 to 0x0013 FFFF
Block 1 SRAM 0x0005 9000 to 0x0005 EFFF	Block 1 SRAM 0x000A C000 to 0x000B 3FFF	Block 1 SRAM 0x000B 2000 to 0x000B DFFF	Block 1 SRAM 0x0016 4000 to 0x0017 BFFF
Reserved 0x0005 F000 to 0x0005 FFFF	Reserved 0x000B 4000 to 0x000B FFFF	Reserved 0x000B E000 to 0x000B FFFF	Reserved 0x0017 C000 to 0x0017 FFFF
Block 2 SRAM 0x0006 0000 to 0x0006 3FFF	Block 2 SRAM 0x000C 0000 to 0x000C 5554	Block 2 SRAM 0x000C 0000 to 0x000C 7FFF	Block 2 SRAM 0x0018 0000 to 0x0018 FFFF
Reserved 0x0006 4000 to 0x0006 FFFF	Reserved 0x000C 5555 to 0x000D FFFF	Reserved 0x000C 8000 to 0x000D FFFF	Reserved 0x0019 0000 to 0x001B FFFF
Block 3 SRAM 0x0007 0000 to 0x0007 3FFF	Block 3 SRAM 0x000E 0000 to 0x000E 5554	Block 3 SRAM 0x000E 0000 to 0x000E 7FFF	Block 3 SRAM 0x001C 0000 to 0x001C FFFF
Reserved 0x0007 4000 to 0x0007 FFFF	Reserved 0x000E 5555 to 0x0000F FFFF	Reserved 0x000E 8000 to 0x000F FFFF	Reserved 0x001D 0000 to 0x001F FFFF

PERIPHERAL ARCHITECTURE

The ADSP1802 contains peripherals that support a wide variety of applications, including high quality audio, medical imaging, communications, military, test equipment, 3D graphics, speech recognition, motor control, general imaging, and other applications.

PWM

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine or audio power control. The PWM generator can generate either center aligned or edge aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in nonpaired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has three groups of four PWM outputs generating 12 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator can operate in two distinct modes while generating center aligned PWM waveforms: single update mode or double update mode. In single update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three phase PWM inverters.

PWM signals can be mapped to the DPI pins.

L2 RAM (8 Mb)

The external port interface supports access to the L2 memory through core and DMA accesses.

The L2 memory is used to expand on-chip memory capacity. The L2 memory is composed of RAM, and the total memory size is 8 Mb. It supports data or instruction access from the DSP core and DMA. The L2 memory is divided into two independent banks, which can be accessed in parallel by the DSP core and DMA.

The L2 memory supports the following features:

- Supports 8 Mb memory size.
- Divided into Bank 0 (4096 kb) and Bank 1 (4096 kb), which are accessed independently.
- Supports 32-bit, 48-bit, and 64-bit width data access from an external port data (EPD) bus, IOD1 bus, or serial port to external port (SPEP) bus.
- Supports instruction fetch only in Bank 0 of L2 memory for instruction set architecture (ISA) and VISA operation, Bank 0 and Bank 1 can both store data.
- Supports SIMD access in normal word addressing space.

The L2 memory supports three access types, which are normal word (NW, 32-bit width), long word (LW, 64-bit width), and instructions (INS, 48-bit width).

The access types of the four ways accessing Bank 0 and Bank 1 are shown in Table 41.

THEORY OF OPERATION

Table 41. Access Data Type

	Core			SPORTs DMA	EPDMA0/1
Bank	**LW**	**INS**	**NW**	**NW**	**NW**
Bank 0	Read/ Write	Read	Read/ Write	Read/Write	Read/Write
Bank 1	Read/ Write	N/A	Read/ Write	Read/Write	Read/Write

The L2 RAM address space is shown in Table 42.

Table 42. Memory Space

Bank	Size in NW	Address Range in NW
Bank 0	128k	0x0020 0000 to 0x0021 FFFF
Bank 1	128k	0x0400 0000 to 0x0401 FFFF

SIMD Access to L2 RAM

The ADSP1802 supports SIMD access on the 64-bit EPD bus, which allows access to the complementary registers on the PEy unit in the NW space.

VISA and ISA Access to L2 RAM

The ADSP1802 supports VISA code operation, which reduces the memory load because the VISA instructions are compressed. Moreover, bus fetching is reduced because, in the best case, one 48-bit fetch contains three valid instructions. Code execution from the traditional ISA operation is also supported. Note that code execution is only supported from Bank 0 regardless of VISA/ISA. Table 43 shows the address ranges for instruction fetch in each mode.

Table 43. Bank 0 Instruction Fetch in L2 RAM

Access Type	Address Range in NW
NW	0x0020 0000 to 0x0021 FFFF (ISA)
Short Word (SW)	0x0060 0000 to 0x0063 FFFF (VISA)

DAI

The DAI allows the connection of various peripherals to any of the DAI pins (DAI_P01 to DAI_P20). Programs make these connections using the DAI SRU.

The DAI SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes eight SPORTs, four PCGs, a S/PDIF transceiver, four ASRCs, and an IDP. The IDP provides an additional input path to the SHARC core, configurable as either eight channels of serial data, or a single 20-bit wide synchronous PDAP. Each data channel has its own DMA channel that is independent from the SPORTs of the ADSP1802.

SPORTs

The ADSP1802 features eight synchronous SPORTs that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as the Analog Devices AD183x family of audio codecs, ADCs, and DACs. The SPORTs consist of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

SPORTs can support up to 16 transmit or 16 receive DMA channels of audio data when all eight SPORTs are enabled, or four full duplex time division multiplexing (TDM) streams of 128 channels per frame.

SPORT data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the SPORTs can work in conjunction with another SPORT to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides two receive signals. The frame sync and clock are shared.

If an external clock is provided as the source of the SPORT frame sync and SCLK, the ASRC must be used, or the DSP core clock must be synchronous with the external clock.

SPORTs operate in five modes as follows:

- Standard serial mode
- Multichannel/TDM mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

S/PDIF-Compatible Digital Audio Receiver/ Transmitter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left-justified, I^2S or right-justified with word widths of 16 bits, 18 bits, 20 bits, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the SRU. They can come from a variety of sources, such as the SPORTs, external pins, or PCGs, and are controlled by the SRU control registers.

ASRC

The ASRC contains four SRC blocks and provides up to −140 dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches.

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Lastly, the SRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

IDP

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I^2S, left-justified sample pair, or right-justified mode.

The IDP also provides a PDAP, which can be used for receiving parallel data. The PDAP has a clock input and a hold input. The data for the PDAP can be received from DAI pins or from the external port pins. The PDAP supports a maximum of 20-bit data and four different packing modes to receive the incoming data.

PCGs

The PCGs consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A B, C, and D, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

The outputs of PCG A and PCG B can be routed through the DAI pins. The outputs of PCG C and PCG D can be driven on to the DAI as well as the DPI pins.

DPI

The ADSP1802 has a DPI that provides connections to two SPI ports, one UART, 12 flags, a TWI, three PWM modules (PWM1 to PWM3), and two general-purpose timers.

SPI

The SPI is an industry-standard synchronous serial link that enables the SPI-compatible port to communicate with other SPI-compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full duplex synchronous serial interface that supports both main and subordinator modes. The SPI port can operate in a multi main environment by interfacing with up to four other SPI-compatible devices, either acting as a main or subordinator device. The SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The SPI-compatible port uses open drain drivers to support a multi-main configuration and to avoid data contention.

UART Port

The ADSP1802 provides a full duplex UART port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation as follows:

- Programmed I/O (PIO)—The processor sends or receives data by writing or reading I/O mapped UART registers. The data is double buffered on both transmit and receive.
- DMA—The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

Timers

The ADSP1802 has a total of three timers: a core timer that can generate periodic software interrupts, and two general-purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes as follows:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

The core timer can be configured to use FLAG3 as a timer expired signal, and the general-purpose timers have one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables the general-purpose timer.

TWI

The TWI is a bidirectional 2-wire, serial bus used to move 8-bit data while maintaining compliance with the I^2C bus protocol. The TWI controller incorporates the following features:

- 7-bit addressing
- Simultaneous main and subordinate operation on multiple device systems with support for multi main data arbitration
- Digital filtering and timed event processing
- 100 kbps and 400 kbps data rates
- Low interrupt rate

I/O PROCESSOR FEATURES

The I/O processor provides up to 34 channels of DMA, as well as an extensive set of peripherals.

DMA Controller

The on-chip DMA controller of the ADSP1802 allows data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA

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operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the internal memory, SPORTs, SPI ports, IDP, PDAP, or the UART port of the ADSP1802. The DMA channel summary is shown in Table 44.

Programs can be downloaded to the ADSP1802 using DMA transfers. Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

Table 44. DMA Channels

Peripheral	DMA Channels
SPORTs	16
IDP/PDAP	8
SPI	2
UART	2
External Port	2
Accelerators	2
MTM	2

FFT Accelerator

The FFT accelerator implements a radix two complex/real input, complex output FFT with no core intervention. The FFT accelerator runs at the peripheral clock frequency.

FIR Accelerator

The FIR accelerator consists of a 1024 words coefficient memory, a 1024 words deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency.

IIR Accelerator

The IIR accelerator consists of a 1440 words coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data, and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency.

APPLICATIONS INFORMATION

SYSTEM DESIGN

The following sections introduce system design options and power supply issues.

Program Booting

The internal memory of the ADSP1802 boots at system power-up from an SPI main or SPI subordinate.

Table 45. Boot Mode Selection

BOOT_CFG1 to BOOT_CFG0	Booting Mode
00	SPI Subordinate Boot
01	SPI Main Boot
10	Reserved
11	Reserved

The running reset feature allows a user to perform a reset of the processor core and peripherals, but without resetting the PLL or performing a boot. The functionality of the $\overline{\text{RESETOUT}}/\overline{\text{RUNRSTIN}}$ pin also extends to acting as the input for initiating a running reset.

Power Supplies

The ADSP1802 has separate power supply connections for the internal (V_{DD_INT}) and external (V_{DD_EXT}) power supplies. The internal power supply must meet the V_{DD_INT} specifications. The external power supply must meet the V_{DD_EXT} specifications. All external power supply pins must be connected to the same power supply.

To reduce noise coupling, the PCB must use a parallel pair of power and ground planes for V_{DD_INT} and GND.

Target Board JTAG Emulator Connector

The Analog Devices SHARC DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP1802 to monitor and control the target board processor during emulation. The Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The JTAG interface of the ADSP1802 ensures that the emulator cannot affect target system loading or timing.

For complete information on the Analog Devices SHARC DSP Tools product line of JTAG emulator operation, see the appropriate emulator hardware user guide.

SURFACE-MOUNT DESIGN

The exposed pad is required to be electrically and thermally connected to GND. Implement this by soldering the exposed pad to a GND PCB land that is the same size as the exposed pad. The GND PCB land must be robustly connected to the GND plane in the PCB for best electrical and thermal performance. No separate GND pins are provided in the package.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments, CrossCore® Embedded Studio, evaluation products, emulators, and a wide variety of software addins.

OUTLINE DIMENSIONS

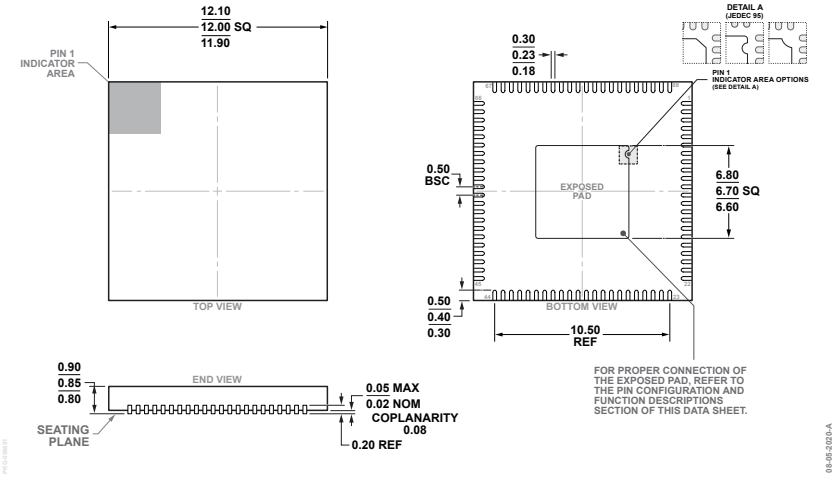

Figure 39. 88-Lead Lead Frame Chip Scale Package [LFCSP]
12 × 12 mm Body and 0.85 mm Package Height
(CP-88-11)
Dimensions shown in millimeters

Updated: April 12, 2024

ORDERING GUIDE

Model[1, 2]	Temperature Range[3]	Package Description	Packing Quantity	Package Option
ADSP1802KCPZ400-RL	0°C to +105°C	88-lead LFCSP (12 mm x 12 mm x 0.85 mm)	Reel, 2000	CP-88-11
ADSP1802WBCPZ400-RL	−40°C to +125°C	88-lead LFCSP (12 mm x 12 mm x 0.85 mm)	Reel, 2000	CP-88-11
ADSP1802WBCPZ400	−40°C to +125°C	88-lead LFCSP (12 mm x 12 mm x 0.85 mm)	Tray, 168	CP-88-11

1 Z = RoHS Compliant Part.

2 W = Qualified for Automotive Applications.

3 Referenced temperature is junction temperature. See the Operating Conditions section for junction temperature (T_J) specification.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADSP1802EBZ	Evaluation Board

1 Z = RoHS Compliant Part.

AUTOMOTIVE PRODUCTS

The ADSP1802W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial model, therefore, designers must review the Specifications section of this data sheet carefully. Only the automotive grade product shown is available for use in automotive applications. Contact the local Analog Devices, Inc., account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for this model.

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