

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-CAT25M01

EEPROM Serial 1-Mb SPI

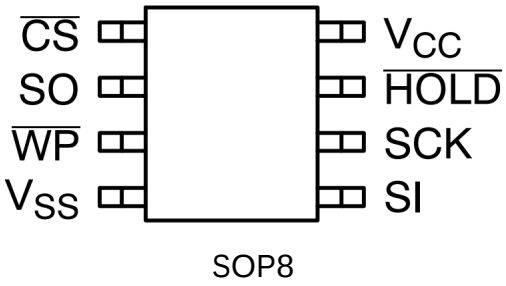
网址 www.sztdbdt.com

用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features



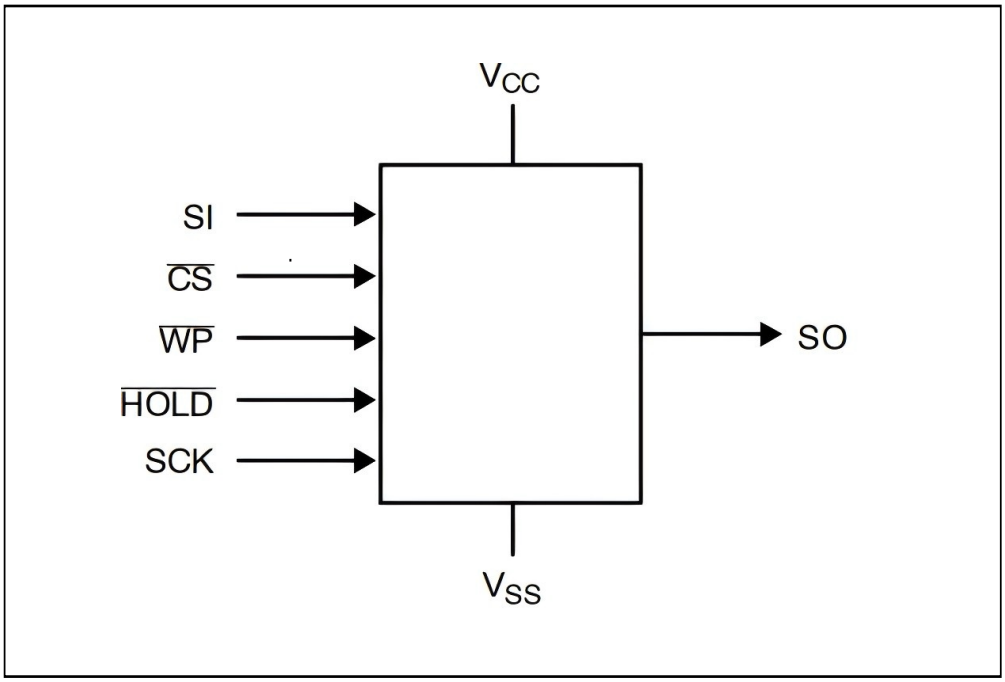
SOP8

- 10 MHz SPI Compatible
- 1.8 V to 5.5 V Supply Voltage Range
- SPI Modes (0,0) & (1,1)
- 256-byte Page Write Buffer
- Additional Identification Page with Permanent Write Protection
- Self-timed Write Cycle
- Hardware and Software Protection
- Block Write Protection – Protect 1/4, 1/2 or Entire EEPROM Array
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- 8 lead SOIC Package
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

Description

The CAT25M01 is a EEPROM Serial 1_Mb SPI device internally organized as 128Kx8 bits. This features a 256-byte page write buffer and supports the Serial Peripheral Interface (SPI) protocol. The device is enabled through a Chip Select (CS) input. In addition, the required bus signals are clock input (SCK), data input (SI) and data output (SO) lines. The HOLD input may be used to pause any serial communication with the CAT25M01 device. The device features software and hardware write protection, including partial as well as full array protection.
On-Chip ECC (Error Correction Code) makes the device suitable for high reliabilityapplications.

Figure 1. Functional Symbol



PIN FUNCTION

Pin Name	Function
CS	Chip Select
SO	Serial Data Output
WP	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock
HOLD	Hold Transmission Input
V_{CC}	Power Supply

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Ratings	Units
Operating Temperature	-45 to +130	℃
Storage Temperature	-65 to +150	℃
Voltage on any Pin with Respect to Ground (Note 1)	-0.5 to +6.5	V

Note：1. The DC input voltage on any pin should not be lower than -0.5 V or higher than VCC + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than VCC + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END}(Note 3)	Endurance	1,000,000	Program/Erase Cycles
T_{DR}	Data Retention	100	Years

Note：2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
3. Page Mode, VCC = 5 V, 25 ° C
4. The device uses ECC (Error Correction Code) logic with 6 ECC bits to correct one bit error in 4 data bytes. Therefore, when a single byte has to be written, 4 bytes (including the ECC bits) are re?programmed. It is recommended to write by multiple of 4 bytes in order to benefit from the maximum number of write cycles.

Table 3. D. C. OPERATING CHARACTERISTICS

(V_{CC} = 1.8 V to 5.5 V, T_A = -40 ° C to +85 ° C and V_{CC} = 2.5 V to 5.5 V, T_A =-40 ° C to +125 ° C, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CCR}	Supply Current (Read Mode)	Read,SO open / -40°C to +85°C	V_{cc}=1.8V,f_{SCK}=5 MHz		1.2	mA
			V_{cc}=2.5 V,f_{SCK}=10 MHz		1.8	mA
			V_{cc}=5.5 V,f_{SCK}=10 MHz		3	mA
		Read,SO open/ -40°C to+125°C	2.5V<V_{cc}<5.5 V, f_{SCK}=10 MHz		3	mA
Iccw	Supply Current (Write Mode)	Write,CS=V_{CC}/ -40°C to +85°C	1.8V<V_{cc}<5.5V		3	mA
		Write,CS=V_{cc}/ -40°C to +125°C	2.5V<V_{cc}<5.5V		3	mA

Table 3. D. C. OPERATING CHARACTERISTICS Continued

(V_{CC} = 1.8 V to 5.5 V, T_A = -40 ° C to +85 ° C and V_{CC} = 2.5 V to 5.5 V, T_A =-40 ° C to +125 ° C, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{SB1}	Standby Current	V_{IN}=GND or V_{cc}, CS=V_{cc},WP=V_{cc}, HOLD=V_{cc},V_{cc}=5.5V	T_A=-40℃ to+85℃		1	μA
			T_A=-40℃ to+125℃		3	
I_{SB2}	Standby Current	V_{IN}=GND or V_{cc}, CS=V_{cc},WP=GND, HOLD=GND, V_{cc}=5.5V	T_A=-40℃ to+85℃		3	μA
			T_A=-40℃ to+125℃		5	μA
I_L	Input Leakage Current	V_{IN}=GND or V_{cc}		-2	2	μA
I_{LO}	Output Leakage Current	CS=V_{cc} V_{OUT} =GND or V_{cc}		-2	2	μA
V_{IL1}	Input Low Voltage	V_{cc}≥2.5V		-0.5	0.3V_{cc}	V
V_{IH1}	Input High Voltage	V_{cc}≥2.5V		0.7V_{cc}	V_{cc}+0.5	V
V_{IL2}	Input Low Voltage	V_{cc}<2.5V		-0.5	0.25V_{cc}	V
V_{IH2}	Input High Voltage	V_{cc}<2.5V		0.75V_{cc}	V_{cc}+0.5	V
V_{OL1}	Output Low Voltage	V_{cc}≥2.5V,I_{OL}=3.0 mA			0.4	V
V_{OH1}	Output High Voltage	V_{cc}≥2.5 V,I_{OH}=-1.6mA		V_{cc} -0.8V		V
V_{OL2}	Output Low Voltage	V_{cc}<2.5 V,I_{OL}=150 μA			0.2	V
V_{OH2}	Output High Voltage	V_{cc}<2.5V,I_{OH}=-100 μA		V_{cc}-0.2V		V

Table 4. PIN CAPACITANCE

(T_A = 25 ° C, f = 1.0 MHz, V_{CC} = +5.0 V) (Note 5)

Symbol	Test	Conditions	Min	Typ	Max	Units
C_{OUT}	Output Capacitance (SO)	V_{OUT}=0V			8	pF
C_{IN}	Input Capacitance(CS,SCK,SI,WP,HOLD)	V_{IN}=0V			8	pF

Note：5. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

Table 5. A.C. CHARACTERISTICS

(T_A = -40 ° C to +125 ° C, unless otherwise specified.) (Note 6)

Symbol	Parameter	V_{CC}=1.8V-5.5V -40℃ to +85℃		V_{CC} = 2.5 V -5.5 V -40℃ to +125℃		Units
		Min	Max	Min	Max	
f_{SCK}	Clock Frequency	DC	5	DC	10	MHz
t_{su}	Data Setup Time	20		10		ns
t_H	Data Hold Time	20		10		ns
t_{WH}	SCK High Time	75		40		ns
t_{WL}	SCK Low Time	75		40		ns
t_{LZ}	HOLD to Output Low Z		50		25	ns
t_{RI}(Note 8)	Input Rise Time		2		2	μs
t_{FI}(Note 8)	Input FallTime		2		2	μs
t_{HD}	HOLD Setup Time	0		0		ns
t_{CD}	HOLD Hold Time	10		10		ns
t_v	Output Valid from Clock Low		75		40	ns
t_{HO}	Output Hold Time	0		0		ns
t_{DIS}	Output Disable Time		50		20	ns
t_{HZ}	HOLD to Output High Z		100		25	ns
t_{cs}	CS High Time	80		40		ns
t_{css}	CS Setup Time	60		30		ns
t_{CSH}	CS Hold Time	60		30		ns
t_{CNS}	CS Inactive Setup Time	60		30		
t_{CNH}	CS Inactive Hold Time	60		30		
t_{WPS}	WP Setup Time	10		10		ns
t_{WPH}	WP Hold Time	10		10		ns
t_{wc}(Note 7)	Write Cycle Time		5		5	ms

Note：6. AC Test Conditions:
Input Pulse Voltages: 0.3 VCC to 0.7 VCC
Input rise and fall times: ≤ 10 ns
Input and output reference voltages: 0.5 VCC
Output load: current source IOL max/IOH max; CL = 30 pF
7. tWC is the time from the rising edge of CS after a valid write sequence to the end of the internal write cycle.

Table 6. POWER_UP TIMING (Notes 8 and 9)

Symbol	Parameter	Max	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{puw}	Power-up to Write Operation	1	ms

Note：8. This parameter is tested initially and after a design or process change that affects the parameter.
9. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Pin Description

SI: The serial data input pin accepts op_codes, addresses and data. In SPI modes (0,0) and (1,1) input data is latched on the rising edge of the SCK clock input.
SO: The serial data output pin is used to transfer data out of the device. In SPI modes (0,0) and (1,1) data is shifted out on the falling edge of the SCK clock.
SCK: The serial clock input pin accepts the clock provided by the host and used for synchronizing communication between host and CAT25M01.
CS: The chip select input pin is used to enable/disable the CAT25M01. When CS is high, the SO output is tri_stated (high impedance) and the device is in Standby Mode (unless an internal write operation is in progress). Every communication session between host and CAT25M01 must be preceded by a high to low transition and concluded with a low to high transition of the CS input.
WP: The write protect input pin will allow all write operations to the device when held high. When WP pin is tied low and the WPEN bit in the Status Register (refer to Status Register description, later in this Data Sheet) is set to “1”, writing to the Status Register is disabled.
HOLD: The HOLD input pin is used to pause transmission between host and CAT25M01, without having to retransmit the entire sequence at a later time. To pause, HOLD must be taken low and to resume it must be taken back high, with the SCK input low during both transitions. When not used for pausing, it is recommended the HOLD input to be tied to V_{CC}, either directly or through a resistor.

Functional Description

The CAT25M01 device supports the Serial Peripheral Interface (SPI) bus protocol, modes (0,0) and (1,1). The device contains an 8_bit instruction register. The instruction set and associated op_codes are listed in Table 7.
Reading data stored in the CAT25M01 is accomplished by simply providing the READ command and an address. Writing to the CAT25M01, in addition to a WRITE command, address and data, also requires enabling the device for writing by first setting certain bits in a Status Register, as will be explained later.
After a high to low transition on the CS input pin, the CAT25M01 will accept any one of the six instruction op_codes listed in Table 7 and will ignore all other possible 8_bit combinations. The communication protocol follows the timing from Figure 2.

The CAT25M01 features an additional Identification Page (256 bytes) which can be accessed for Read and Write operations when the IPL bit from the Status Register is set to “ 1 ”. The user can also choose to make the Identification Page permanent write protected.

Table 7. INSTRUCTION SET

Instruction	Opcode	Operation
WREN	00000110	Enable Write Operations
WRDI	00000100	Disable Write Operations
RDSR	00000101	Read Status Register
WRSR	00000001	Write Status Register
READ	00000011	Read Data from Memory
WRITE	00000010	Write Data to Memory

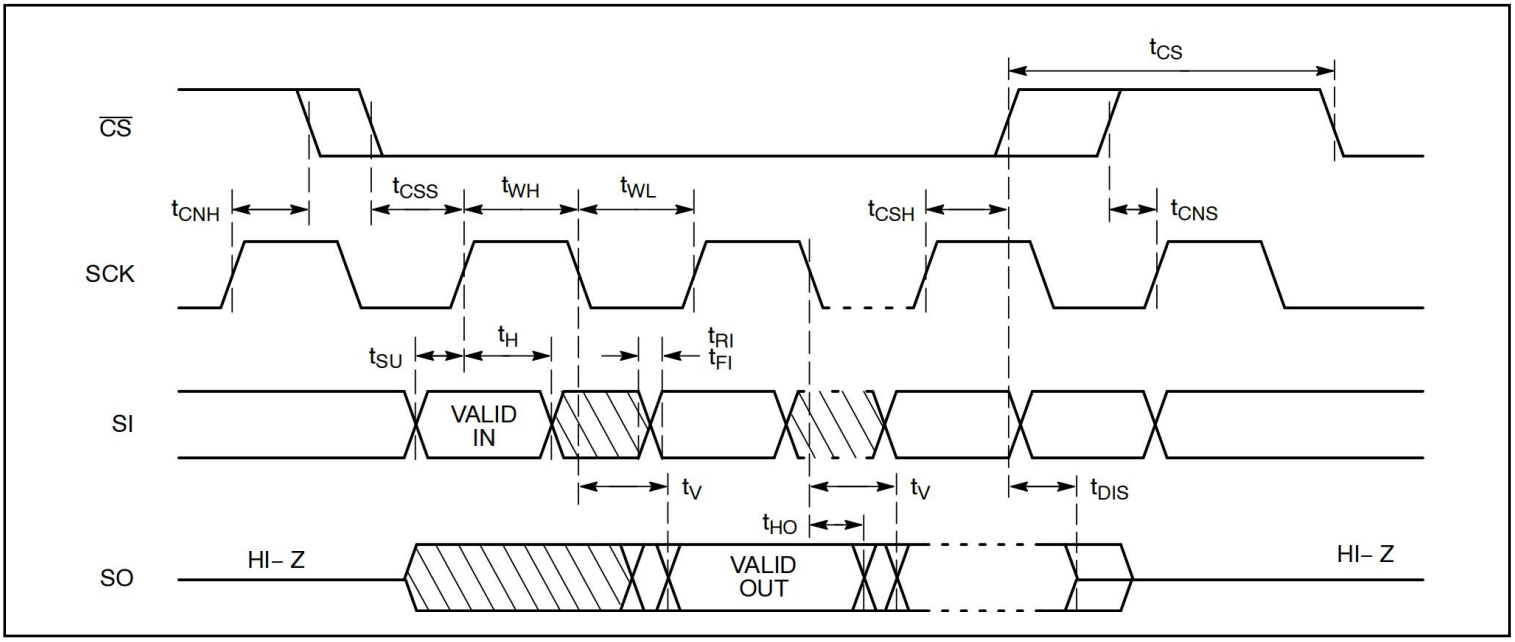


Figure 2. Synchronous Data Timing

Status Register

The Status Register, as shown in Table 8, contains a number of status and control bits.
The RDY (Ready) bit indicates whether the device is busy with a write operation. This bit is automatically set to 1 during an internal write cycle, and reset to 0 when the device is ready to accept commands. For the host, this bit is read only.

The WEL (Write Enable Latch) bit is set/reset by the WREN/WRDI commands. When set to 1, the device is in a Write Enable state and when set to 0, the device is in a Write Disable state.
The BP0 and BP1 (Block Protect) bits determine which blocks are currently write protected. They are set by the user with the WRSR command and are non_volatile. The user is allowed to protect a quarter, one half or the entire memory, by setting these bits according to Table 9. The protected blocks then become read_only.
The WPEN (Write Protect Enable) bit acts as an enable for the WP pin. Hardware write protection is enabled when the WP pin is low and the WPEN bit is 1. This condition prevents writing to the status register and to the block protected sections of memory. While hardware write protection is active, only the non_block protected memory can be written. Hardware write protection is disabled when the WP pin is high or the WPEN bit is 0. The WPEN bit, WP pin and WEL bit combine to either permit or inhibit Write operations, as detailed in Table 10.
The IPL (Identification Page Latch) bit determines whether the additional Identification Page (IPL = 1) or main memory array (IPL = 0) can be accessed both for Read and Write operations. The IPL bit is set by the user with the WRSR command and is volatile. The IPL bit is automatically reset after read/write operations.
The LIP bit is set by the user with the WRSR command and is non_volatile. When set to 1, the Identification Page is permanently write protected (locked in Read_only mode).

Note: The IPL and LIP bits cannot be set to 1 using the same WRSR instruction. If the user attempts to set (“ 1 ”) both the IPL and LIP bit in the same time, these bits cannot be written and therefore they will remain unchanged.

Table 8. STATUS REGISTER

7	6	5	4	3	2	1	0
WPEN	IPL	0	LIP	BP1	BP0	WEL	RDY

Table 9. BLOCK PROTECTION BITS

Status Register Bits		Array Address Protected	Protection
BP1	BP0		
0	0	None	No Protection
0	1	18000h-1FFFFh	Quarter Array Protection
1	0	10000h-1FFFFh	Half Array Protection
1	1	00000h-1FFFFh	FullArray Protection

Table 10. WRITE PROTECT CONDITIONS

WPEN	WP	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

Write Operations：The CAT25M01 device powers up into a write disable state. The device contains a Write EnableLatch (WEL) which must be set before attempting to write to the memory array or to the status register. In addition, the address of the memory location(s) to be written must be outside the protected area, as defined by BP0 and BP1 bits from the status register.

Write Enable and Write Disable：The internal Write Enable Latch and the correspon – ding Status Register WEL bit are set bysending the WREN instruction to the CAT25M01. Care must be taken to take the CS input high after the WREN instruction, as otherwise the Write Enable Latch will not be properly set. WREN timing is illustrated in Figure 3. The WREN instruction must be sent prior any WRITE or WRSR instruction. The internal write enable latch is reset by sending the WRDI instruction as shown in Figure 4. Disabling write operations by resetting the WEL bit, will protect the device against inadvertent writes.

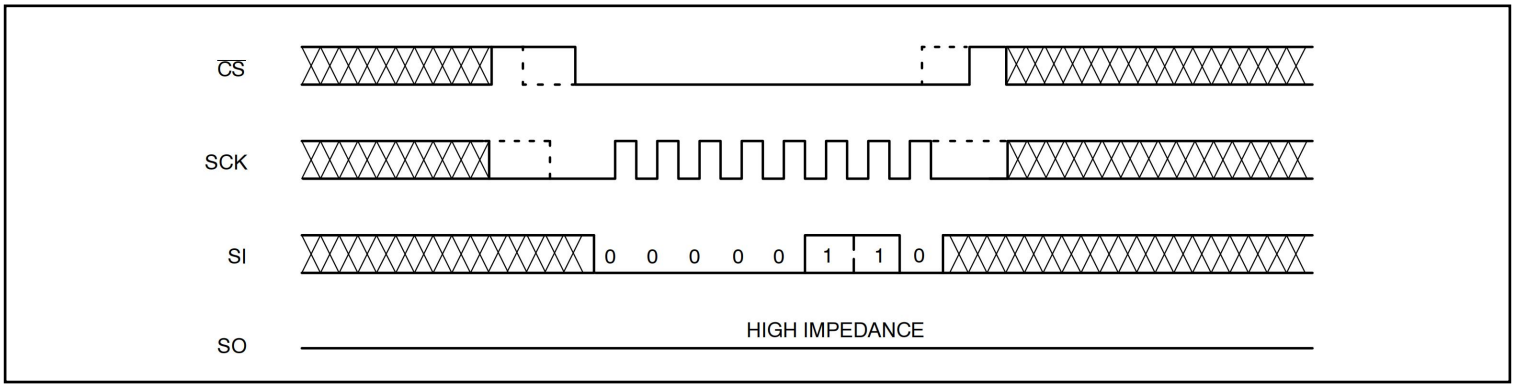


Figure 3. WREN Timing

Note: Dashed Line = mode (1, 1)

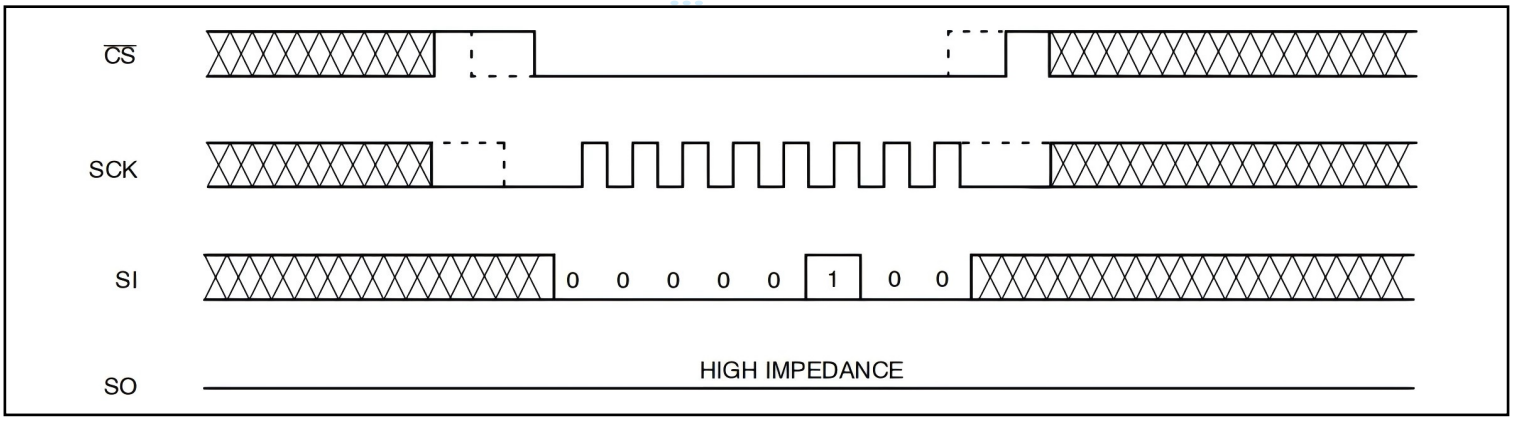


Figure 4. WRDI Timing

Note: Dashed Line = mode (1, 1)

Byte Write：Once the WEL bit is set, the user may execute a write sequence, by sending a WRITE instruction, a24_bit address and a data byte as shown in Figure 5. Only 17 significant address bits are used bythe CAT25M01. The rest are don ' t care bits, as shown in Table 11. Internal programming will start after the low to high CS transition. During an internal write cycle, all commands, except for RDSR (Read Status Register) will be ignored. The RDY bit will indicate if the internal write cycle is in progress (RDY high), or the device is ready to accept commands (RDY low).

Page Write：After sending the first data byte to the CAT25M01, the host may continue sending data, up to a total of 256 bytes, according to timing shown in Figure 6. After each data byte, the lower order address bits are automatically incremented, while the higher order address bits (page address) remain unchanged. If during this process the end of page is exceeded, then loading will " roll over " to the first byte in the page, thus possibly overwriting previoualy loaded data. Following completion of the write cycle, the CAT25M01 is automatically returned to the write disable state.

Write Identification Page：The additional 256_byte Identification Page (IP) can be written with user data using the same Write commands sequence as used for Page Write to the main memory array (Figure 6). The address bits [A23:A8] are Don ' t Care and the [A7:A0] bits define the byte address within theIdentification Page. In addition, the Byte Address must point to a location outside the protected area defined by the BP1, BP0 bits from the Status Register. When the full memory array is write protected (BP1, BP0 = 1,1), the write instruction to the IP is not accepted and not executed. Also, the write to the IP is not accepted if the LIP bit from the Status Register is set to 1 (the pageis locked in Read_only mode).

*The IPL bit from the Status Register must be set (IPL = 1) using the WRSR instruction, before attempting to write to the IP.

Table 11. BYTE ADDRESS

Device	Address Significant Bits	Address Don't Care Bits	#Address Clock Pulses
Main Memory Array	A16-A0	A23-A17	24
Identification Page	A7-A0	A23-A8	24

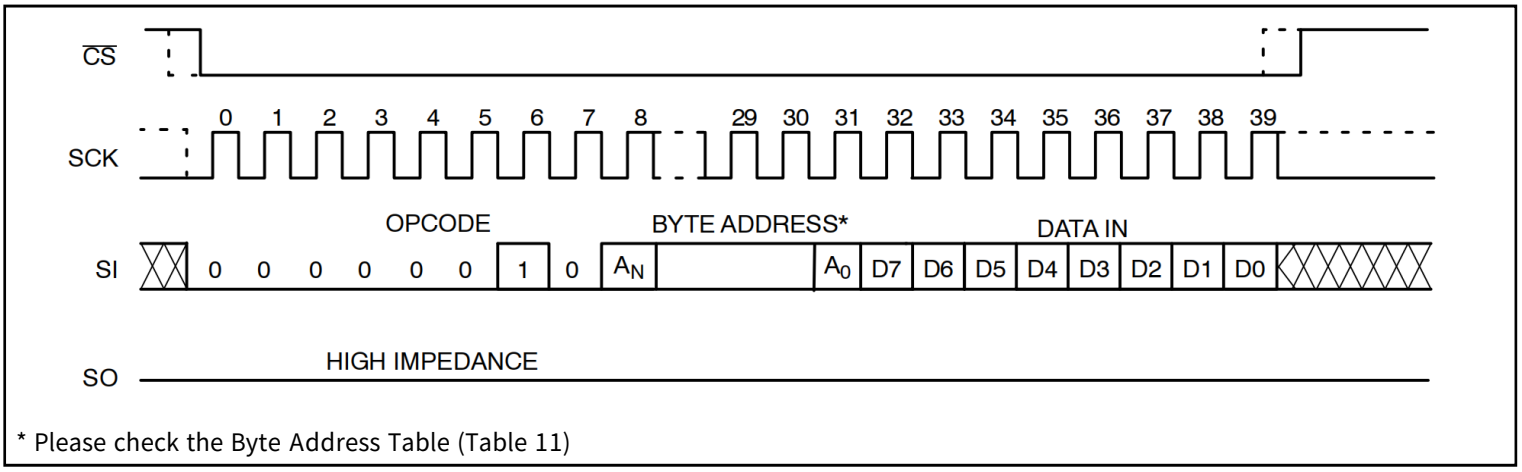


Figure 5. Byte WRITE Timing

Note: Dashed Line = mode (1, 1)

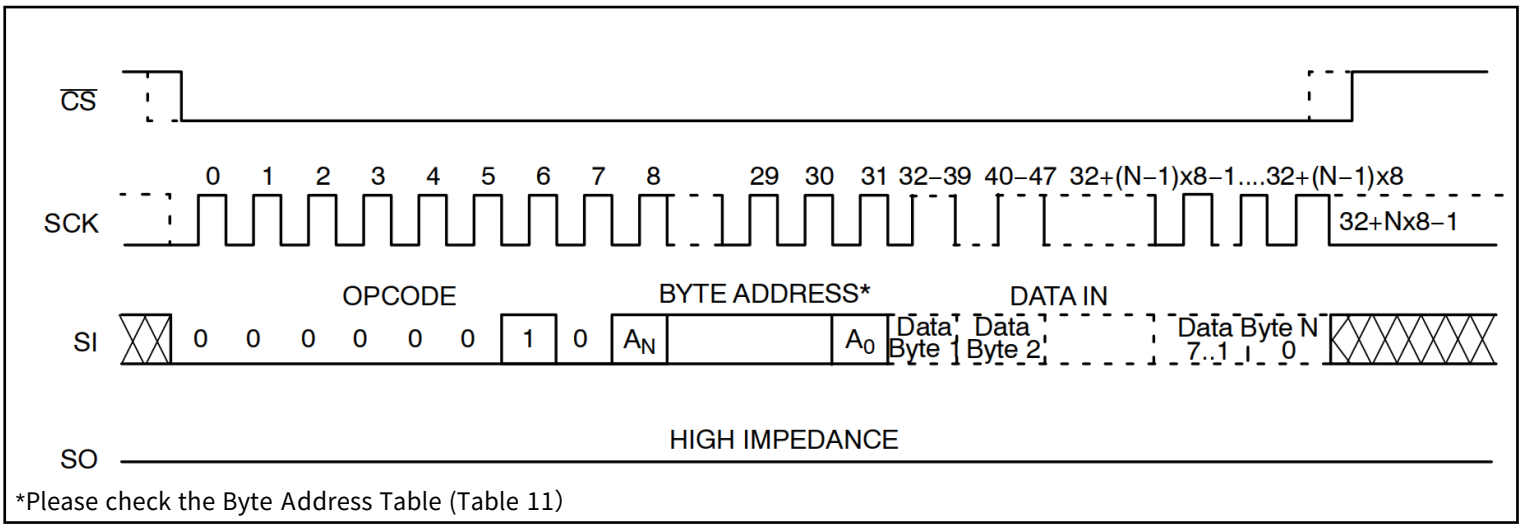


Figure 6. Page WRITE Timing

Note: Dashed Line = mode (1, 1)

Write Status Register：The Status Register is written by sending a WRSR instruction according to timing shown in Figure 7.Only bits 2, 3, 4, 6 and 7 can be written using the WRSR command.

Write Protection：The Write Protect (WP) pin can be used to protect the Block Protect bits BP0 and BP1 against being inadvertently altered. When WP is low and the WPEN bit is set to “ 1 ”, write operations to the Status Register are inhibited. WP going low while CS is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, WP going low will have no effect on any write operation to the Status Register. The WP pin function is blocked when the WPEN bit is set to “ 0 ”. The WP input timing is shown in Figure 8.

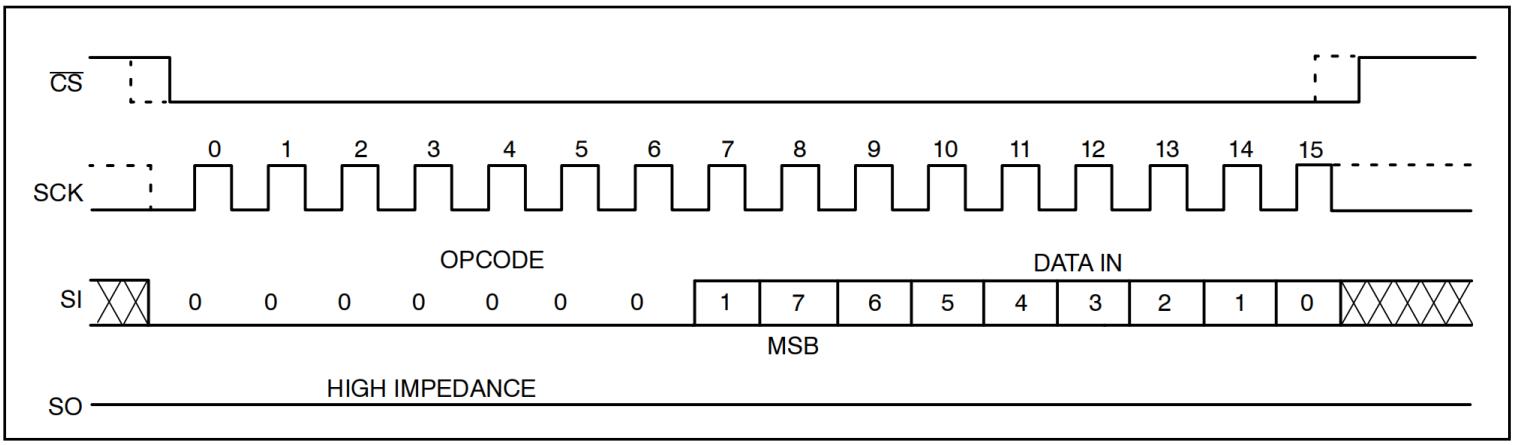


Figure 7. WRSR Timing

Note: Dashed Line = mode (1, 1)

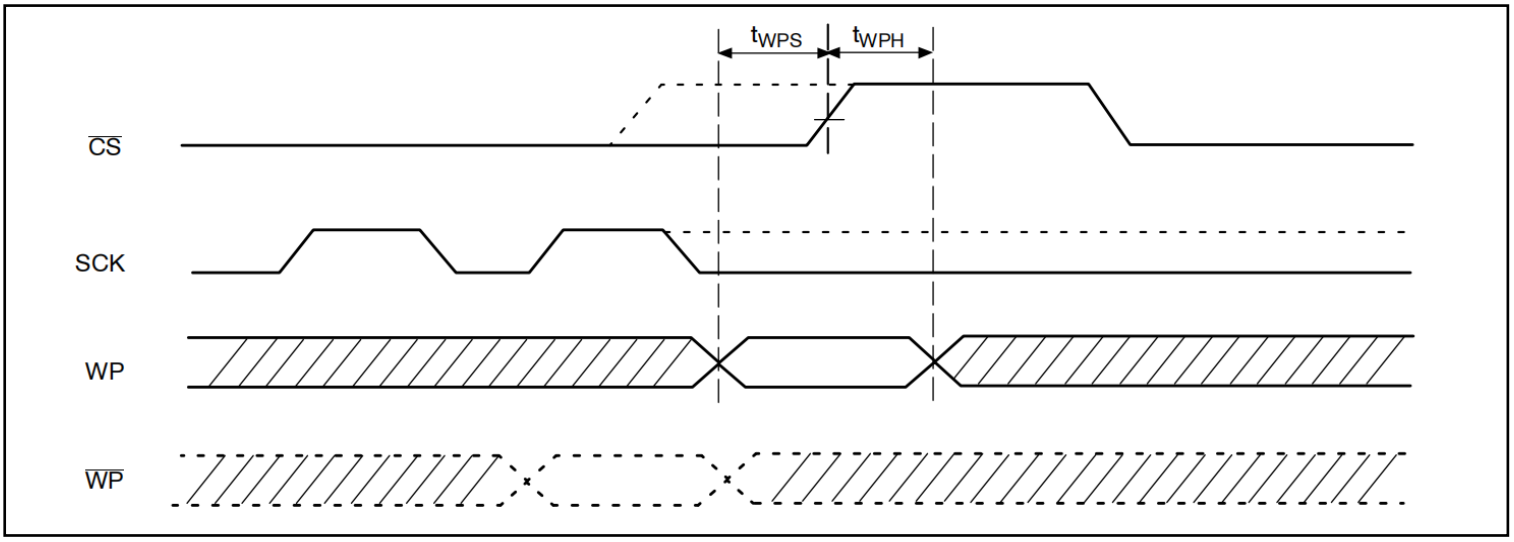


Figure 8. WP Timing

Note: Dashed Line = mode (1, 1)

Read Operations

Read from Memory Array：To read from memory, the host sends a READ instruction followed by a 24_bit address (see Table 11 for the number of significant address bits). After receiving the last address bit, the CAT25M01 will respond by shifting out data on the SO pin (as shown in Figure 9). Sequentially stored data can be read out by simply continuing to run the clock. The internal address pointer is automatically incremented to the next higher address as data is shifted out. After reaching the highest memory address, the address counter " rolls over to the lowest memory address, and the read cycle can be continued indefinitely. The read operation is terminated by taking CS high.

Read Identification Page：Reading the additional 256_byte Identification Page (IP) is achieved using the same Read command sequence as used for Read from main memory array (Figure 9). The IPL bit from the Status Register must be set (IPL = 1) before attempting to read from the IP. The [A7:A0] are the address significant bits that point to the data byte shifted out on the SO pin. If the CS continues to be held low, the internal address register defined by [A7:A0] bits is automatically incremented and the next data byte from the IP is shifted out. The byte address must not exceed the 256_byte page boundary.

Read Status Register：To read the status register, the host simply sends a RDSR command. After receiving the last bit of the command, the CAT25M01 will shift out the contents of the status register on the SO pin (Figure 10). The status register may be read at any time, including during an internal write cycle.

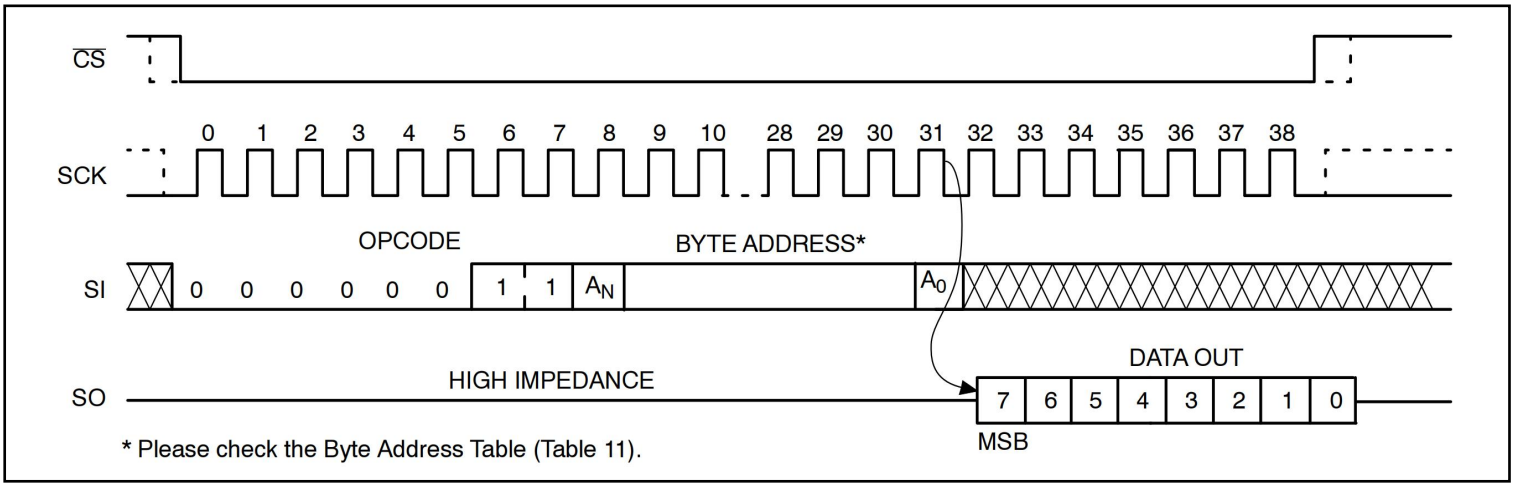


Figure 9. READ Timing

Note: Dashed Line = mode (1, 1)

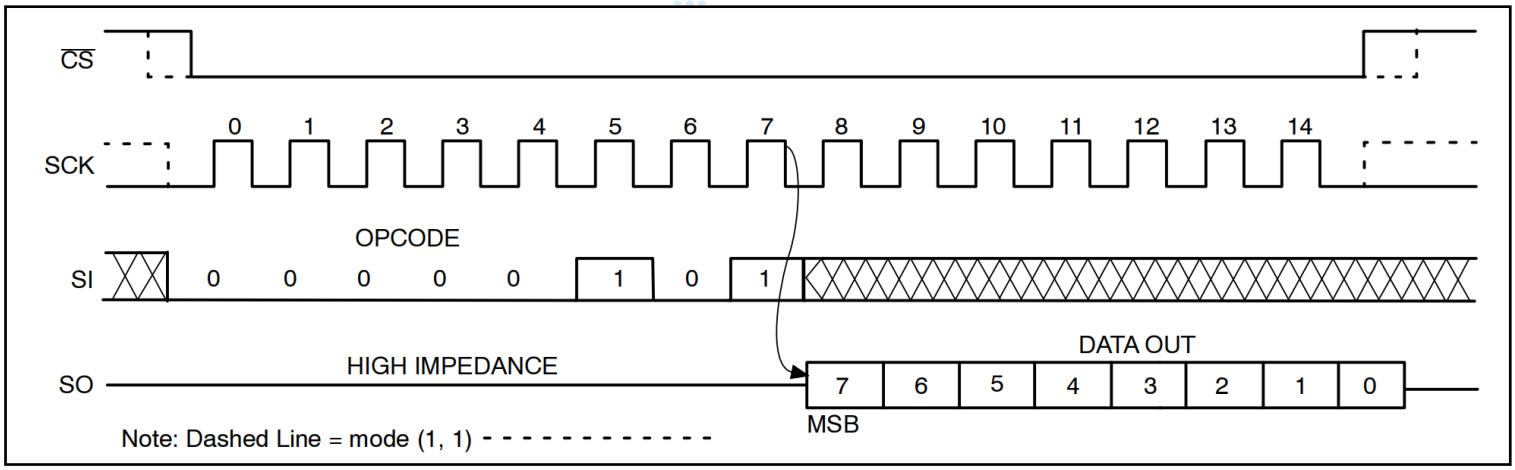


Figure 10. RDSR Timing

Hold Operation ：The HOLD input can be used to pause communication between host and CAT25M01. To pause, HOLD must be taken low while SCK is low (Figure 11). During the hold condition the device must remain selected (CS low). During the pause, the data output pin (SO) is tri_stated (high impedance) and SI transitions are ignored. To resume communication, HOLD must be taken high while SCK is low.

Design Considerations ：The CAT25M01 device incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bidirectional POR behavior protects the device against ‘ brownout ’ failure following a temporary loss of power. The CAT25M01 device powers up in a write disable state and in a low power standby mode. A WREN instruction must be issued prior any writes to the device.
After power up, the CS pin must be brought low to enter a ready state and receive an instruction. After a successful byte/page write or status register write, the device goes into a write disable mode. The CS input must be set high after the proper number of clock cycles to start the internal write cycle. Access to the memory array during an internal write cycle is ignored and programming is continued. Any invalid opcode will be ignored and the serial output pin (SO) will remain in the high impedance state.

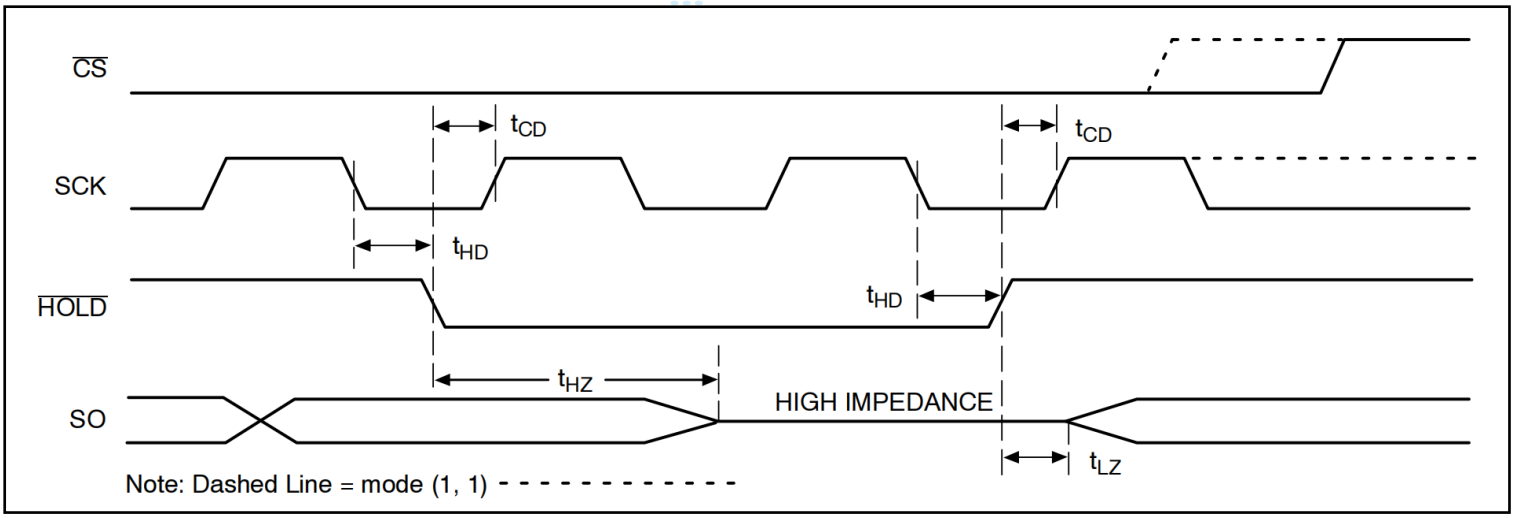


Figure 11. HOLD Timing

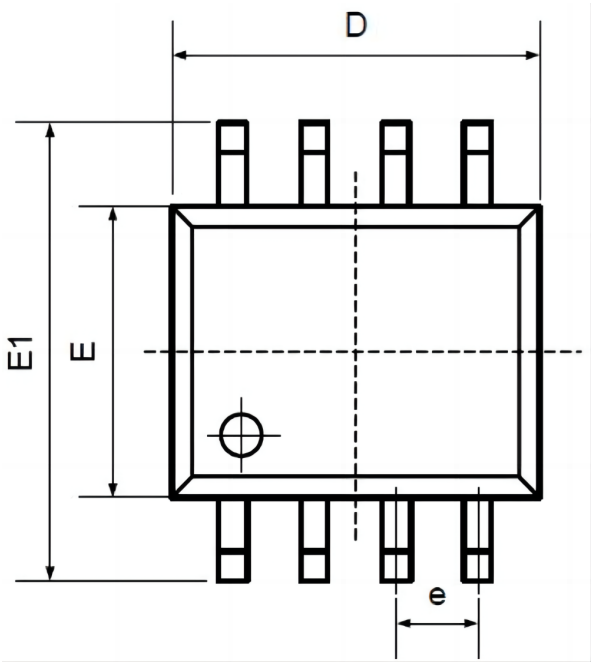
Order information

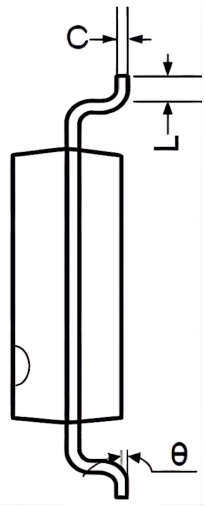
Order Number	Package	Package Quantity	Marking On The park	Temperature
CAT25M01VI-GT3-TUDI	SOP8	Tape,Reel,4000	25M01A	-40°C to +85°C

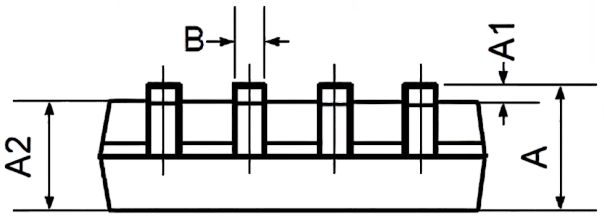
Revision history

	Date	Revision	Page
V1.0	2020/7	New	1-19
V1.1	2024/1	Update model and PDF template	1-19

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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