

钍地半导体
Tudi Semiconductor

Product Specification

TUDI- AT25M02

SPI Serial EEPROM 2 Mbits (262,144 x 8)

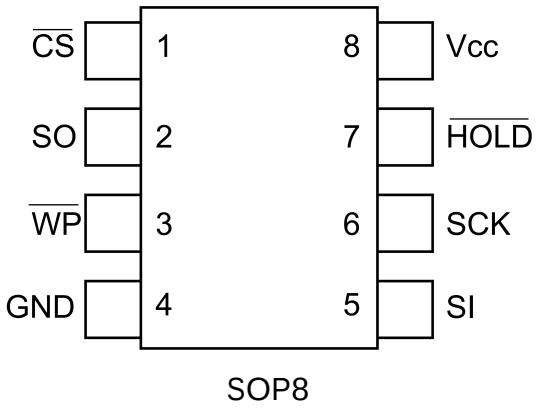
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Features



SOP8

- ●Serial Peripheral Interface (SPI) Compatible
- ● Supports SPI Modes 0 (0,0) and 3 (1,1):
- – Data sheet describes mode 0 operation
- ● Low-Voltage and Standard-Voltage Operation:
- – 1.7V (V_{CC} = 1.7V to 5.5V)
- – 2.5V (V_{CC} = 2.5V to 5.5V)
- ● Industrial Temperature Range: -40 ° C to +85 ° C
- ● 5 MHz Clock Rate (5V)
- ● 256-Byte Page Mode
- ● Block Write Protection:
- – Protect 1/4, 1/2 or entire array
- ●Write-Protect (WP) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- ● Self-Timed Write Cycle within 10 ms Maximum
- ●ESD Protection > 4,000V
- ● High Reliability:
- – Endurance: 1,000,000 write cycles
- – Data retention: 100 years
- ● Green (Lead-free/Halide-free/RoHS Compliant) Package Options
- ●Die Sale Options: Wafer Form and Bumped Wafers

Description

The AT25M02 provides 2,097,152 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 262,144 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low_power and low_voltage operation are essential. The device is available in space-saving 8_lead SOIC . All packages operate from 1.7V to 5.5V or 2.5V to 5.5V.

Pin Description

Table1 Pin Function Table

The descriptions of the pins are listed in Table 1.

Name	8-Lead SOIC	Function
CS	1	Chip Select
SO	2	Serial Data Output
WP(1)	3	Write-Protect
GND	4	Ground
SI	5	Serial Data Input
SCK	6	Serial Data Clock
HOLD(1)	7	Suspends Serial Input
VCC	8	Device Power Supply

Note:1. The Write-Protect (WP) and Hold (HOLD) pins should be driven high or low as appropriate

Chip Select (CS) :The AT25M02 is selected when the Chip Select (CS) pin is low. When the device is not selected, data will not be accepted via the Serial Data Input (SI) pin, and the Serial Output (SO) pin will remain in a high-impedance state.
To ensure robust operation, the CS pin should follow VCC upon power-up. It is therefore recommended to connect CS to VCC using a pull-up resistor (less than or equal to 10 kΩ). After power-up, a low level on CS is required prior to any sequence being initiated.

Serial Data Output (SO): The Serial Data Output (SO) pin is used to transfer data out of the AT25M02. During a readsequence, data is shifted out on this pin after the falling edge of the Serial Data Clock (SCK).

Write-Protect (WP): The Write-Protect (WP) pin will allow normal read/write operations when held high. When the WP pin is brought low and the WPEN bit is set to a logic ‘1’, all write operations to the STATUS register are inhibited. WP going low while CS is still low will interrupt a write operation to the STATUS register. If the internal write cycle has already been initiated, WP going low will have no effect on any write operation to the STATUS register. The WP pin function is blocked when the WPEN bit in the STATUS register is set to a logic ‘0’. This will allow the user to install the AT25M02 in a system with the WP pin tied to ground and still be able to write to the STATUS register. All WP pin functions are enabled when the WPEN bit is set to a logic ‘1’.

Ground (GND): The ground reference for the Device Power Supply (V_{CC}). The Ground (GND) pin should be connected to the system ground.

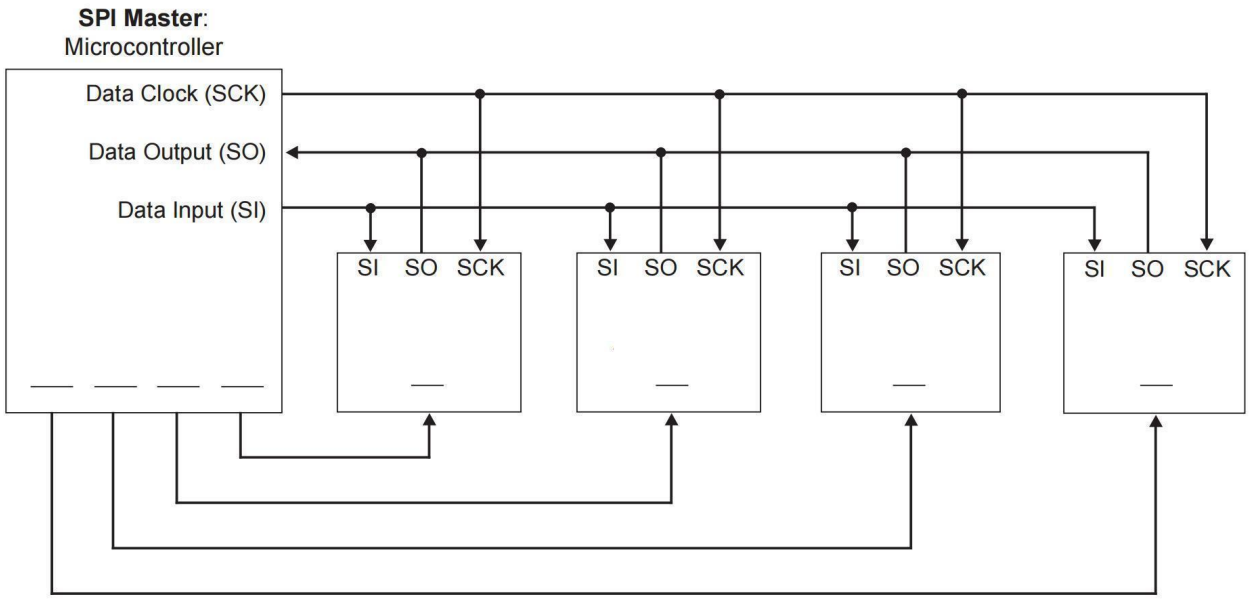
Serial Data Input (SI): The Serial Data Input (SI) pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the Serial Data Clock (SCK).

Serial Data Clock (SCK): The Serial Data Clock (SCK) pin is used to synchronize the communication between a master and the AT25M02. Instructions, addresses or data present on the Serial Data Input (SI) pin is latched in on the rising edge of SCK, while output on the Serial Data Output (SO) pin is clocked out on the falling edge of SCK.

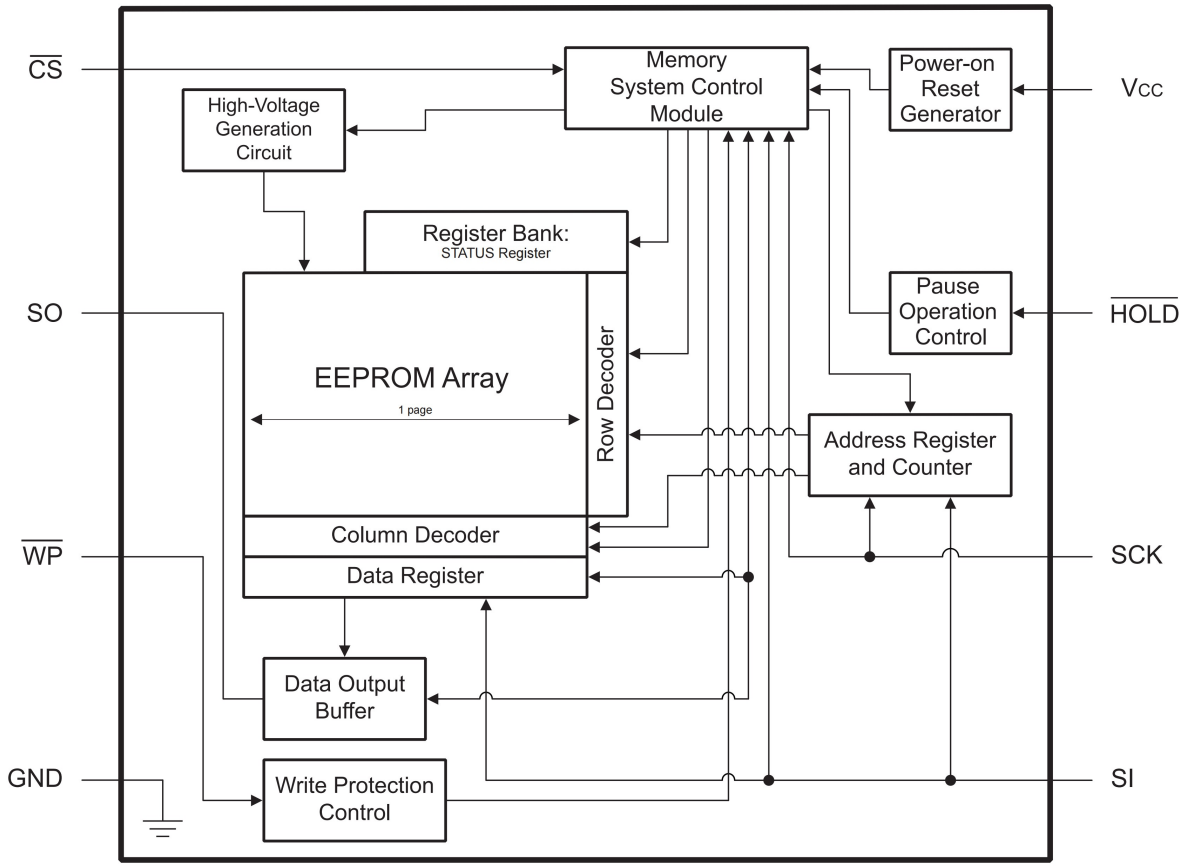
Suspend Serial Input (HOLD): The Suspend Serial Input (HOLD) pin is used in conjunction with the Chip Select (CS) pin to pause the AT25M02. When the device is selected and a serial sequence is underway, HOLD can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the HOLD pin must be brought low while the Serial Data Clock (SCK) pin is low. To resume serial communication, the HOLD pin is brought high while the SCK pin is low (SCK may still toggle during HOLD). Inputs to the Serial Data Input (SI) pin will be ignored while the Serial Data Output (SO) pin will be in the high_impedance state.

Device Power Supply (Vcc): The Device Power Supply (V_{CC}) pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.

SPI Bus Master Connections to Serial EEPROMs



Block Diagram



Electrical Characteristics

Absolute Maximum Ratings

Operating temperature·····-55°C to +125°C

Storage temperature·····-65°C to +150°C

Voltage on any pin with respect to ground·····-1.0V to +7.0V

V_{CC}·····6.25V

DC output current·····5.0 mA

ESD protection·····> 4 kV

Note: Stresses above those listed under " Absolute Maximum Ratings " may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

DC and AC Operating Range

Table 2.DC and AC Operating Range

AT25M02		
Operating Temperature(Case)	Industrial Temperature Range	-40℃ to+85℃
V_{CC} Power Supply	Low-Voltage Grade	1.7V to 5.5V
	Standard-Voltage Grade	2.5V to 5.5V

Table 3.DC Characteristics (1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	
Supply Voltage	Vcc1	1.7	—	5.5	V		
Supply Voltage	Vcc2	2.5	—	5.5	V		
Supply Current	Icc1	—	0.3	1.0	mA	Vcc=1.8V(3)at 1 MHz,SO=Open,Read	
Supply Current	Icc2	—	0.5	1.0	mA	Vcc=1.8V(3)at 5 MHz,SO=Open,Read,Write	
Supply Current	Icc3	—	1.0	2.0	mA	Vcc=5.0V at 1 MHz,SO=Open,Read	
Supply Current	Icc4	—	2.0	3.0	mA	Vcc=5.0V at 5 MHz,SO=Open,Read	
Supply Current	Icc5	—	0.3	2.0	mA	Vcc=1.8V(3),SO=Open,During t_{WC},CS=Vcc	
Supply Current	Icc6	—	0.5	3.0	mA	Vcc=5.0V,SO=Open,During t_{WC},CS =Vcc	
Standby Current	I_{SB1}	—	0.08	1.0	μA	Vcc=1.8V(3) ,CS=Vcc	
Standby Current	I_{SB2}	—	0.08	2.0	μA	Vcc=2.5V,CS=Vcc	
Standby Current	I_{SB3}	—	0.15	3.0	μA	Vcc=5.5V,CS=Vcc	
Input Leakage	I_{IL}	-3.0	—	3.0	μA	V_{IN}=0V to Vcc	
Output Leakage	I_{OL}	-3.0	—	3.0	μA	V_{IN}=0V to Vcc,T_A=0℃ to+70℃	
Input Low-Voltage	$V_{IN(2)}$	-1.0	—	Vcc×0.3	V		
Input High-Voltage	$V_{IN(2)}$	Vcc×0.7	—	Vcc+0.5	V		
Output Low-Voltage	V_{OL1}	—	—	0.4	V	3.6V≤Vcc≤5.5V	I_{OL}=3.0 mA

Table 3.DC Characteristics (1)(continued)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	
Output High-Voltage	V_{OH1}	Vcc-0.8	—	—	V	3.6V≤Vcc≤5.5V	I_{OH}=-1.6 mA
Output Low-Voltage	V_{OL2}	—	—	0.2	V	1.7V≤Vcc≤3.6V	I_{OL}=0.15 mA
Output High-Voltage	V_{OH2}	Vcc-0.2	—	—	V	1.7V≤Vcc≤3.6V	I_{OH}=-100 μA

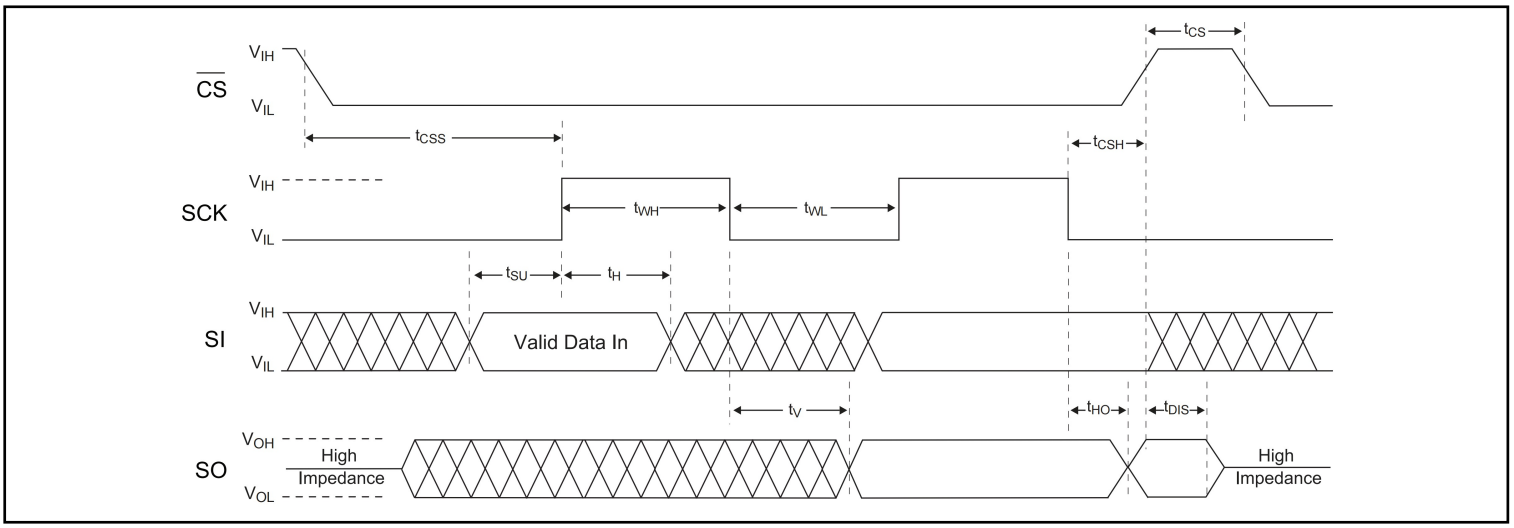
Note:1. Applicable over recommended operating range from T_A = -40 ° C to +85 ° C, V_{CC} = As Specified, C_L = 1 TTL Gate and 30 pF (unless otherwise noted).
2. This parameter is ensured by characterization only.

Table 4.AC Characteristics(1)

Parameter	Symbol	Minimum	Maximum	Units
SCK Clock Frequency	f_{SCK}	0	5	MHz
Input Rise Time	t_{RI}(2)	—	80	ns
Input Fall Time	t_{FI}(2)	—	80	ns
SCK High Time	t_{WH}	80	—	ns
SCK Low Time	t_{WL}	80	—	ns
CS High Time	t_{CS}	200	—	ns
CS Setup Time	t_{CSS}	200	—	ns
CS Hold Time	t_{CSH}	200	—	ns
Data In Setup Time	t_{SU}	20	—	ns
Data In Hold Time	t_{H}	20	—	ns
HOLD Setup Time	t_{HD}	20	—	ns
HOLD Hold Time	t_{CD}	20	—	ns
Output Valid	t_{V}	0	80	ns
Output Hold Time	t_{HO}	0	—	ns
HOLD to Output Low-Z	t_{LZ}	0	100	ns
HOLD to Output High-Z	t_{HZ}	—	100	ns
Output Disable Time	t_{DIS}	—	100	ns
Write Cycle Time	t_{WC}	—	10	ms

Note:1. Applicable over recommended operating range from T_A = -40 ° C to +85 ° C, V_{CC} = As Specified, C_L = 1 TTL Gate and 30 pF (unless otherwise noted).
2. This parameter is ensured by characterization only

SPI Synchronous Data Timimg



Electrical Specifications

Power-Up Requirements and Reset Behavior: During a power-up sequence, the VCC supplied to the AT25M02 should monotonically rise from GND to the minimum VCC level, as specified in Table 2, with a slew rate no faster than 0.1 V/µs.

Device Reset: To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, the AT25M02 includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any instructions until the VCC level crosses the internal voltage threshold (VPOR) that brings the device out of Reset and into Standby mode. The system designer must ensure the instructions are not sent to the device until the VCC supply has reached a stable value greater than or equal to the minimum VCC level. Additionally, once the VCC is greater than or equal to the minimum VCC level, the bus master must wait at least tPUP before sending the first instruction to the device. See Table 5 for the values associated with these power-up parameters.

Table 5.Power-Up Conditions(1)

Symbol	Parameter	Min.	Max.	Units
tPUP	Time required after Vcc is stable before the device can accept instructions	100	—	µs
VPOR	Power-on Reset Threshold Voltage	—	1.5	V
tPOFF	Minimum time at Vcc=0V between power cycles	1	—	ms

Note: 1. These parameters are characterized but they are not 100% tested in production.
If an event occurs in the system where the V_{CC} level supplied to the AT25M02 drops below the maximum V_{POR} level specified, it is recommended that a full-power cycle sequence be performed by first driving the V_{CC} pin to GND in less than 1 ms, waiting at least the minimum t_{POFF} time and then performing a new power-up sequence in compliance with the requirements defined in this section.

Table 6. Pin Capacitance(1,2)

Symbol	Test Condition	Max.	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT}=0V
C_{IN}	Input Capacitance(CS,SCK,SI,WP,HOLD)	6	pF	V_{IN}=0V

Note:1. This parameter is characterized but is not 100% tested in production.
2. Applicable over recommended operating range from: T_A = 25 ° C, f_{SCK} = 1.0 MHz, V_{CC} = 5.0V (unless otherwise noted).

Table 7. EEPROM Cell Performance Characteristics

Operation	Test Condition	Min.	Max.	Units
Write Endurance(1)	T_A=25°C,V_{cc}(min.)<V_{cc}<V_{cc}(max.), Byte(2)or Page Write mode	1,000,000	—	Write Cycles
Data Retention(1)	T_A=55°C	100	—	Years

Note:1. Performance is determined through characterization and the qualification process.
2. Due to the memory array architecture, the Write Cycle Endurance is specified for writes in groups of four data bytes. The beginning of any 4-byte boundaries can be determined by multiplying any integer (N) by four (i.e., 4*N). The end address can be found by adding three to the beginning value (i.e., 4*N+3).

Software Reset: The SPI interface of the AT25M02 can be reset by toggling the CS input. If the CS line is already in the active state, it must complete a transition from the inactive state (≥V_{IH}) to the active state (≤V_{IL}) and then back to the inactive state (≥V_{IH}) without sending clocks on the SCK line. Upon completion of this sequence, the device will be ready to receive a new opcode on the SI line.

Device Default Condition: The AT25M02 is shipped from Microchip to the customer with the EEPROM array set to an all FFh data pattern (logic ‘1’ state). The Write-Protect Enable bit in the STATUS register is set to logic ‘0’ and the Block Write-Protection bits in theSTATUS register are set to logic ‘0’.

Device Default State at Power-Up

The AT25M02 default state upon power-up consists of:

- Standby Power mode
- A high-to-low-level transition on CS is required to enter active state
- Write Enable Latch (WEL) bit in the STATUS register = 0
- Ready/Busy bit in the STATUS register = 0, indicating the device is ready to accept a new command
- Device is not selected
- Not in Hold condition
- WPEN, BP1 and BP0 bits in the STATUS register are unchanged from their previous state due to the fact that they are nonvolatile values

Device Operation

The AT25M02 is controlled by a set of instructions that are sent from a host controller, commonly referred to as the SPI Master. The SPI Master communicates with the AT25M02 via the SPI bus which is comprised of four signal lines: Chip Select (CS), Serial Data Clock (SCK), Serial Data Input (SI) and Serial Data Output (SO).

The SPI protocol defines a total of four modes of operation (Mode 0, 1, 2 or 3) with each mode differing in respect to the SCK polarity and phase and how the polarity and phase control the flow of data on the SPI bus. The AT25M02 supports the two most common modes, SPI Modes 0 and 3. With SPI Modes 0 and 3, data is always latched in on the rising edge of SCK and always output on the falling edge of SCK. The only difference between SPI Modes 0 and 3 is the polarity of the SCK signal when in the inactive state (when the SPI Master is in Standby mode and not transferring any data). SPI Mode 0 is defined as a low SCK while CS is not asserted (at VCC) and SPI Mode 3 has SCK high in the inactive state. The SCK Idle state must match when the CS is deasserted both before and after the communication sequence in SPI Mode 0 and 3. The figures in this document depict Mode 0 with a solid line on SCK while CS is inactive and Mode 3 with a dotted line.

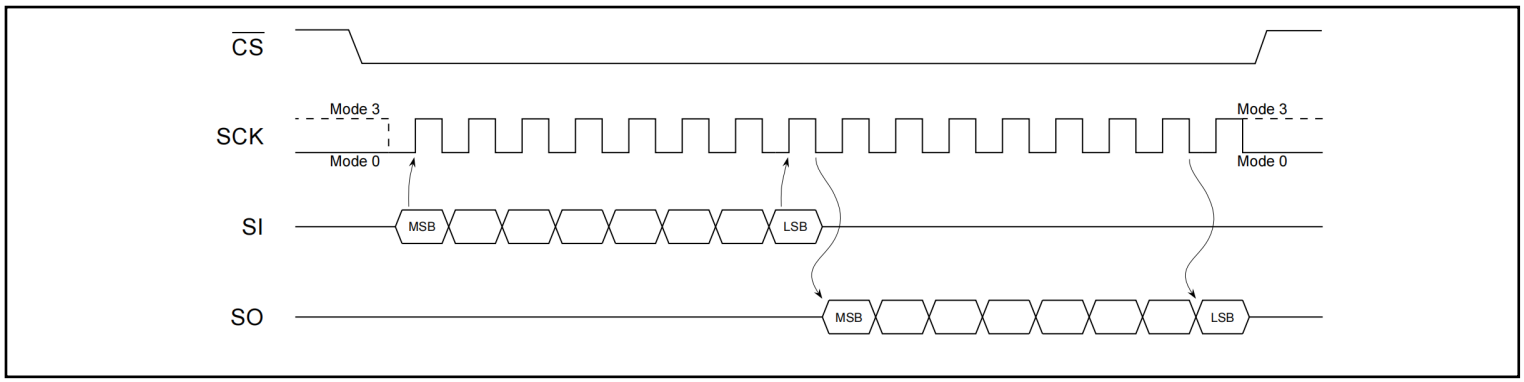


Figure1.SPI Mode 0 and Mode 3

Interfacing the AT25M02 on the SPI Bus: Communication to and from the AT25M02 must be initiated by the SPI Master device, such as a microcontroller. The SPI Master device must generate the serial clock for the AT25M02 on the Serial Data Clock (SCK) pin. The AT25M02 always operates as a slave due to the fact that the SCK is always an input.

Selecting the Device :The AT25M02 is selected when the Chip Select (CS) pin is low. When the device is not selected, data will not be accepted via the Serial Data Input (SI) pin, and the Serial Data Output (SO) pin willremain in a high_impedance state.

Sending Data to the Device :The AT25M02 uses the SI pin to receive information. All instructions, addresses and data input bytes are clocked into the device with the Most Significant bit (MSb) first. The SI pin samples on the first rising edge of the SCK line after the CS has been asserted.

Receiving Data from the Device: Data output from the device is transmitted on the SO pin, with the MSb output first. The SO data is latched on the first falling edge of SCK after the instruction has been clocked into the device, such as the Read from Memory Array (READ) and Read STATUS Register (RDSR) instructions.

Device Opcodes

Serial Opcode: After the device is selected by driving CS low, the first byte will be received on the SI pin. This byte contains the opcode that defines the operation to be performed. Refer to Table 8 for a list of all opcodes that the AT25M02 will respond to.

Invalid Opcode: If an invalid opcode is received, no data will be shifted into AT25M02 and the SO pin will remain in a high-impedance state until the falling edge of CS is detected again. This will reinitialize the serial communication.

Hold Function: The Suspend Serial Input (HOLD) pin is used to pause the serial communication with the device without having to stop or reset the clock sequence. The Hold mode, however, does not have an effect on the internal write cycle. Therefore, if a write cycle is in progress, asserting the HOLD pin will not pause the operation and the write cycle will continue to completion.
The Hold mode can only be entered while the CS pin is asserted. The Hold mode is activated by asserting the HOLD pin during the SCK low pulse. If the HOLD pin is asserted during the SCK high pulse, then the Hold mode will not be started until the beginning of the next SCK low pulse. The device will remain in the Hold mode as long as the HOLD pin and CS pin are asserted.
While in Hold mode, the SO pin will be in a high-impedance state. In addition, both the SI pin and the SCK pin will be ignored. The Write-Protect (WP) pin, however, can still be asserted ordeassertedwhile in the Hold mode.

To end the Hold mode and resume serial communication, the HOLD pin must be deasserted during the SCK low pulse. If the HOLD pin is deasserted during the SCK high pulse, then the Hold mode will not end until the beginning of the next SCK low pulse.
If the CS pin is deasserted while the HOLD pin is still asserted, then any operation that may have been started will be aborted and the device will reset the WEL bit in the STATUS register back to the logic ‘ 0 ’ state.

Write Protection: The Write-Protect (WP) pin will allow normal read and write operations when held high. When the WP pin is brought low and WPEN bit is a logic ‘ 1 ’, all write operations to the STATUS register are inhibited. The WP pin going low while CS is still low will interrupt a Write STATUS Register (WRSR). If the internal write cycle has already been initiated, WP going low will have no effect on any write operation to the STATUS register. The WP pin function is blocked when the WPEN bit in the STATUS register is a logic ‘ 0 ’. This will allow the user to install the AT25M02 device in a system with the WP pin tied to ground and still be able to write to the STATUS register. All WP pin functions are enabled when the WPEN bit is set to a logic ‘ 1 ’

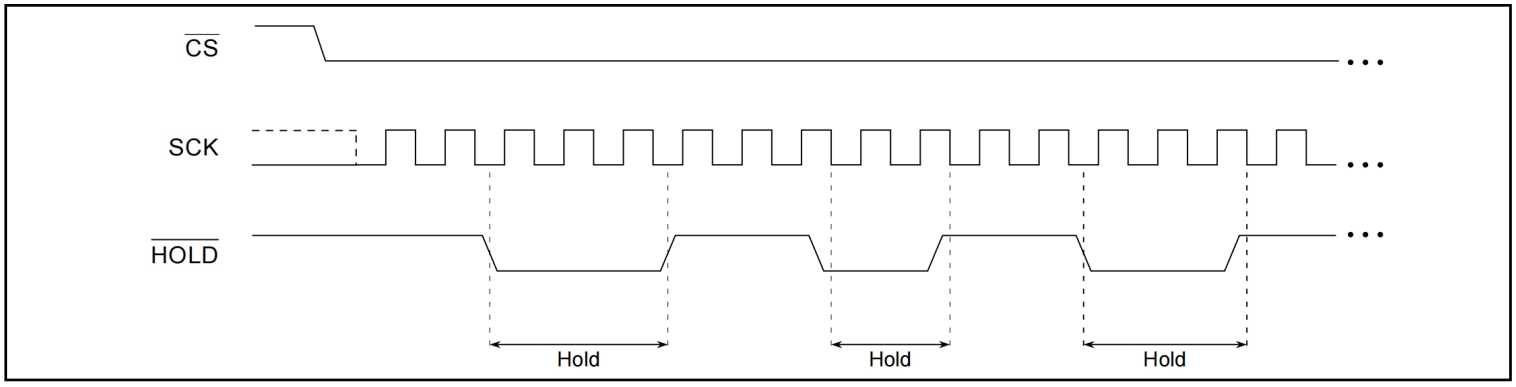


Figure 2.Hold Mode

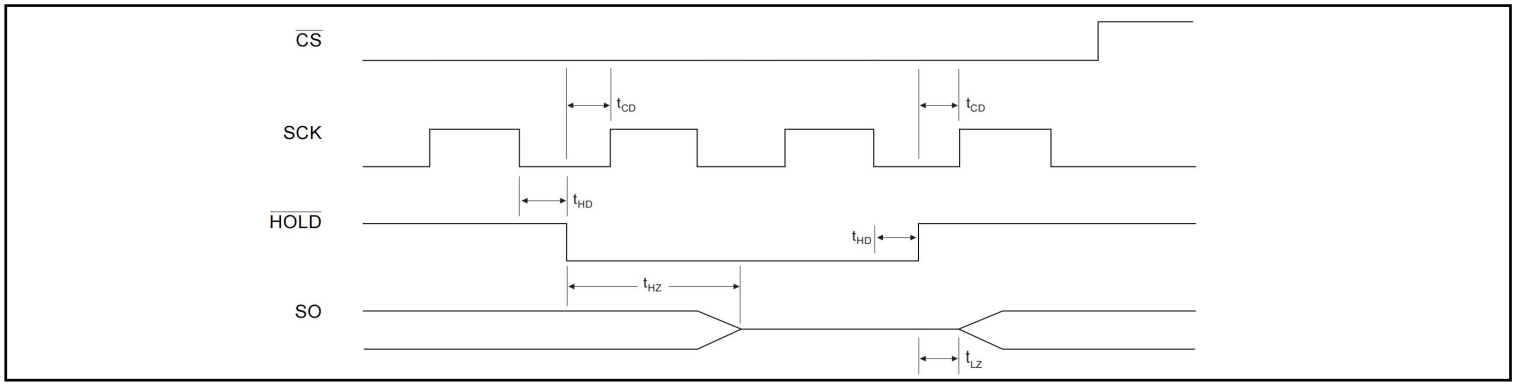


Figure3.Hold Timing

Device Commands and Addressing

The AT25M02 is designed to interface directly with the synchronous Serial Peripheral Interface (SPI). The AT25M02 utilizes an 8_bit instruction register. The list of instructions and their operation codes are contained in Table 8. All instructions, addresses and data are transferred with the MSb first and start with a high_to_low CS transition.

Table8. Instruction Set for the AT25M02

Instruction Name	Instruction Format	Operates On	Operation Description
WREN	0000 0110 (06h)	STATUS Register	Set Write Enable Latch (WEL)
WRDI	0000 0100 (04h)	STATUS Register	Reset Write Enable Latch (WEL)
RDSR	0000 0101(05h)	STATUS Register	Read STATUS Register
WRSR	0000 0001 (01h)	STATUS Register	Write STATUS Register
READ	0000 0011 (03 h)	Memory Array	Read from Memory Array
WRITE	0000 0010 (02 h) 0000 0111 (07 h)	Memory Array	Write to Memory Array
LPWP	0000 1000(08h)	STATUS Register	Low-Power Write Poll

STATUS Register Bit Definition and Function

The AT25M02 includes an 8_bit STATUS register. The STATUS register bits modulate various features of the device as shown in Table9 and Table 10. These bits can be changed by specific instructions that are detailed in the following sections.

Table 9.STATUS Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEL	RDY/BSY

Table10. STATUS Register Bit Definition

Bit	Name		Type	Description	
7	WPEN	Write-Protect Enable	R/W	0	See Table 12(Factory Default)
				1	See Table 12(Factory Default)
6:4	RFU	Reserved for Future Use	R	0	Reads as zeros when the device is not in a writecycle
				1	Reads as ones when the device is in a write cycle
3:2	BP1 BP0	Block Write Protection	R/W	00	No array write protection (Factory Default)
				01	Quarter array write protection (see Table 11)
				10	Half array write protection (see Table 11)
				11	Entire array write protection(see Table 11)
1	WEL	Write Enable Latch	R	0	Device is not write enabled(Power-up Default)
				1	Device is write enabled
0	RDY/BSY	Ready/Busy Status	R	0	Device is ready for a new sequence
				1	Device is busy with an internal operation

Read STATUS Register (RDSR) and Low-Power Write Poll (LPWP)

Read STATUS Register (RDSR) : The Read STATUS Register (RDSR) instruction provides access to the STATUS register. The ready/busy and write enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection (BP1, BP0) bits indicate the extent of memory array protection employed. The STATUS register is read by asserting the CS pin, followed by sending in a 05h opcode on the SI pin. Upon completion of the opcode, the device will return the 8_bit STATUS register value on the SO pin.

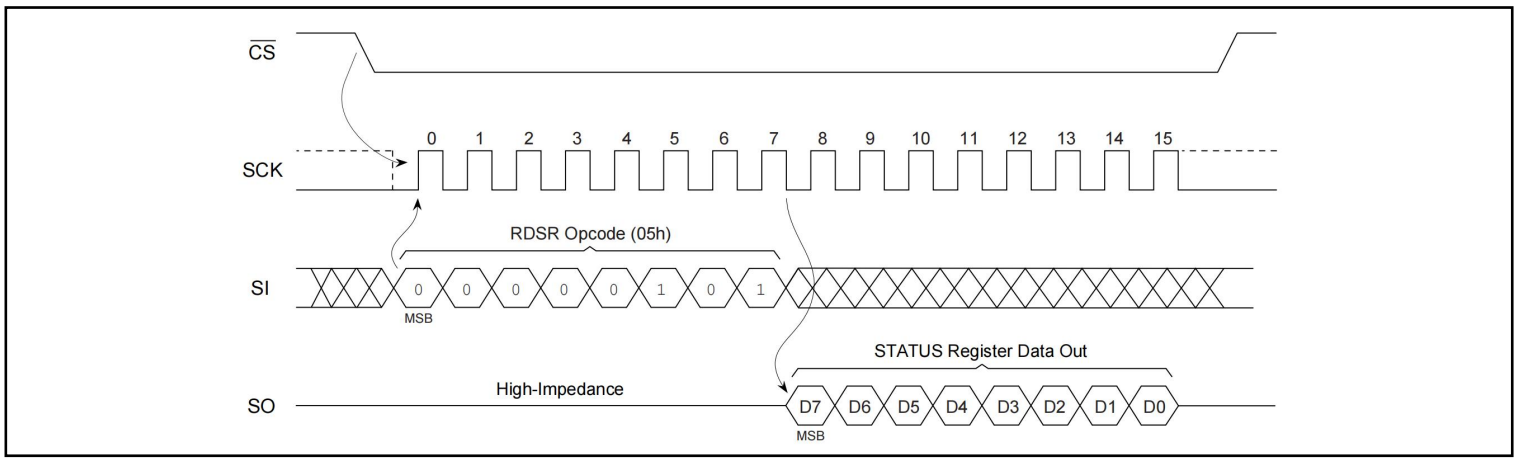


Figure 4. RDSR Waveform

Low-Power Write Poll (LPWP) :The Low-Power Write Poll command can be used after any write command as a means to check if the device has completed its internal write cycle. The LPWP command requires an opcode of 08h and will return an FFh value when the part is still busy completing the write cycle. The LPWP command will return a 00h value if the part is no longer in a write cycle. Refer to Polling Routine for a description on implementing a polling routine. Continuous reading of the LPWP state is supported and the value output by the device will be updated every eight bits.

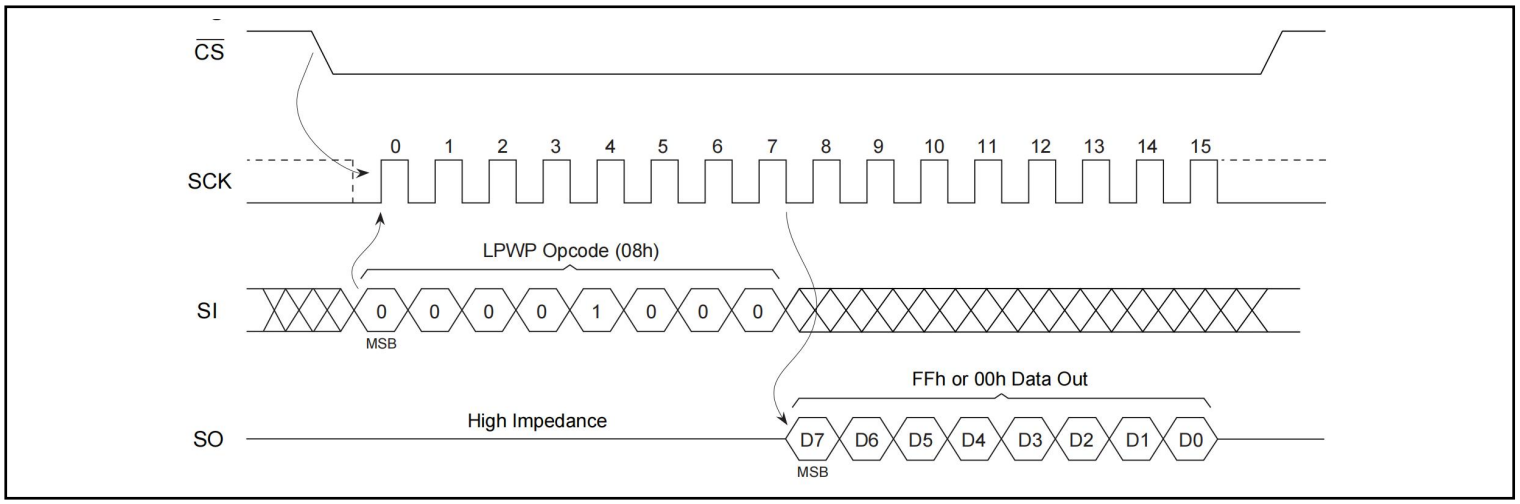


Figure 5. LPWP Waveform

Write Enable (WREN) and Write Disable (WRDI):Enabling and disabling writing to the STATUS register and EEPROM array is accomplished through the Write Enable (WREN) instruction and the Write Disable (WRDI) instruction. These functions change the status of the WEL bit in the STATUS register.

Write Enable Instruction (WREN) :The Write Enable Latch (WEL) bit of the STATUS register must be set to a logic ‘ 1 ’ prior to each Write STATUS Register (WRSR) and Write to Memory Array (WRITE) instructions. This is accomplished by sending a WREN (06h) instruction to the AT25M02. First, the CS pin is driven low to select the device and then a WREN instruction is clocked in on the SI pin. Then the CS pincan be driven high and the WEL bit will be updated in the STATUS register to a logic ‘ 1 ’. The device will power_up in the Write Disable state (WEL = 0).

Write Disable Instruction (WRDI) :To protect the device against inadvertent writes, the Write Disable (WRDI) instruction (opcode 04h) disables all programming modes by setting the WEL bit to a logic ‘ 0 ’. The WRDI instruction is independent of the status of the WP pin.

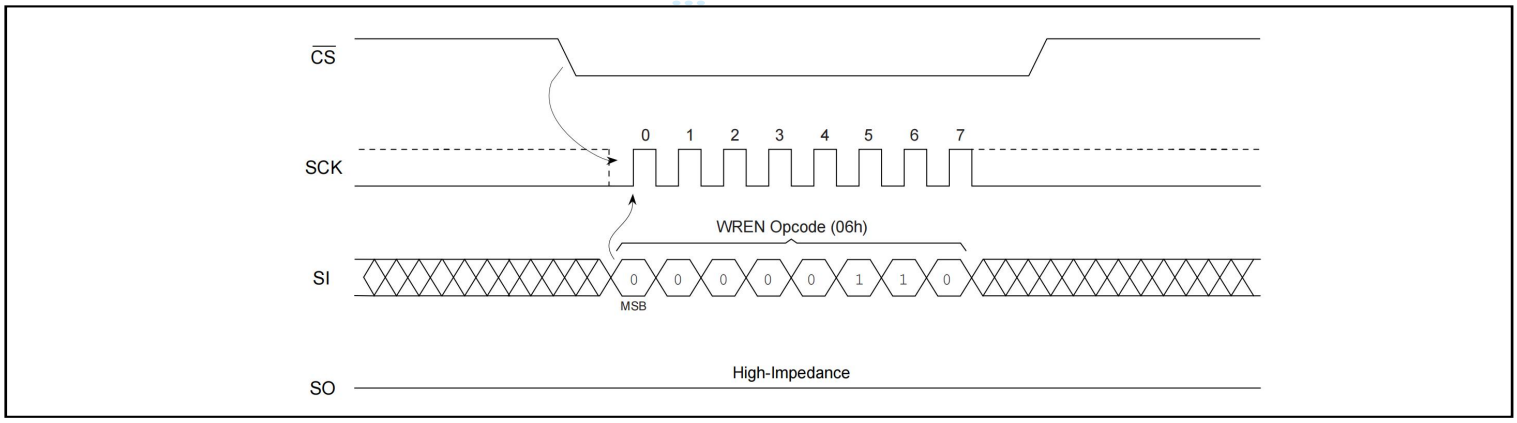


Figure 6.WREN Timing

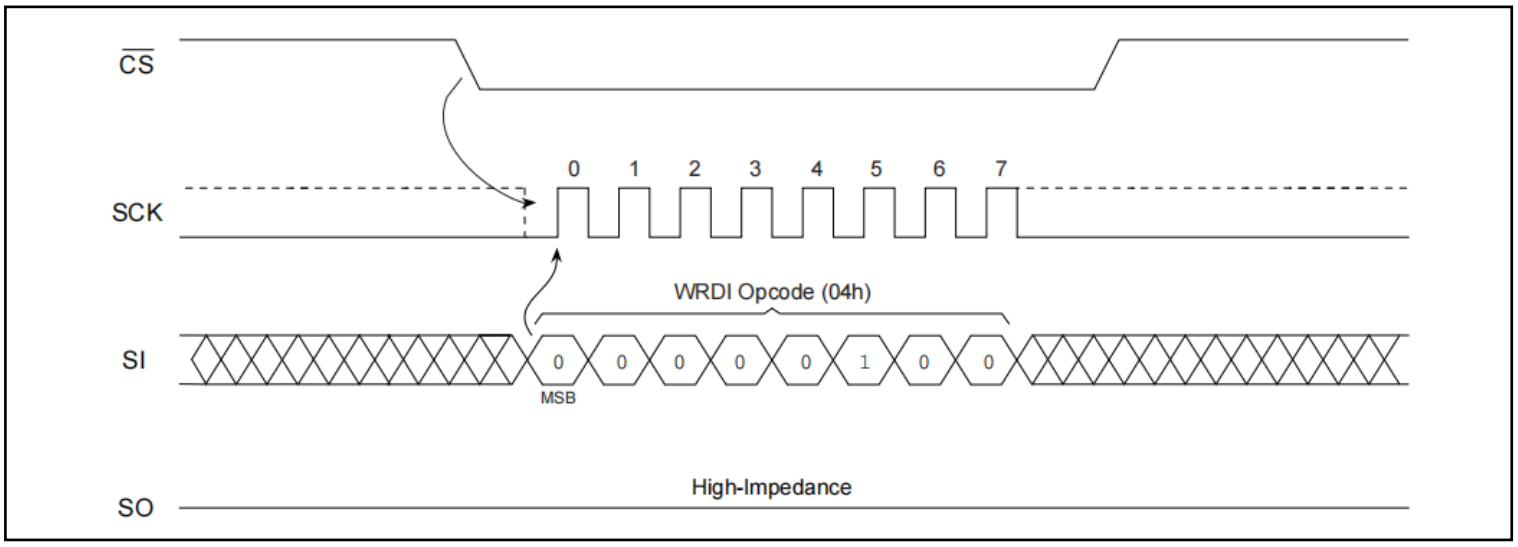


Figure 7.WRDI Timing

Write STATUS Register (WRSR)

The Write STATUS Register (WRSR) instruction enables the SPI Master to change selected bits of the STATUS register. Before a WRSR instruction can be initiated, a WREN instruction must be executed to set the WEL bit to logic ‘ 1 ’. Upon completion of a WREN instruction, a WRSR instruction can be executed.

The AT25M02 will not respond to commands other than a RDSR after a WRSR instruction until the self_timed internal write cycle has completed. When the write cycle is completed, the WEL bit in the STATUS register is reset to logic ‘ 0 ’.

Note:The WRSR instruction has no effect on bit 6, bit 5, bit 4, bit 1 and bit 0 of the STATUS register. Only bit 7, bit 3 and bit 2 can be changed via the WRSR instruction. These modifiable bits are the Write-Protect Enable (WPEN) and Block Protect (BP1, BP0) bits. These three bits are nonvolatile bits that have the same properties and functions as regular EEPROM cells. Their values are retained while power is removed from the device.

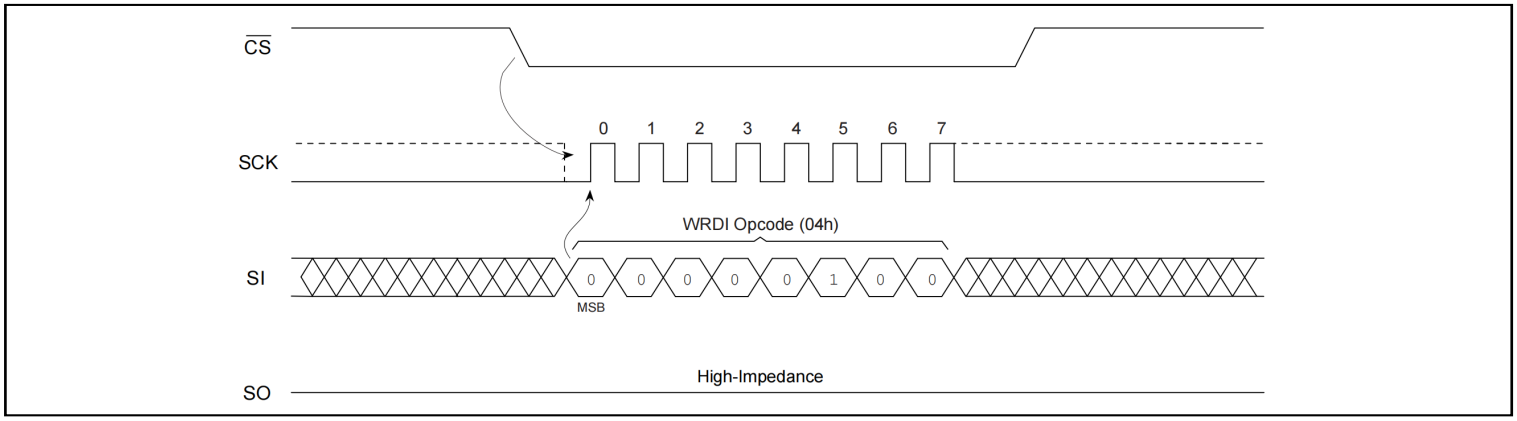


Figure8.WRSR Waveform

Note: 1. This instruction initiates a self-timed internal write cycle (t_{WC}) on the rising edge of CS after a valid sequence.

Block Write-Protect Function

The WRSR instruction allows the user to select one of four possible combinations as to how the memory array will be inhibited from writing through changing the Block Write-Protect bits (BP1, BP0). The four levels of array protection are:

- None of the memory array is protected.
- Upper quarter (¼) address range is write-protected meaning the highest order address bits are read_only.
- Upper half (¼) address range is write-protected meaning the highest order address bits are read_only.
- All of the memory array is write-protected meaning all address bits are read_only.

The Block Write Protection levels and corresponding STATUS register control bits are shown in Table 11.

Table 11.Block Write-Protect Bits

Level	STATUS Register Bits		Write-Protected/Read-Only Address Range
	BP1	BP0	AT25M02
0	0	0	None
1(1/4)	0	1	30000h-3FFFFh
2(1/ 2)	1	0	20000h-3FFFFh
3(All)	1	1	00000h-3FFFFh

Write-Protect Enable Function :The WRSR instruction also allows the user to enable or disable the Write-Protect (WP) pin throughthe use of the Write-Protect Enable (WPEN) bit. When the WPEN bit is set to logic ‘ 0 ’, the ability to write the EEPROM array is dictated by the values of the Block Write-Protect (BP1, BP0) bits. The ability to writethe STATUS register is controlled by the WEL bit. When the WPEN bit is setto logic ‘ 1 ’, the STATUS register is read-only.
Hardware Write Protection is enabled when both the WP pin is low and the WPEN bit has been set to a logic ‘ 1 ’. When the device is Hardware Write-Protected, writes to the STATUS register, including the Block Write-Protect, WEL and WPEN bits and to the sections in the memory array selected by the Block Write-Protect bits are disabled. When Hardware Write Protection is enabled, writes are only allowed to sections of the memory that are not block-protected.
Hardware Write Protection is disabled when either the WP pin is high or the WPEN bit is a logic ‘ 0 ’. When Hardware Write Protection is disabled, writes are only allowed to sections of the memory that are not block-protected. Refer to Table 12 for additional information.

Note: When the WPEN bit is Hardware Write_Protected, it cannot be set back to a logic ‘ 0 ’ as long as the WP pin is held low.

Table 12. WPEN Operation

WPEN	WP Pin	WEL	Protected Blocks	Unprotected Blocks	STATUS Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

Read Sequence

Reading the AT25M02 via the SO pin requires the following sequence. After the CS line is pulled low to select a device, the READ (03h) instruction is transmitted via the SI line followed by the 24_ bit address to be read. Refer to Table 13 for the address bits for AT25M02.

Table13.AT25M02 Address Bits

Address	AT25M02
A_N	A_{17}—A_0
Don't Care Bits	A_{23} —A_{18}

Upon completion of the 24-bit address, any data on the SI line will be ignored. The data (D7_D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the CS line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest-order address bit is reached, the address counter will rollover to the lowest-order address bit allowing the entire memory to be read in one continuous read cycle regardless of the starting address.

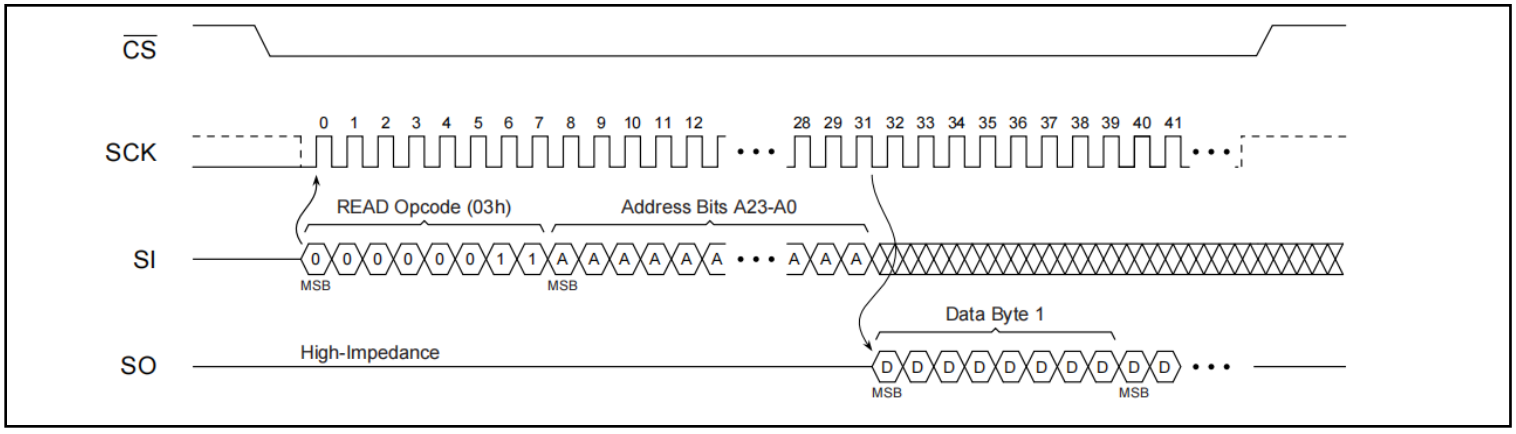


Figure9. Read Waveform

Write Sequence

In order to program the AT25M02, two separate instructions must be executed. First, the device must be write enabled via the Write Enable (WREN) instruction. Then, one of the two possible write sequences described in this section may be executed.

Note: If the device is not Write Enabled (WREN), the device will ignore the WRITE instruction and will return to the standby state when CS is brought high. A new CS assertion is required to re-initiate communication.
The address of the memory location(s) to be programmed must be outside the protected address field location selected by the block write protection level. During an internal write cycle, all commands will be ignored except the RDSR instruction. Refer to Table 14 for the address bits for AT25M02.

Table14.AT25M02 Address Bits

Address	AT25M02
A_N	A_{17}—A_0
Don't Care Bits	A_{23}—A_{18}

Byte Write

A byte write requires the following sequence and is depicted in Figure10. After the CS line is pulled low to select the device, the WRITE (02h or 07h) instruction is transmitted via the SI line followed by the 24_bit address and the data (D7_D0) to be programmed. Programming will start after the CS pin is brought high. The low_to_high transition of the CS pin must occur during the SCK low time (Mode 0) and SCK high time (Mode 3) immediately after clocking in the D0 (LSB) data bit. The AT25M02 is automatically returned to the Write Disable state (STATUS register bit WEL = 0) at the completion of a write cycle.

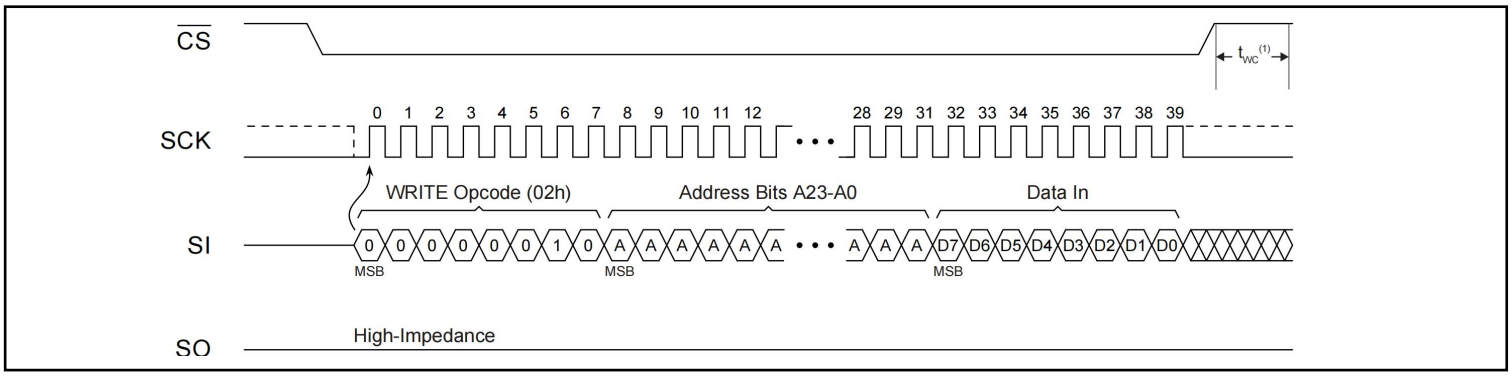


Figure10. Byte Write

Note:1. This instruction initiates a self-timed internal write cycle (t_{WC}) on the rising edge of CS after a valid sequence.

Page Write

A page write sequence allows up to 256 bytes to be written in the same write cycle, provided that all bytes are in the same row of the memory array. Partial page writes of less than 256 bytes are allowed. After each byte of data is received, the eight lowest order address bits are internally incrementedfollowing the receipt of each data byte. The higher order address bits are not incremented and retain the memory array page location. If more bytes of data are transmitted that what will fit to the end of that memory row, the address counter will rollover to thebeginningof the same row. Nevertheless, creating a rollover event should be avoided as previously loaded data in the page could become unintentionally altered. The AT25M02 is automatically returned tothe Write Disable state (WEL = 0) at the completion of a write cycle.

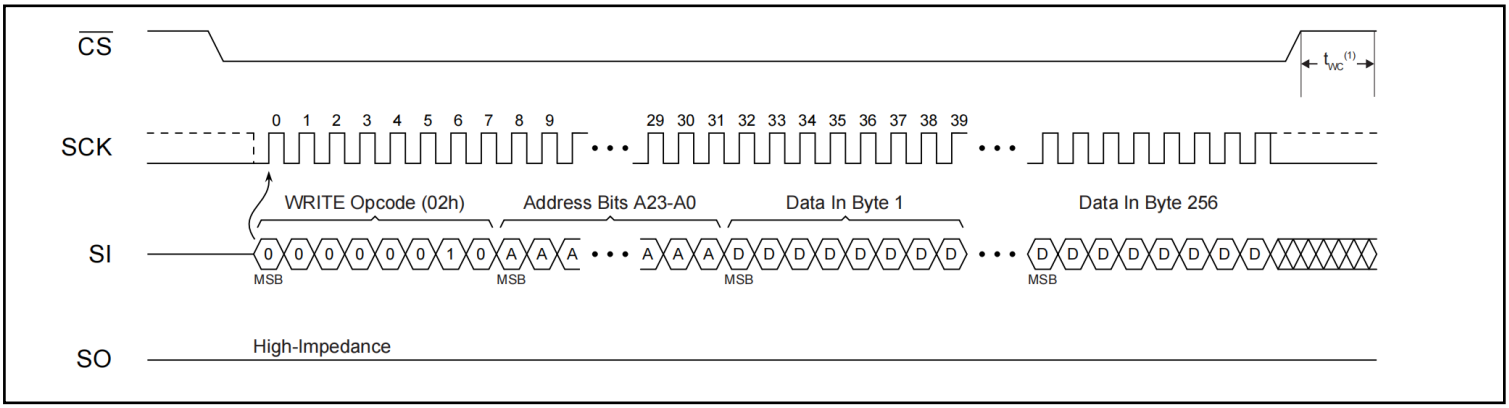


Figure11.Page Write

Note:1. This instruction initiates a self_timed internal write cycle (t_{WC}) on the rising edge of CS after a valid sequence.

Internal Writing Methodology

The AT25M02 incorporates a built-in error detection and correction (EDC) logic scheme. The EEPROM array is internally organized as a group of four connected 8-bit bytes plus an additional six ECC (Error Correction Code) bits of EEPROM. These 38 bits are referred to as the internal physical data word. During a read sequence, the EDC logic compares each 4-byte physical data word with its corresponding six ECC bits. If a single bit out of the 4-byte region reads incorrectly, the EDC logic will detect the bad bit and replace it with a correct value before the data is serially clocked out. This architecture significantly improves the reliability of the AT25M02 compared to an implementation that does not utilize EDC.

It is important to note that data is always physically written to the part at the internal physical data word level, regardless of the number of bytes written. Writing single bytes is still possible with the byte write operation, but internally, the other three bytes within that 4-byte location where the single byte was written, along with the six ECC bits will be updated. Due to this architecture, the AT25M02 EEPROM write endurance is rated at the internal physical data word level (4-byte word). The system designer needs to optimize the application writing algorithms to observe these internal word boundaries in order to reach the endurance rating.

Polling Routine

A polling routine can be implemented to optimize time?sensitive applications that would not prefer to wait the fixed maximum write cycle time (twc). This method allows the application to know immediately when the write cycle has completed to start a subsequent operation.
Once the internally-timed write cycle has started, a polling routine can be initiated. This involves repeatedly sending Read STATUS Register (RDSR) instruction to determine if the device has completed its self-timed internal write cycle. If the RDY/BSY bit (bit 0 of STATUS register) = 1, the write cycle is still in progress. If bit 0 = 0, the write cycle has ended. If the RDY/BSY bit = 1, repeated RDSR commands canbe executed until the RDY/BSY bit = 0, signaling that the device is ready to execute a new instruction. Only the Read STATUS Register (RDSR) and the Low-Power Write Poll (LPWP) instructions are is enabled during the write cycle.

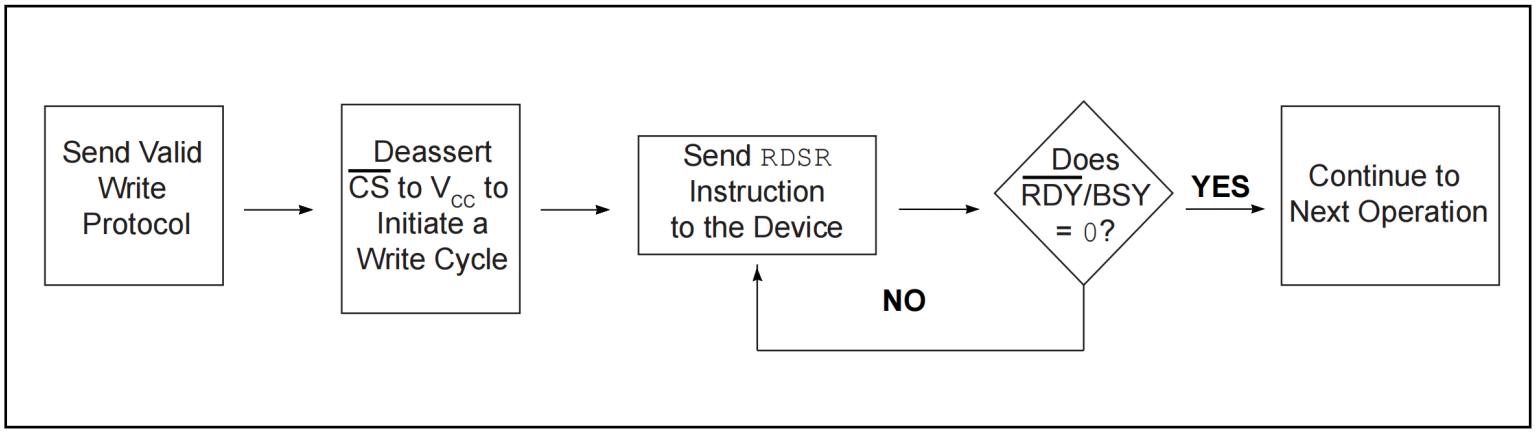


Figure 12.Polling Flowchart

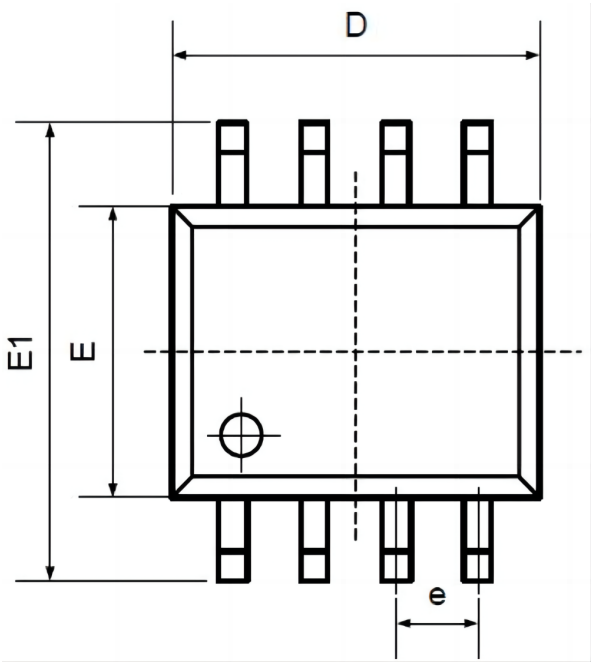
Order information

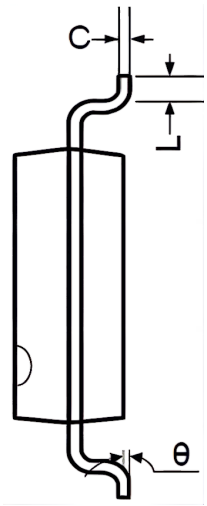
Order Number	Package	Package Quantity	Marking On The park	Temperature
AT25M02-SSHM-T-TUDI	SOP8	Tape,Reel,4000	25M02	-40°C to +85°C
			5HM	
AT25M02-SSHD-T-TUDI	SOP8	Tape,Reel,4000	25M02D	
			5HD	

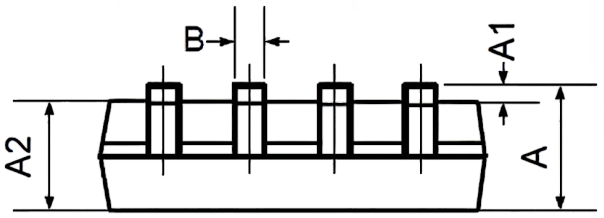
Revision history

	Date	Revision	Page
V1.0	2020/3	New	1-16
V1.1	2024/12	Update model and PDF template	1-27

Package SOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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