

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-AT24C32C/AT24C64C

2-Wire Serial EEPROM 32K (4096 x 8) 64K (8192 x 8)

网址 www.sztdbdt.com

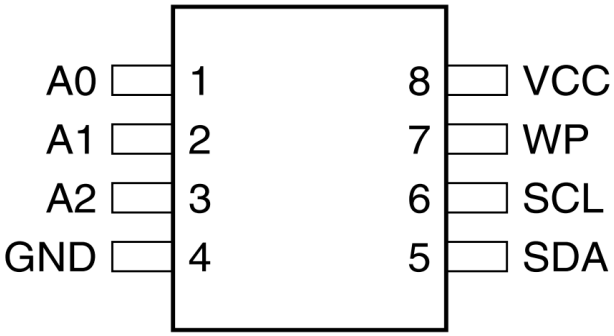
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- ●Low-voltage and Standard-voltage Operation
  - 1.8 (V_{CC} = 1.8 to 5.5V)
- ●Internally Organized 4096 x 8, 8192 x 8
- ●2-Wire Serial Interface
- ●Schmitt Trigger, Filtered Inputs for Noise Suppression
- ●Bi-directional Data Transfer Protocol
- ● 1 MHz (5.0V) and 400 KHz (1.8V Compatibility)
- ●Write Protect Pin for Hardware Data Protection
- ●32-Byte Page Write Mode (Partial Page Writes Allowed)
- ●Self-Timed Write Cycle (5 ms max)
- ●High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- ●Lead-free/Halogen-free Devices
- ●8-lead PDIP, 8-lead JEDEC SOIC Packages.
- ●Die Sales: Wafer Form, Waffle Pack, and Bumped Wafers



SOP8/DIP8

Description

The AT24C32C/64C provides 32,768/65,536 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 4096/8192 words of 8 bits each. The device ’ s cascadable feature allows up to 8 devices to share a common 2- wire bus. The device is optimized for use in many industrial and commercial applica-tions where low power and low voltage operation are essential. The AT24C32C/64C is available in space saving 8-lead PDIP, 8-lead JEDEC SOIC packages and is accessed via a 2-wire serial interface. In addition, theentire family is available in 1.8V (1.8 to 5.5V) version.

Pin Configurations

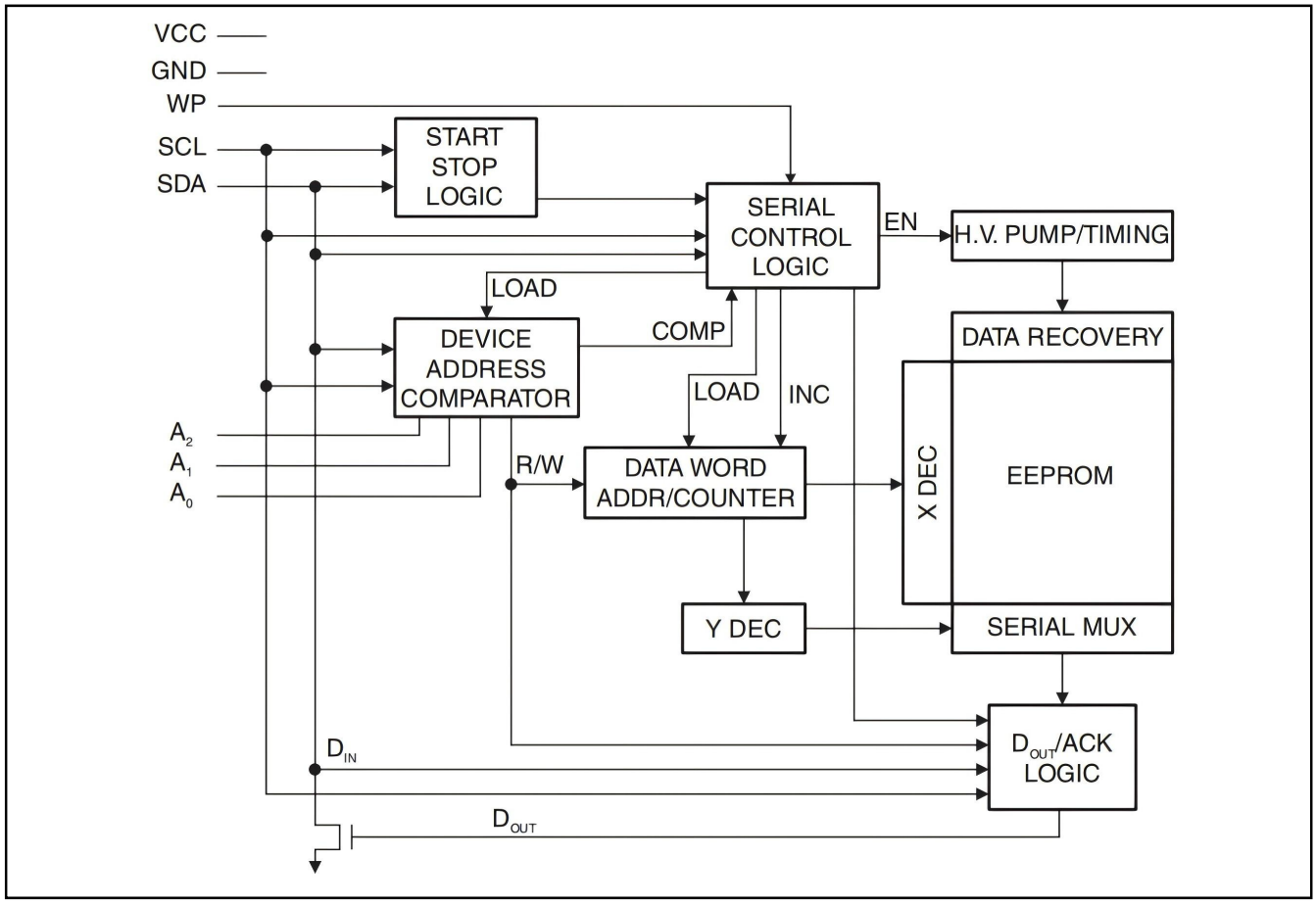
Pin Name	Function
A0-A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

Absolute Maximum Ratings

Operating Temperature..... -55 to +125°C
Storage Temperature ..... -65 to +150°C
Voltage on Any Pin
with Respect to Ground ..... -1.0 to +7.0V
Maximum Operating Voltage 6.25V
DC Output Current..... 5.0 mA

NOTICE: Stresses beyond those listed under “ Absolute Maximum Ratings ” may cause permanent dam-age to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in th operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired or left not connected for hardware compatibility with other AT24CXX devices. When the pins are hardwired, as many as eight 32K/64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). If the pins are left floating, the A2, A1 and A0 pins will be internally pulled down to GND if the capaci-tive coupling to the circuit board V_{cc} plane is <3pF. If coupling is >3pF, TUDI recommends connecting the address pins to GND.

WRITE PROTECT (WP): The write protect input, when connected to GND, allows normal write operations. When WP is connected high to V_{cc}, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive cou-pling to the circuit board V_{cc} plane is <3pF. If coupling is >3pF, Atmel recommends connecting the pin to GND.

Memory Organization

AT24C32C/64C, 32/64K SERIAL EEPROM: The 32K/64K is internally organized as 128/256 pages of 32 bytes each. Random word addressing requires a 12/13 bit data word address.

Pin Capacitance(1)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V to 5.5V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$=0V
C_{IN}	Input Capacitance(A_0, A_1, A_2,SCL)	6	pF	V_{IN}=0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40 to +85°C, V_{CC} = +1.8 to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
I_{CC1}	Supply Current	V_{cc}=5.0V	READ at 400 kHz		0.4	1.0	mA
I_{CC2}	Supply Current	V_{cc}=5.0V	WRITE at 400 kHz		2.0	3.0	mA
I_{SB1}	Standby Current (1.8V option)	V_{cc}=1.8V	VIN=V_{cc} or V_{SS}			1.0	µA
		V_{cc}=5.5V				6.0	µA
I_{LI}	Input Leakage Current V_{cc}=5.0V	V_{IN}=V_{cc} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current V_{cc}=5.0V	V_{OUT}=V_{cc} or V_{SS}			0.05	3.0	µA
V_{IL}	Input Low Level(1)			-0.6		V_{cc}×0.3	V
V_{IH}	Input High Level(1)			V_{cc}×0.7		V_{cc}+0.5	V
V_{OL2}	Output Low Level	V_{cc}=3.0V	I_{OL}=2.1 mA			0.4	V
V_{OL1}	Output Low Level	V_{cc}=1.8V	I_{OL}=0.15mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_{AI} = -40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	1.8-volt		5.0-volt		
		Min	Max	Min	Max	Units
f_{SCL}	Clock Frequency,SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3		0.4		μs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		μs
t_i	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.05	0.9	0.05	0.55	μ s
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1.3		0.5		μs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		μs
$t_{SU.STA}$	Start Set-up Time	0.6		0.25		μ s
$t_{HD.DAT}$	Data In Hold Time	0		0		μs
$t_{SU.DAT}$	Data In Set-up Time	100		100		ns
t_R	Inputs Rise Time(1)		0.3		0.3	μs
t_F	Inputs Fall Time(1)		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		0.25		μs
t_{DH}	Data Out Hold Time	50		50		ns
t_W	Write Cycle Time		5		5	ms
Endurance(1)	25℃,Page Mode,3.3V	1,000,000				Write Cycles

Notes: 1. This parameter is ensured by characterization.
2. AC measurement conditions:
R_L (connects to V_{cc}): 1.3 kΩ (2.5V, 5.0V), 10 kΩ (1.8V)
Input pulse voltages: 0.3 V_{CC} to 0.7 V_{cc}
Input rise and fall times: ≤ 50 ns
Input and output timing reference voltages: 0.5 V_{cc}

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Valid-ity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowl-edge that it has received each word.

STANDBY MODE: The AT24C32C/64C features a low power standby mode which is enabled: a) upon power-up and b) after the receipt of the Stop bit and the completion of any internal operations.

SOFTWARE RESET: After an interruption in protocol, power loss or system reset, and 2-wire part can be protocol reset by following these steps: (a) Create a start bit condition, (b) clock 9 cycles, (c) create another start bit followed by stop bit condition as shown below. The device is ready for next communication after above steps have been completed.

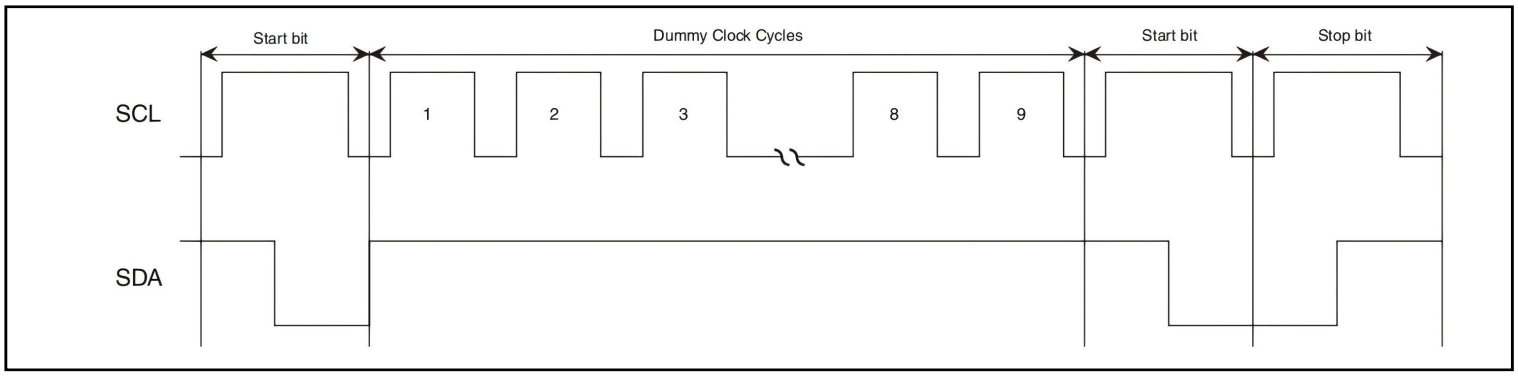


Figure 1. Software Reset

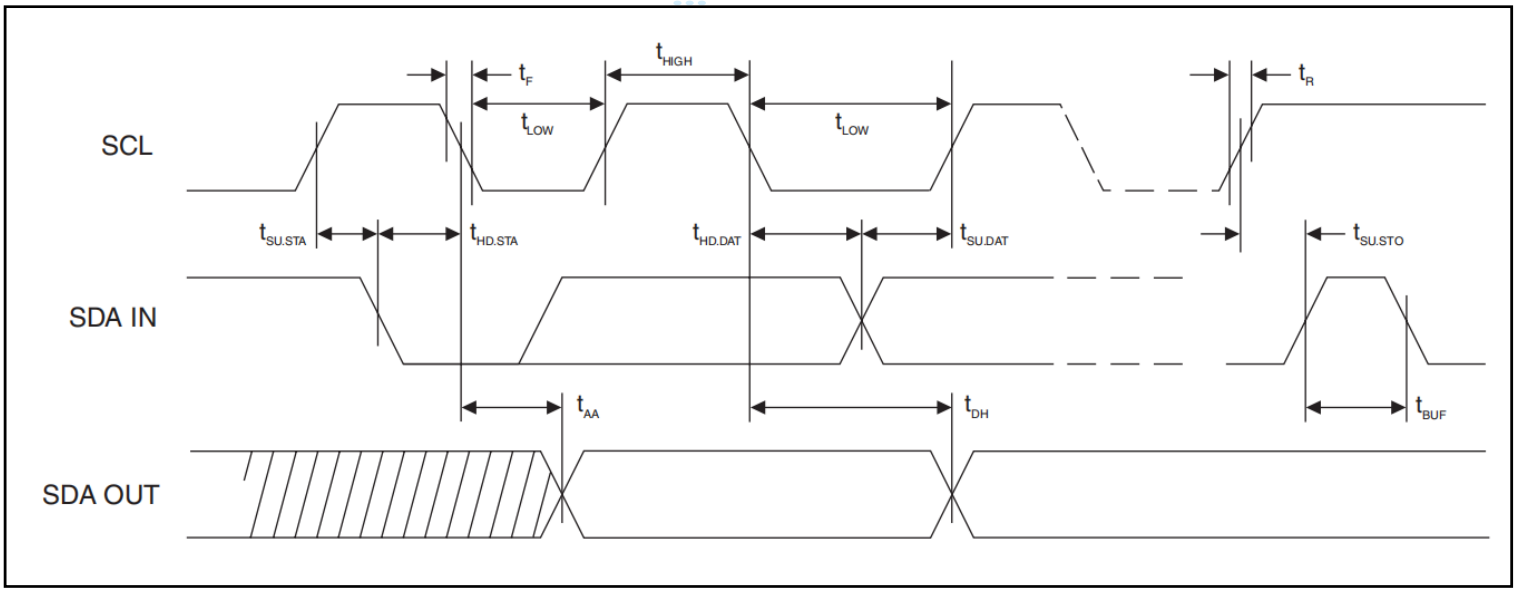


Figure 2.Bus Timing

SCL: Serial Clock, SDA: Serial Data I/O

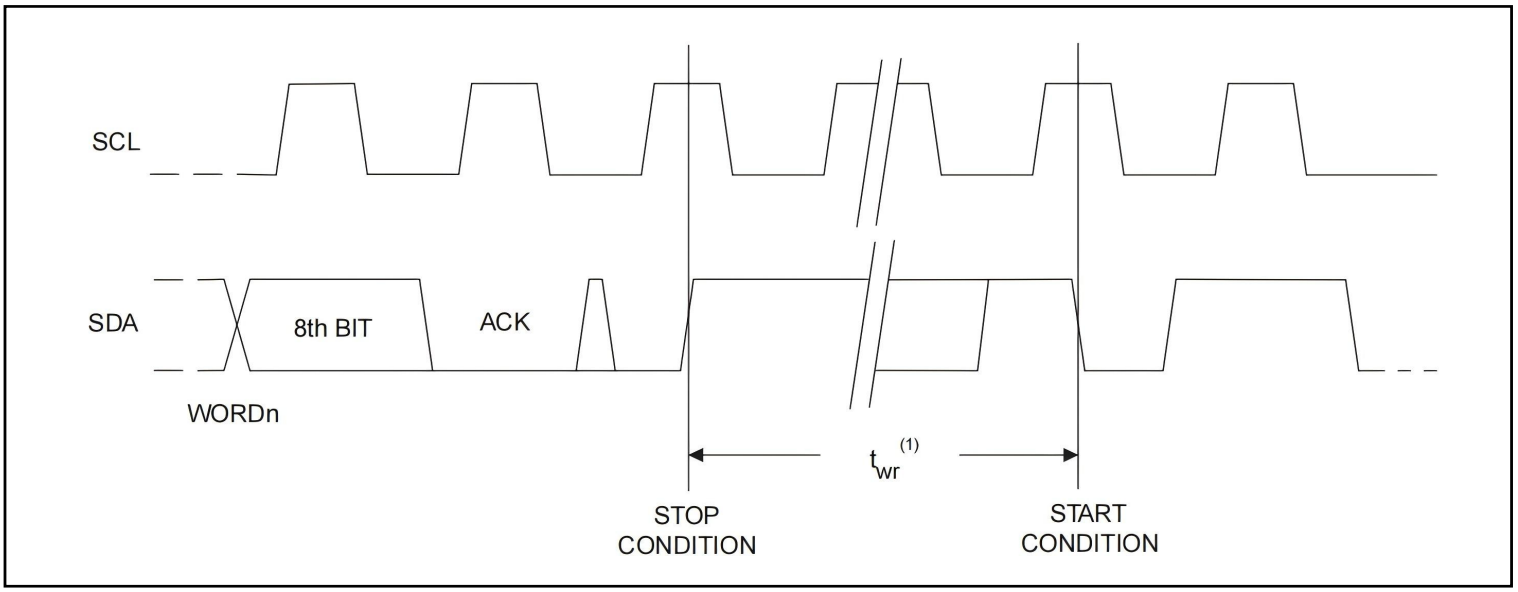


Figure 3.Write Cycle Timing

SCL: Serial Clock, SDA: Serial Data I/O

Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

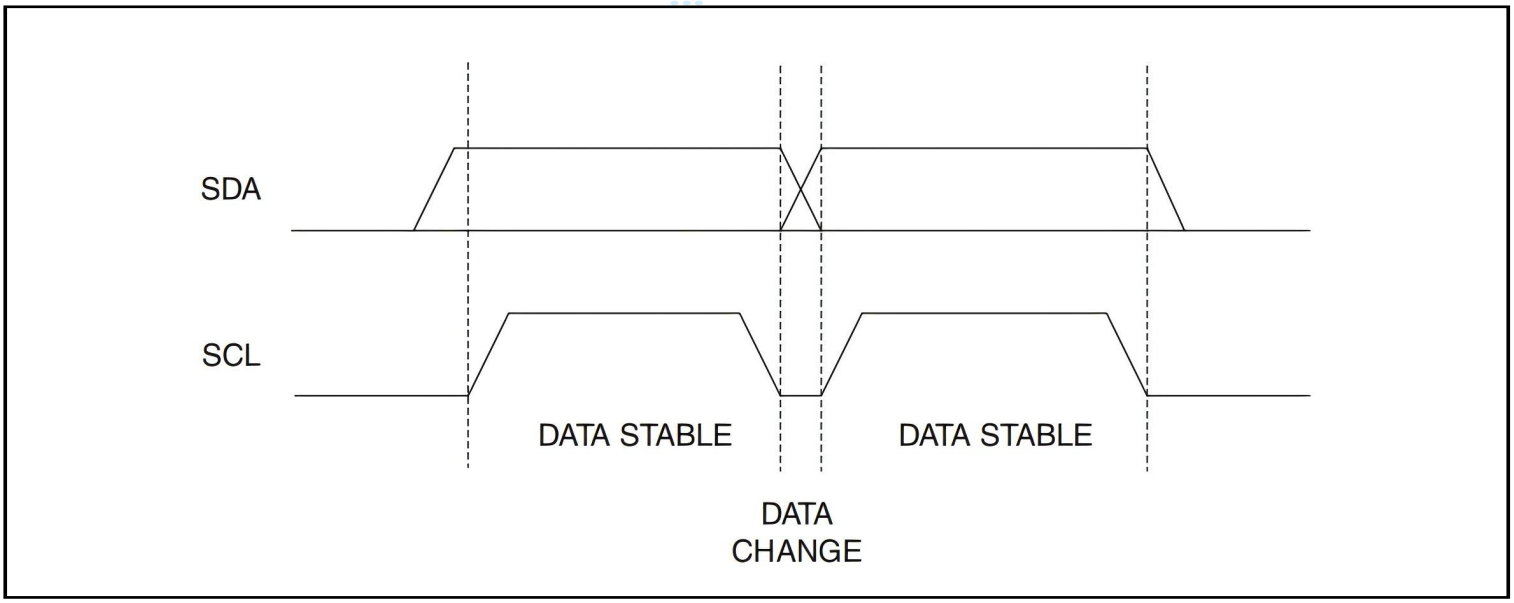


Figure 4.Data Validity

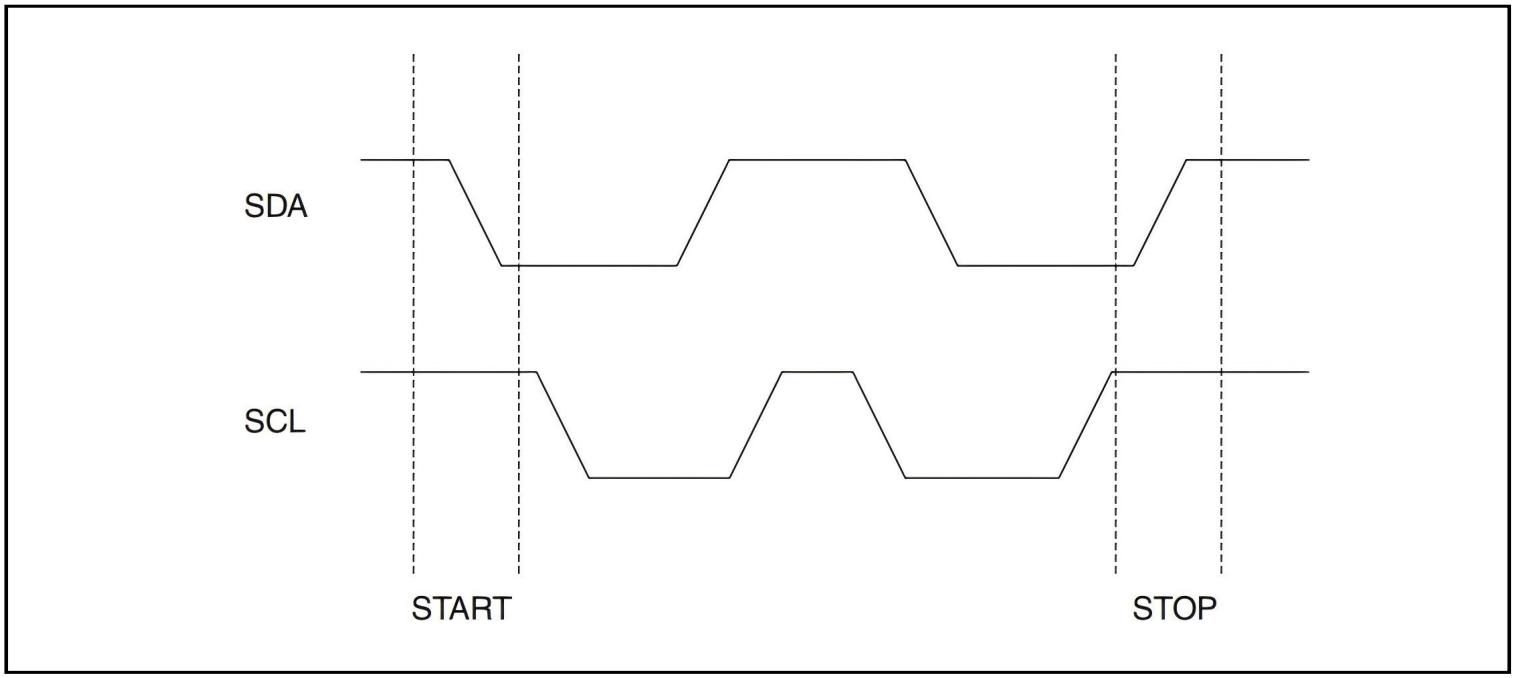


Figure 5.Start and Stop Definition

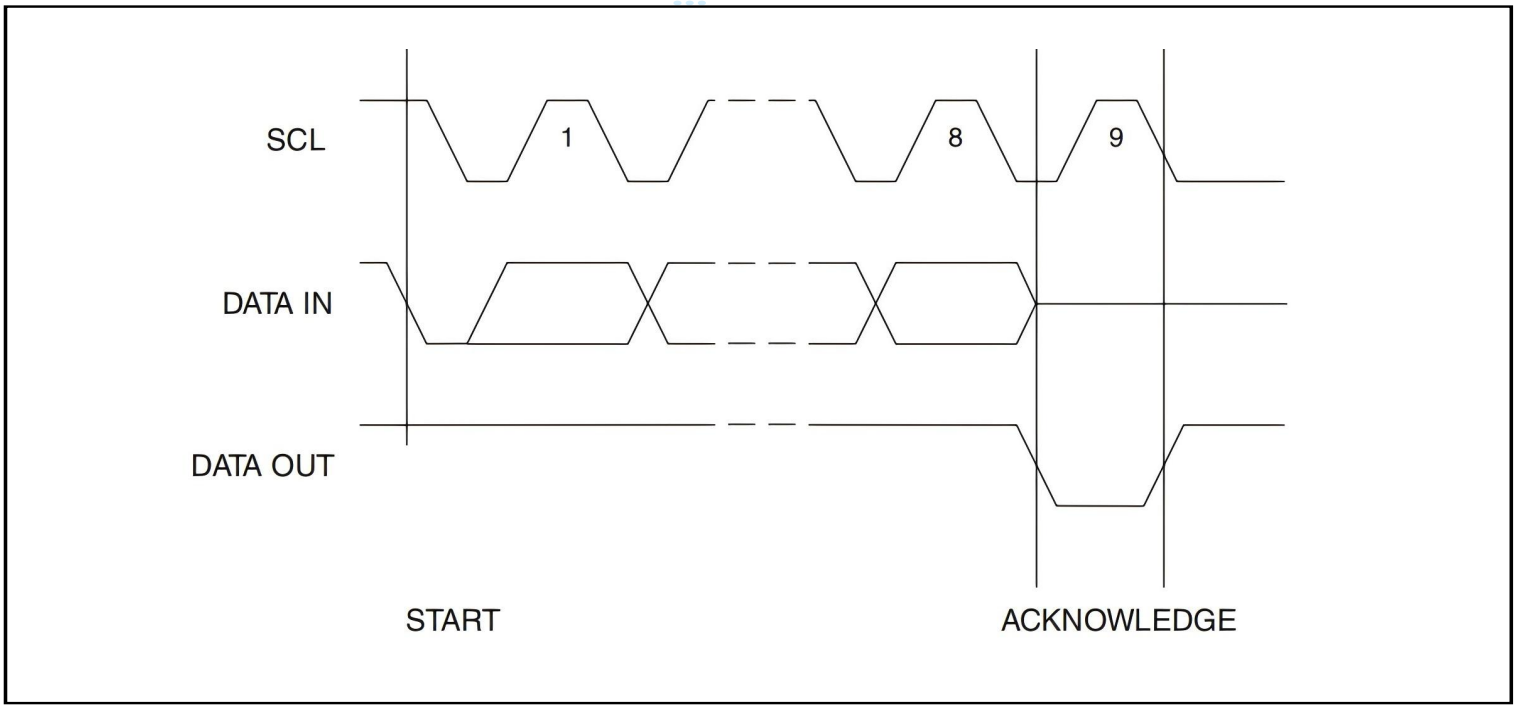


Figure 6.Output Acknowledge

Device Addressing

The 32K/64K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 7). The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is commo to all 2-wire EEPROM devices.

The 32K/64K uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A2, A1, and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is ini -tiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to standby state.

DATA SECURITY: The AT24C32C/64C has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at V_{CC}.

Write Operations

BYTE WRITE: A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and theEEPROM will not respond until the write is complete (see Figure 8).

PAGE WRITE: The 32K/64K EEPROM is capable of 32-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must ter-minate the page write sequence with a stop condition (see Figure 9).

The data word address lower 5 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the follow-ing byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will “ roll over ” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/ write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “ roll over ” during read is from the last byte of the last memory page, to the first byte of the first page. The address “ roll over ” during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see Figure 10).

Read Operations

RANDOM READ: A random read requires a “ dummy ” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/ write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a follow-ing stop condition (see Figure 11).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a ran-dom address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “ roll over ” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 12).

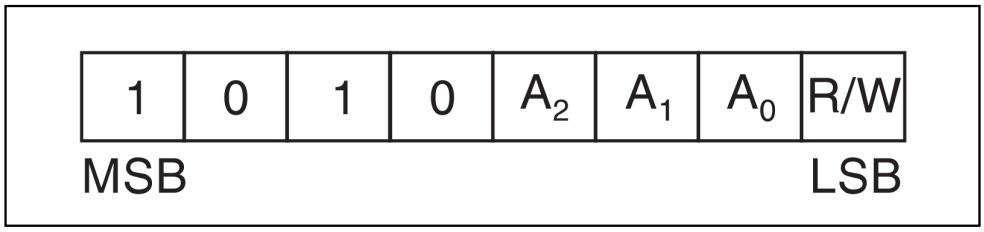


Figure 7. Device Address

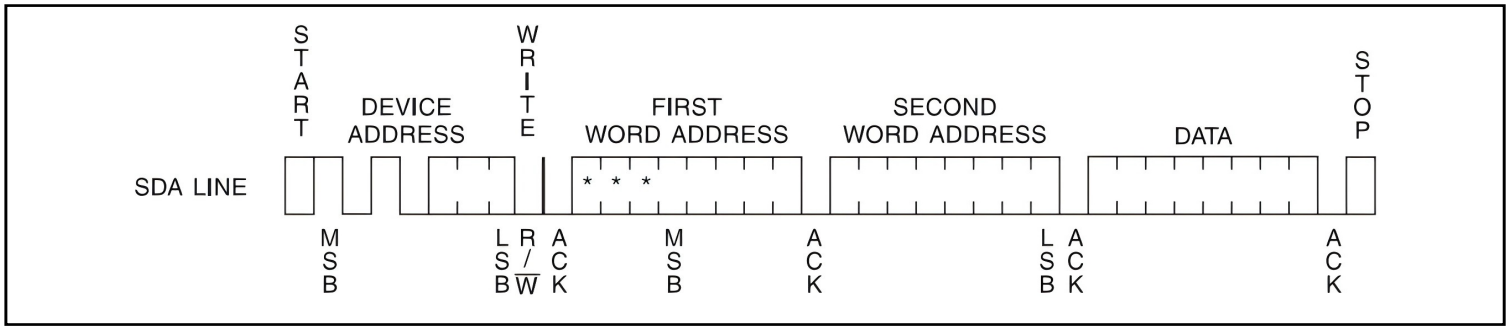


Figure 8. Byte Write

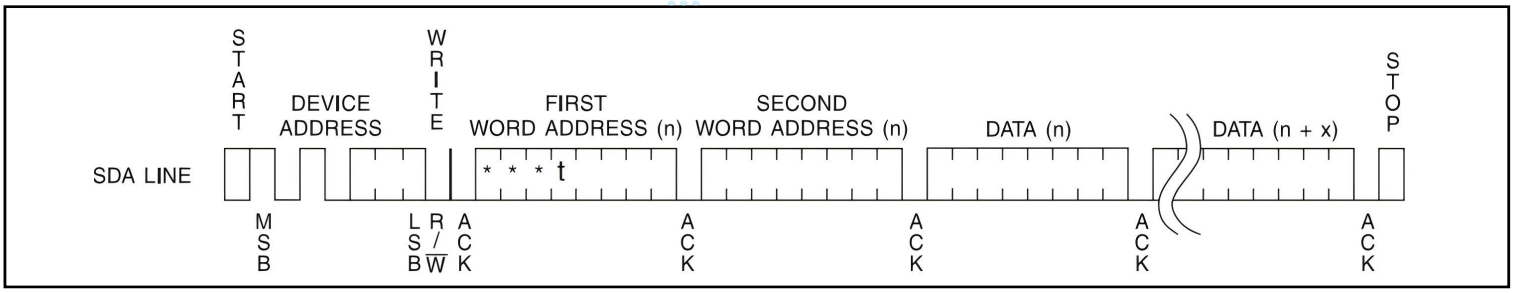


Figure 9. Page Write

Note: 1. * = DON ’ T CARE bits
2. t = DON ’ T CARE bit for AT24C32C

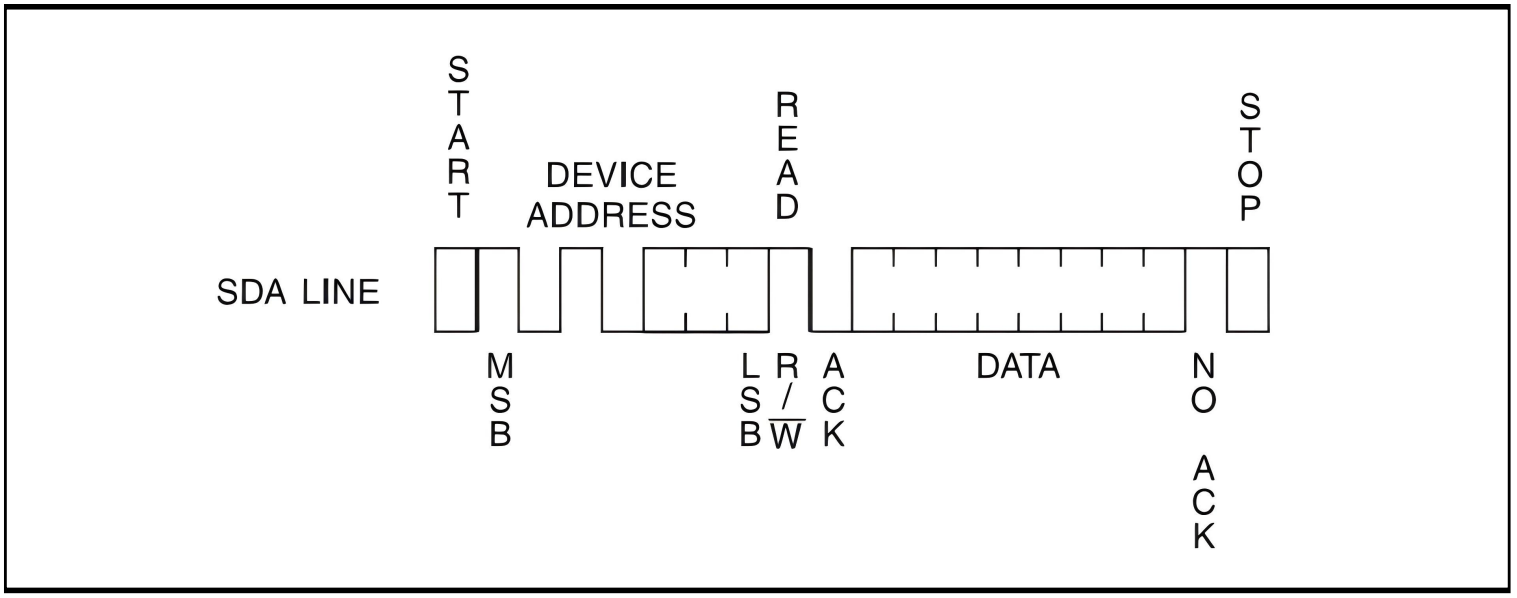


Figure 10. Current Address Read

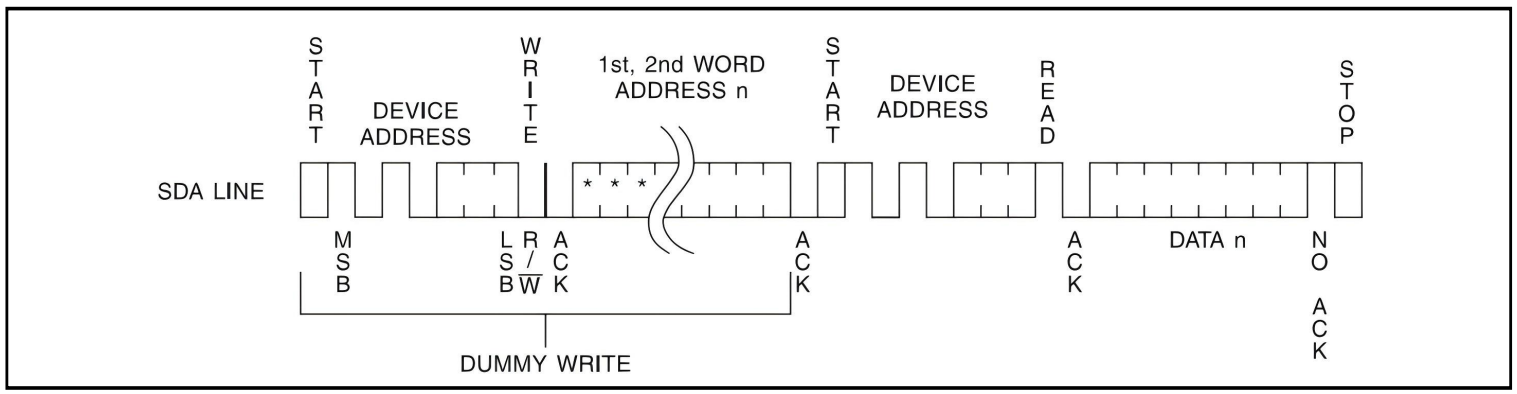


Figure 11. Random Read

Note: 1. * = DON ’ T CARE bits

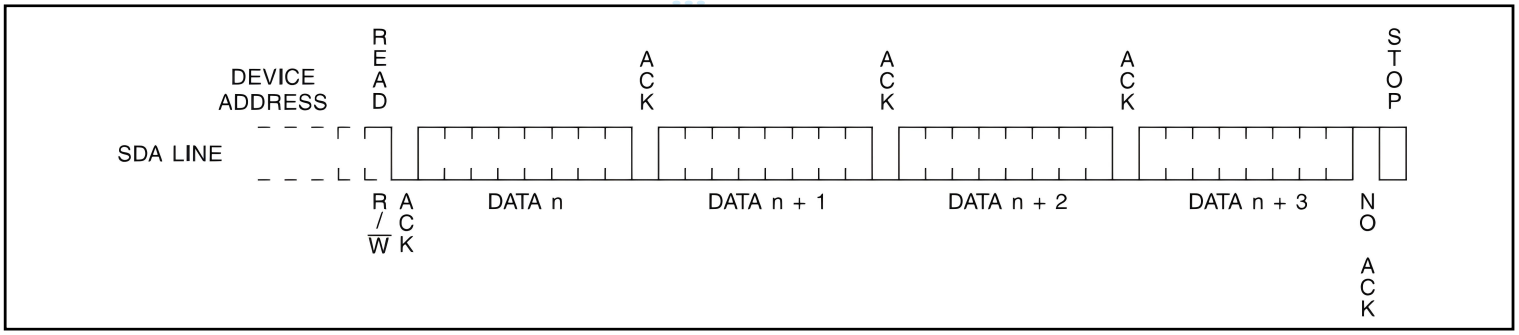


Figure 12. Sequential Read

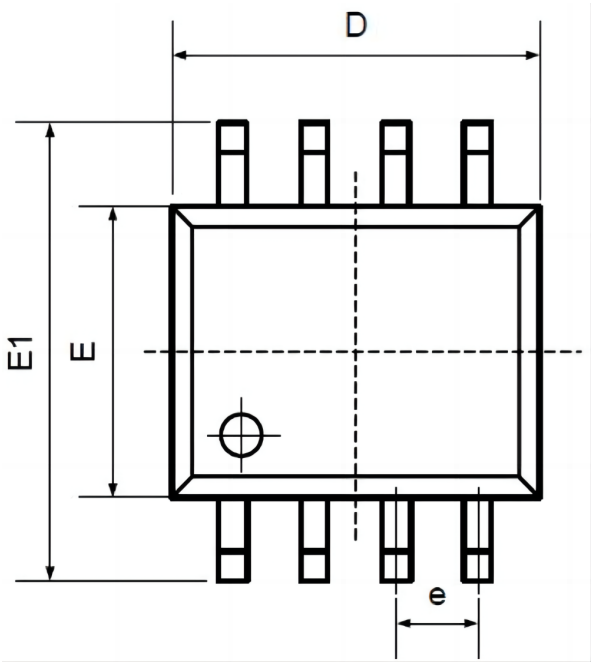
Order information

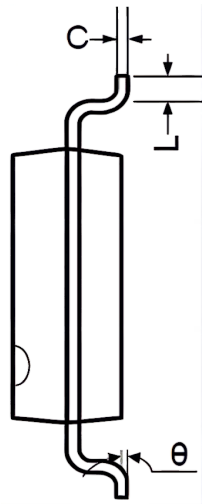
Order Number	Package	Package Quantity	Marking On The park	Temperature
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AT24C32CN-SH-T-TUDI	SOP8	Tape,Reel,4000	32C1	
AT24C64C-PU-TUDI	DIP8	Tube,50,A box of 2000	24C64C-PU	
AT24C64CN-SH-T-TUDI	SOP8	Tape,Reel,4000	64C1	

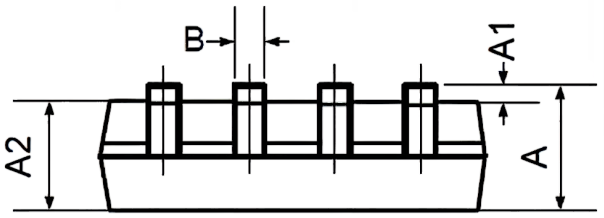
Revision history

	Date	Revision	Page
V1.0	2022/5	New	1-13
V1.1	2025/1	Update model and PDF template	1-18

Package SOP8

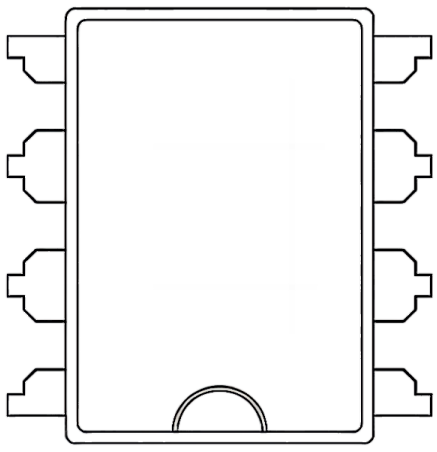


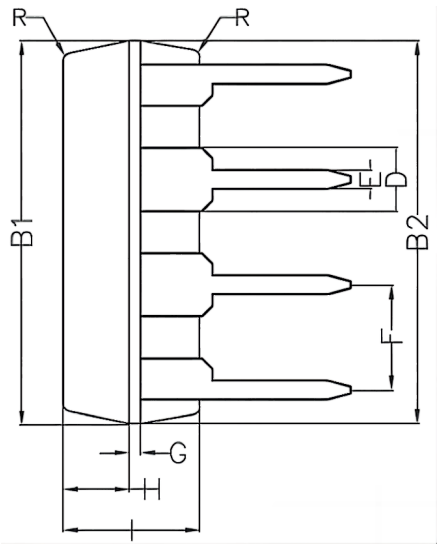


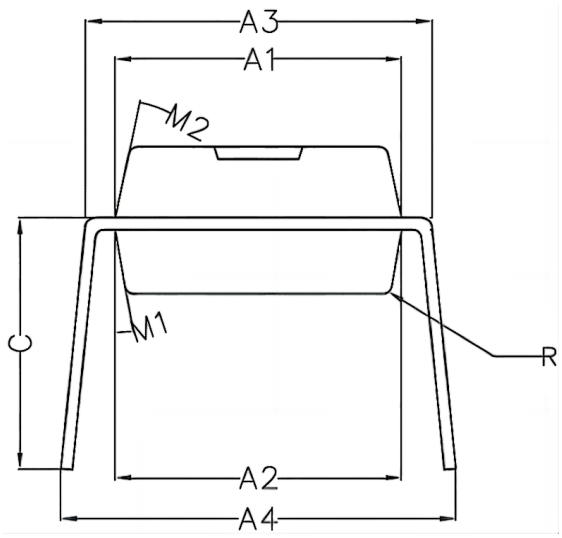


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8







Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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