

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-CAT24C128

128 kb I^2C CMOS Serial EEPROM

网址 www.sztdbdt.com

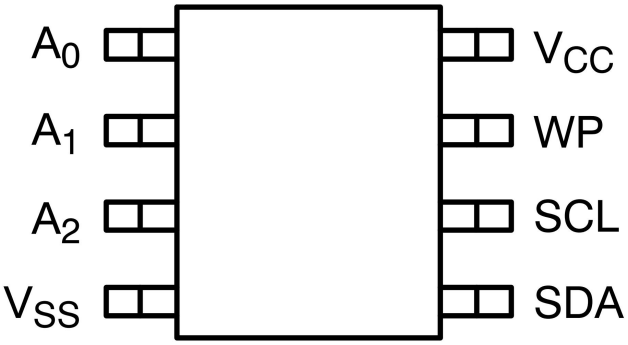
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Supports Standard, Fast and Fast?Plus I2C Protocol
- 1.8 V to 5.5 V Supply Voltage Range
- 64-Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I^2C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- 8-lead PDIP, SOIC and TSSOP Packages



SOP8/DIP8/TSSOP8

Description

The CAT24C128 is a 128 kb Serial CMOS EEPROM, internally organized as 16,384 words of 8 bits each. It features a 64-byte page write buffer and supports both the Standard (100 kHz), Fast (400 kHz) and Fast-Plus (1 MHz) I^2C protocol. Write operations can be inhibited by taking the WP pin High (this protects the entire memory). On-Chip ECC (Error Correction Code) makes the device suitable for high reliability applications.*

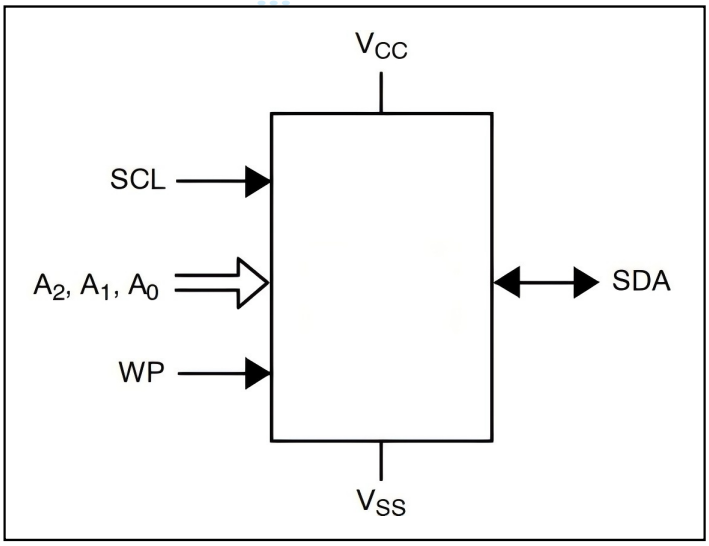


Figure 1. Functional Symbol

PIN FUNCTION

Pin Namet	Function
Ao,A1,A_2	Device Address Inputs
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect Input
V_{cc}	Power Supply
V_{ss}	Ground

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Storage Temperature	-65 to +150	℃
Voltage on Any Pin with Respect to Ground (Note 1)	-0.5 to +6.5	V

Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The DC input voltage on any pin should not be lower than-0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
NEND (Notes 3,4)	Endurance	1,000,000	Program/Erase Cycles
TDR	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
3. Page Mode, V_{CC} = 5 V, 25°C
4. The new product revision (C) uses ECC (Error Correction Code) logic with 6 ECC bits to correct one bit error in 4 data bytes. Therefore, when a single byte has to be written, 4 bytes (including the ECC bits) are re?programmed. It is recommended to write by multiple of 4 bytes in order to benefit from the maximum number of write cycles.

Table 3. D.C. OPERATING CHARACTERISTICS - Mature Product (Rev B)

(V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CCR}	Read Current	Read,fscL=400 kHz			1	mA
I_{CCW}	Write Current	Write,fscL=400 kHz			3	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}	T_A=-40℃ to+85℃		1	μA
			T_A=-40℃ to+125℃		2	
I_L	I/O Pin Leakage	Pin at GND or V_{CC}	T_A=-40℃ to+85℃		1	μA
			T_A=-40℃ to+125℃		2	
V_{IL}	Input Low Voltage			-0.5	V_{CC}×0.3	V
V_{IH}	Input High Voltage			V_{CC}x0.7	V_{CC}+0.5	V
V_{OL1}	Output Low Voltage	V_{CC}≥2.5V,I_{OL}=3.0 mA			0.4	V
V_{OL2}	Output Low Voltage	V_{CC}<2.5 V,I_{OL}=1.0 mA			0.2	V

Table 4. PIN IMPEDANCE CHARACTERISTICS - Mature Product (Rev B)

(V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
C_{IN}(Note 5)	SDA I/O Pin Capacitance	V_{IN}=0V	8	pF
CIn(Note 5)	Input Capacitance (other pins)	V_{IN}=0V	6	pF
I_{WP}(Note 6)	WP Input Current	V_{IN}<V_{IH}	200	μA
		V_{IN}>V_{IN}	1	μA

5. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
6. When not driven, the WP pin is pulled down to GND internally. For improved noise immunity, the internal pull-down is relatively strong;therefore the external driver must be able to supply the pull-down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0. 0.5 x V_{CC}), the strong pulldown reverts to a weak current source.

Table 5. D.C. OPERATING CHARACTERISTICS -New Product (Rev C) (Note 7)

(V_{CC}= 1.8 V to 5.5 V, T_A= -40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = -40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Max	Units
C_{CR}	Read Current	Read,f_{SCL}=400 kHz/1 MHz			1	mA
I_{CCW}	Write Current				3	mA
I_{SB}	Standby Current	All /O Pins at GND or V_{CC}	T_A=-40°C to +85°C		2	μA
			T_A=-40°C to+125°C		5	
I_L	I/O Pin Leakage	Pin at GND or V_{CC}	T_A=-40°C to +85°C		1	μA
			T_A=-40°C to+125°C		2	
V_{IL1}	Input Low Voltage	2.5V≤V_{CC}≤5.5V		-0.5	0.3 V_{CC}	V
V_{IL2}	Input Low Voltage	1.8V≤V_{CC}<2.5V		-0.5	0.25 V_{CC}	V
V_{IH1}	Input High Voltage	2.5V≤V_{CC}≤5.5V		0.7 V_{CC}	V_{CC}+0.5	V
V_{IH2}	Input High Voltage	1.8V≤V_{CC}<2.5V		0.75 V_{CC}	V_{CC}+0.5	V
V_{OL1}	Output Low Voltage	V_{CC}≥2.5V,I_{OL}=3.0 mA			0.4	V
V_{OL2}	Output Low Voltage	V_{CC}<2.5 V,I_{OL}=1.0 mA			0.2	V

Table 6. PIN IMPEDANCE CHARACTERISTICS - New Product (Rev C) (Note 7)

(V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to +85°C and V_{CC}= 2.5 V to 5.5 V, T_A = -40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
CIn(Note 8)	SDA I/O Pin Capacitance	V_{IN}=0V	8	pF
CIn(Note 8)	Input Capacitance (other pins)	V_{IN}=0V	6	pF
Iwp,IA(Note 9)	WP Input Current,Address InputCurrent (A_0,A_1,A_2)	V_{IN}<V_{IH},V_{cc}=5.5V	75	µA
		V_{IN}<V_{IH},V_{cc}=3.3V	50	
		V_{IN}<V_{IH},V_{cc}=1.8V	25	
		V_{IN}>V_{IH}	2	

7. The product Rev C is identified by letter “C” or dedicated marking code on top of the package.
8. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
9. When not driven, the WP, A0, A1, A2 pins are pulled down to GND internally. For improved noise immunity, the internal pull-down is relatively strong; therefore the external driver must be able to supply the pull-down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull-down reverts to a weak current source.

Table 7. A.C. CHARACTERISTICS

(V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = -40°C to +125°C) (Note 10)

Symbol	Parameter	Standard V_{cc}=1.8V-5.5V		FastV_{cc}=1.8V-5.5V		Fast-Plus(Note 13)V_{cc}=2.5V-5.5VTA=-40°°C to +85°C		Units
		Min	Max	Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400		1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		0.25		µs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		0.45		µs
t_{HIGH}	High Period of SCL Clock	4		0.6		0.40		µs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		0.25		µs

Table 7. A.C. CHARACTERISTICS (Continue)

Symbol	Parameter	Standard V_{CC}=1.8V-5.5V		Fast V_{CC}=1.8V-5.5V		Fast-Plus(Note 13)V_{CC}=2.5V-5.5VTA=-40°°C to +85°C		Units
		Min	Max	Min	Max	Min	Max	
$t_{HD:DAT}$	Data In Hold Time	0		0		0		μ s
$t_{SU:DAT}$	Data In Setup Time	250		100		50		ns
t_R(Note 11)	SDA and SCL Rise Time		1,000		300		100	ns
t_F(Note 11)	SDA and SCL Fall Time		300		300		100	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		0.25		μ s
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9		0.40	μ s
t_{DH}	Data Out Hold Time	100		100		50		ns
T_i(Note 11)	Noise Pulse Filtered at SCL and SDA Inputs		100		100		50	ns
$t_{SU:WP}$	WP Setup Time	0		0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		1		μs
t_{WR}	Write Cycle Time		5		5		5	ms
t_{PU}(Notes 11,12)	Power-up to Ready Mode		1		1	0.1	1	ms

10.Test conditions according to “ A.C. Test Conditions ” table.
11. Tested initially and after a design or process change that affects this parameter.
12.tPU is the delay between the time V_{CC} is stable and the device is ready to accept commands.
13.Fast-Plus (1 MHz) speed class available for new product revision “ C ”. The die revision “ C ” is identified by letter “ C ” or a dedicated marking code on top of the package.

Table 8. A.C. TEST CONDITIONS

Input Levels	Input Rise and Fall Times	Input Reference Levels	Output Reference Levels	Output Load
0.2×Vcc to 0.8×Vcc	≤50 ns	0.3×Vcc, 0.7×Vcc	0.5×Vcc	Current Source:I_{OL}=3mA(Vcc≥2.5V);I_{OL}=1mA(Vcc<2.5V); C_L=100 pF

Power-On Reset (POR)

The CAT24C128 incorporates Power-On Reset (POR) circuitry which protects the device against powering up in the wrong state. The CAT24C128 will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi-directional POR feature protects the device against ‘brown-out’ failure following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master.
SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.
A0, A1 and A2: The Address pins accept the device address. When not driven, these pins are pulled LOW internally.
WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. When not driven, this pin is pulled LOW internally.

Functional Description

The CAT24C128 supports the Inter-Integrated Circuit (I2C) Bus data transmission protocol,which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24C128 acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 8 devices may be connected to the bus as determined by the device address inputs A0, A1, and A2.

I²C Bus Protocol

The I²C bus consists of two ‘wires’, SCL and SDA. The two wires are connected to the V_{CC} supply via pull-up resistors. Master and Slave devices connect to the 2-wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to ‘transmit’ a ‘0’ and releases it to ‘transmit’ a ‘1’. Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics). During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 2). The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a ‘wake-up’ call to all receivers. Absent a START, a Slave will not respond to commands. The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH.

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations (Figure 3). The next 3 bits, A2, A1 and A0, select one of 8 possible Slave devices and must match the state of the external address pins. The last bit, R/W, specifies whether a Read (1) or Write (0) operation is to be performed.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 4). The Slave will also acknowledge all address bytes and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9th clock cycle. As long as the Master acknowledges the data, the Slave will continue transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by issuing a STOP condition. Bus timing is illustrated in Figure 5.

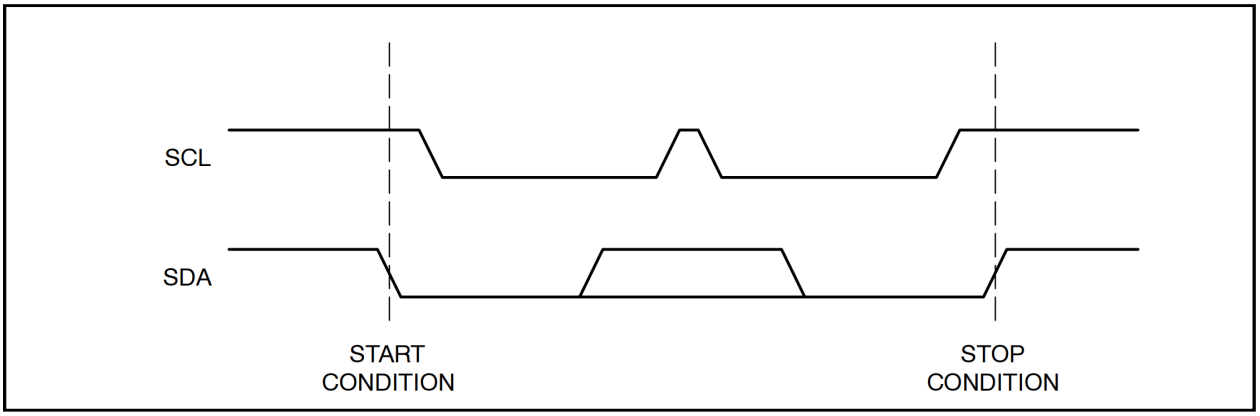


Figure 2. START/STOP Conditions

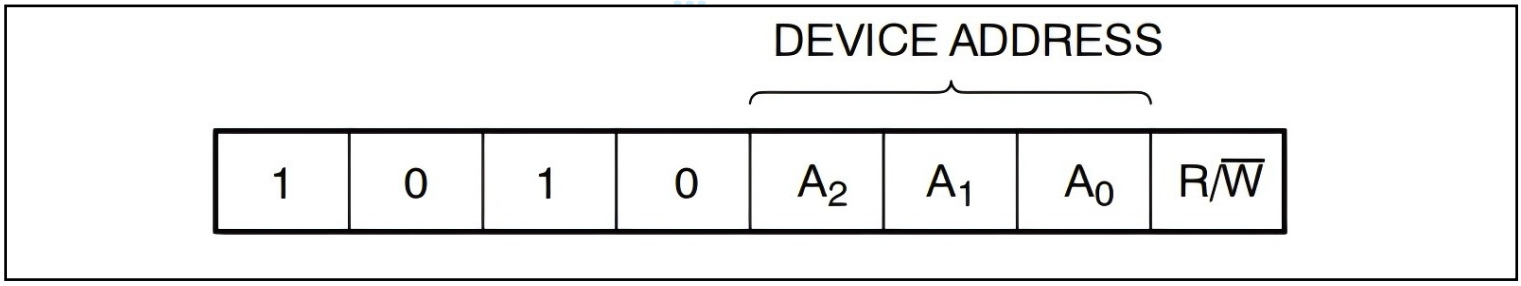


Figure 3. Slave Address Bits

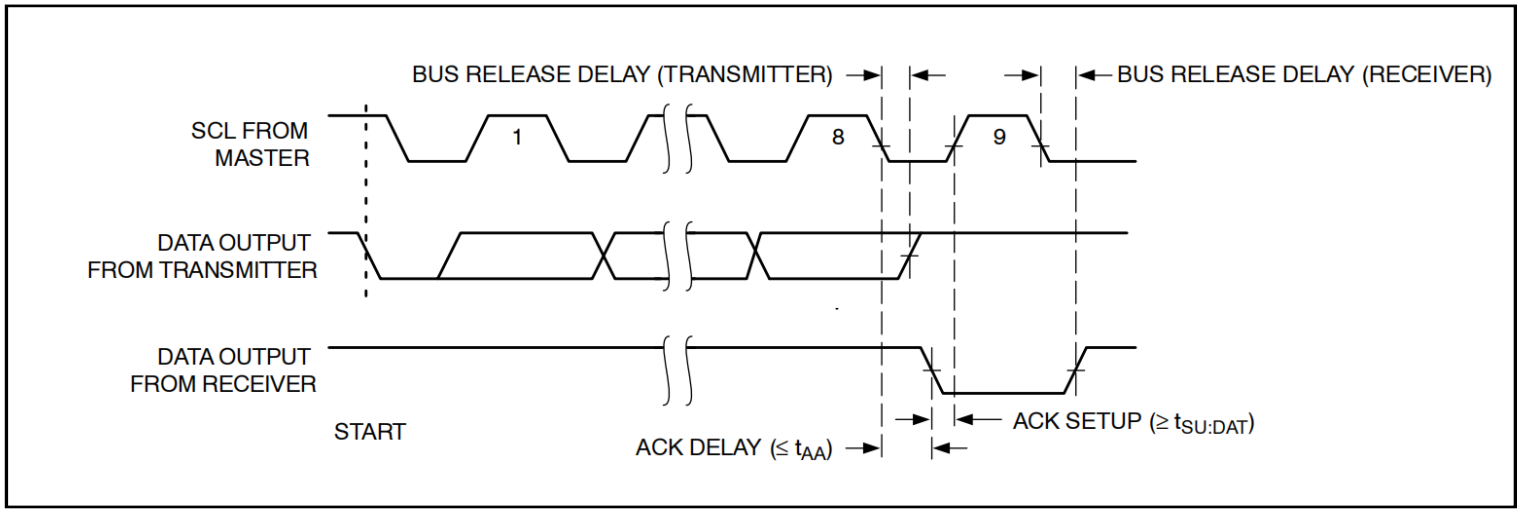


Figure 4. Acknowledge Timing

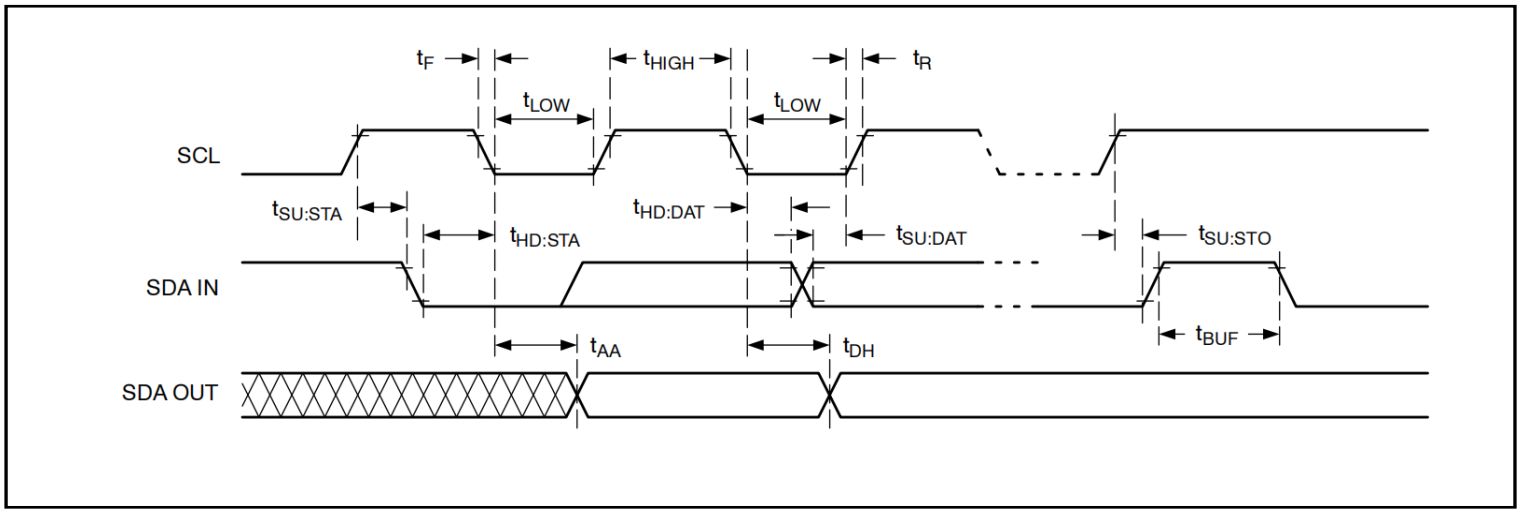


Figure 5. Bus Timing

Write Operations

Byte Write：Upon receiving a Slave address with the R/W bit set to ‘0’, the CAT24C128 will interpret the next two bytes as address bytes. These bytes are used to initialize the internal address counter;the 2 most significant bits are ‘don’t care’, the next 8 point to one of 256 available pages and the last 6 point to a location within a 64 byte page. A byte following the address bytes will be interpreted as data. The data will be loaded into the Page Write Buffer and will eventually be written to memory at the address specified by the 14 active address bits provided earlier.The CAT24C128 will acknowledge the Slave address, address bytes and data byte. The Master then starts the internal Write cycle by issuing a STOP condition (Figure 6). During the internal Write cycle (tWR), the SDA output will be tri?stated and additional Read or Write requests will be ignored (Figure 7).

Page Write： By continuing to load data into the Page Write Buffer after the 1st data byte and before issuing the STOP condition, up to 64 bytes can be written simultaneously during one internal Write cycle (Figure 8). If more data bytes are loaded than locations available to the end of page, thenloading will continue from the beginning of page, i.e. the page address is latched and the address countau tomatically increments to and then wraps-around at the page boundary. Previously loaded data ca nthus be overwritten by new data. What is eventually written to memory reflects the latest Page Write Buffer contents. Only data loaded within the most recentPage Write sequence will be written to memory.

Acknowledge Polling： The ready/busy status of the CAT24C128 can be ascertained by sending Read or Write requests immediately following the STOP condition that initiated the internal Write cycle. As long as internal Write is in progress, the CAT24C128 will not acknowledge the Slave address.

Hardware Write Protection：With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAT24C128. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the CAT24C128 will not acknowledge the data byte and the Write request will be rejected.

Delivery State：The CAT24C128 is shipped erased, i.e., all bytes are FFh.

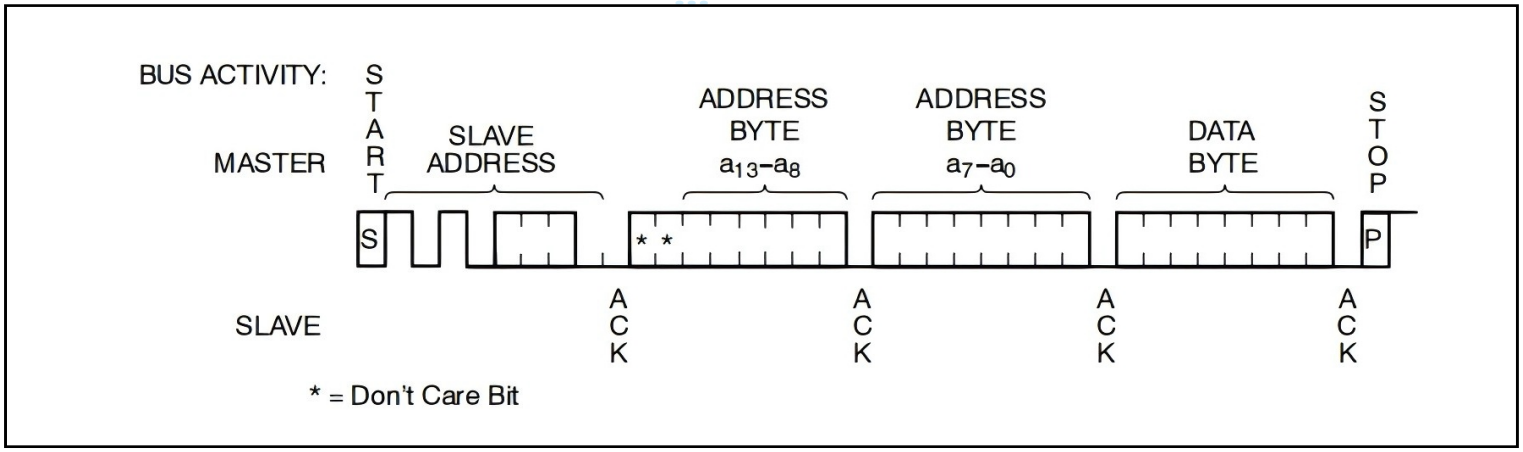


Figure 6. Byte Write Sequence

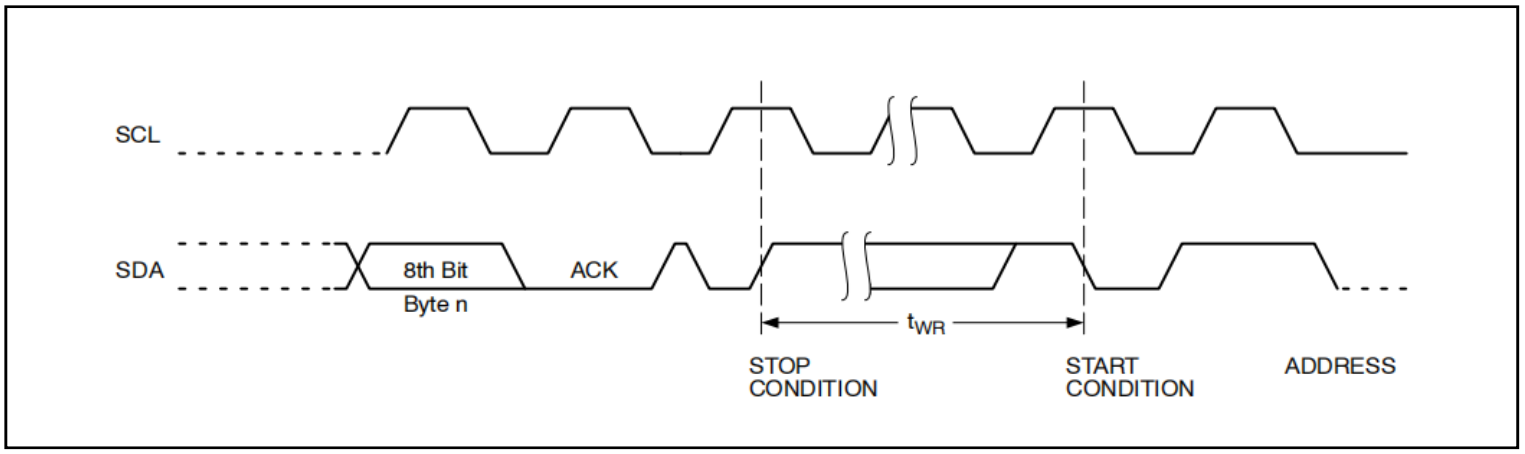


Figure 7. Write Cycle Timing

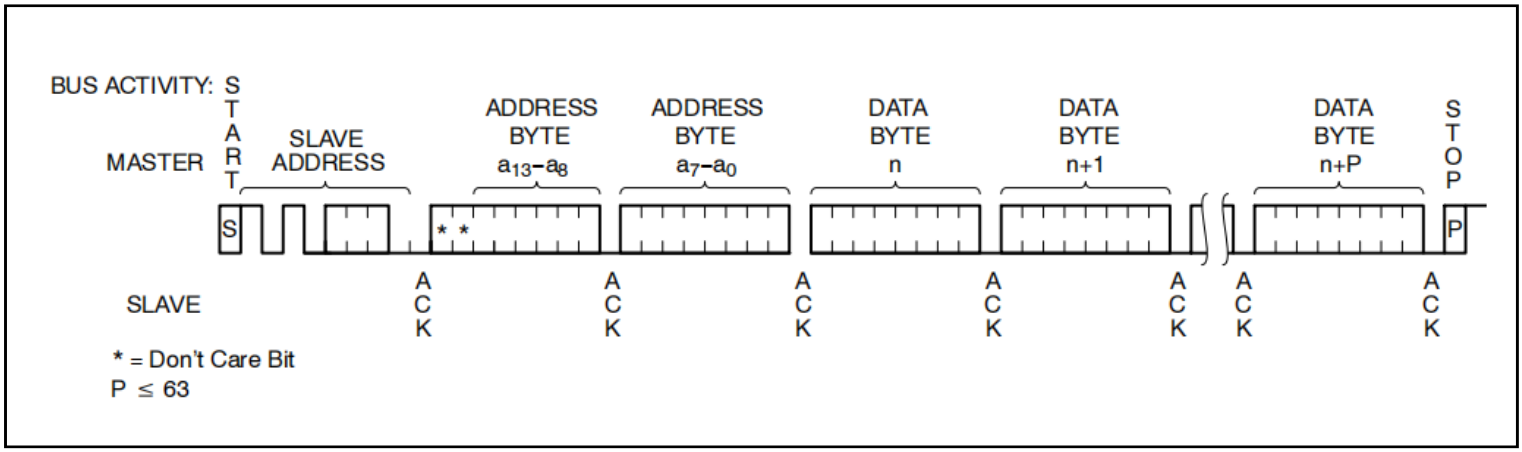


Figure 8. Page Write Sequence

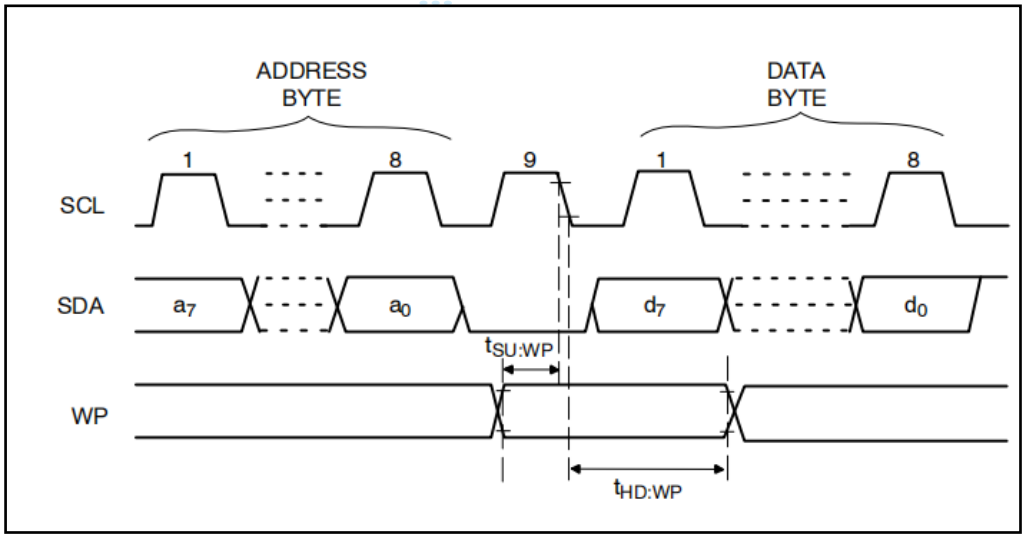


Figure 9. WP Timing

Read Operations

Immediate Read：Upon receiving a Slave address with the R/W bit set to ‘1’, the CAT24C128 will interpret this as a request for data residing at the current byte address in memory. The CAT24C128 will acknowledge the Slave address, will immediately shift out the data residing at the current address,and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 10), the CAT24C128 returns to Standby mode.

Selective Read： To read data residing at a specific location, the internal address counter must first be initialized as described under Byte Write. If rather than following up the two address bytes with data, theMaster instead follows up with an Immediate Read sequence, then the CAT24C128 will use the 14 active address bits to initialize the internal address counter and will shift out data residing at the corresponding location. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 11), the CAT24C128 returns to Standby mode.

Sequential Read：If during a Read session the Master acknowledges the 1st data byte, then the CAT24C128 will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 12). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wrap-around at end of memory (rather than end of page).

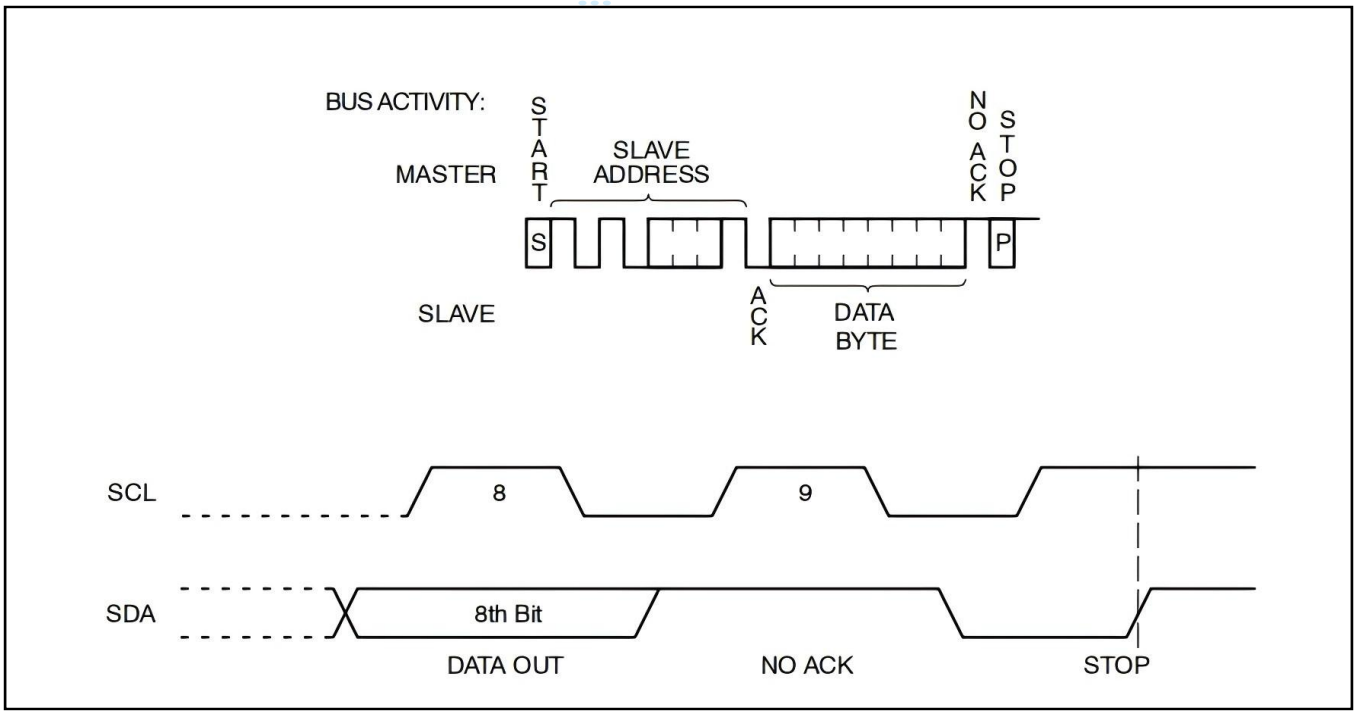


Figure 10. Immediate Read Sequence and Timing

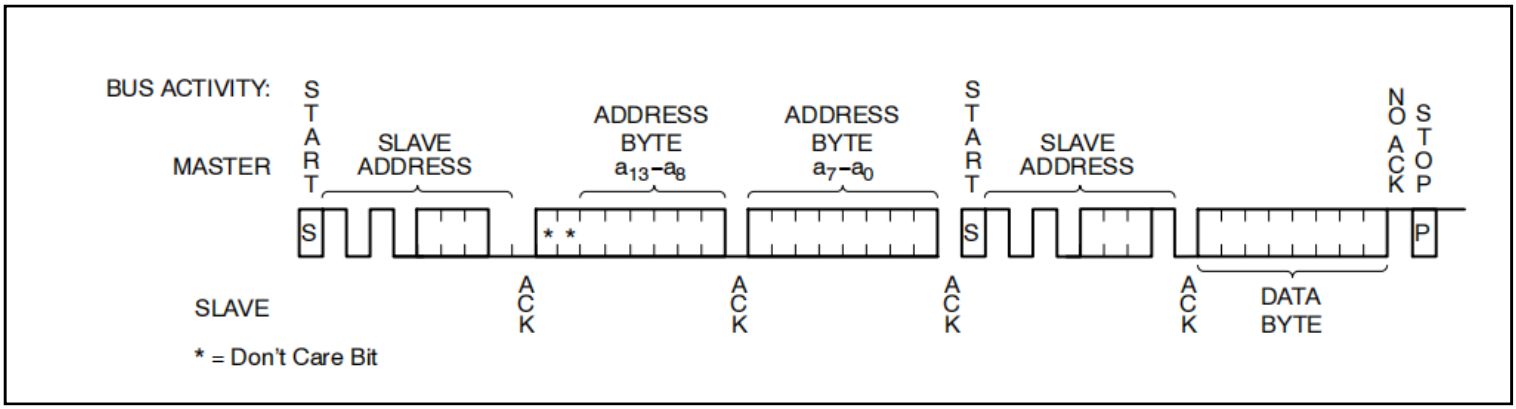


Figure 11. Selective Read Sequence

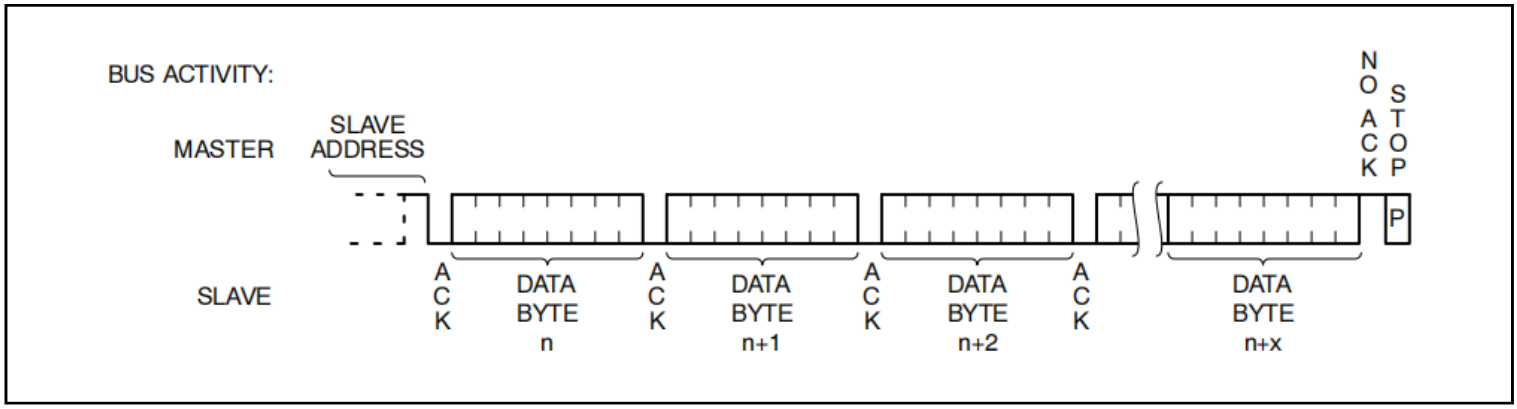


Figure 12. Sequential Read Sequence

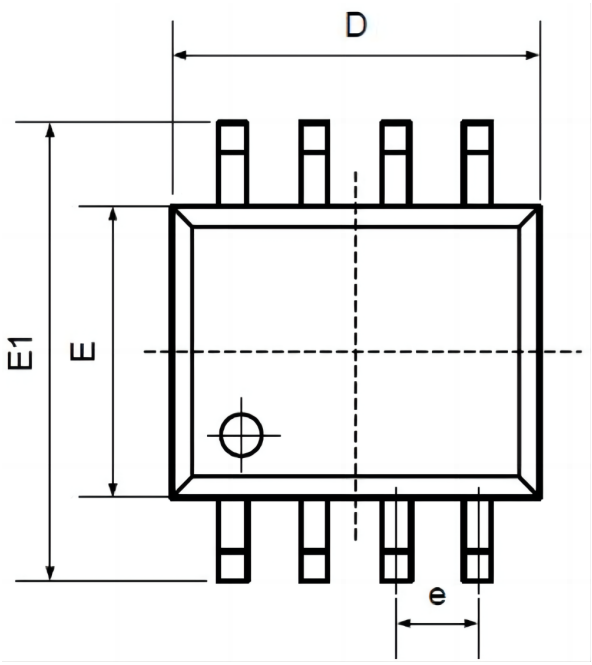
Order information

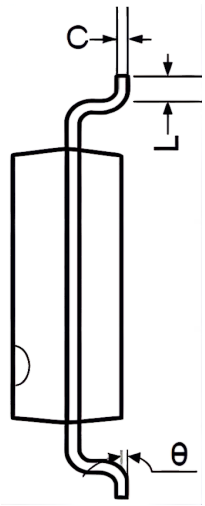
Order Number	Package	Package Quantity	Marking On The park	Temperature
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CAT24C128WI-GT3-TUDI	SOP8	Tape,Reel,4000	24128C	
			24128W	
CAT24C128YI-GT3-TUDI	TSSOP8	Tape,Reel,4000	C28C	

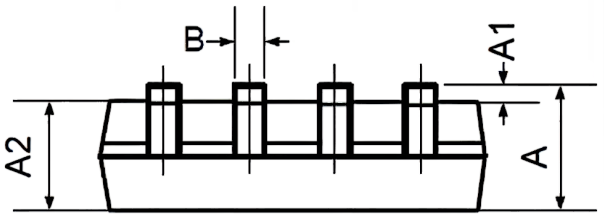
Revision history

	Date	Revision	Page
V1.0	2022/7	New	1-14
V1.1	2024/3	Update model and PDF template	1-19

Package SOP8

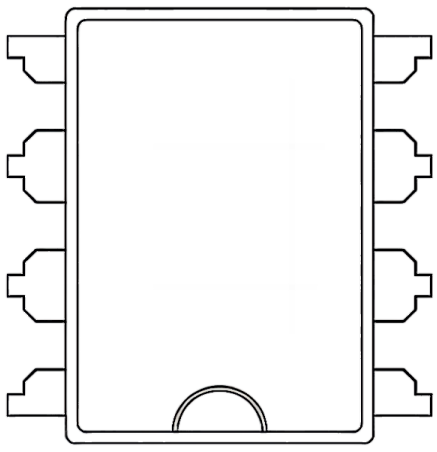


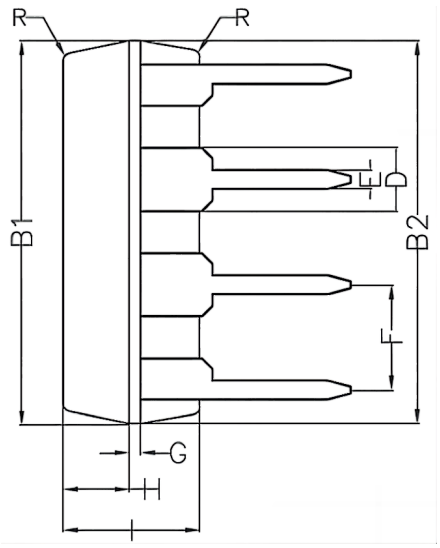


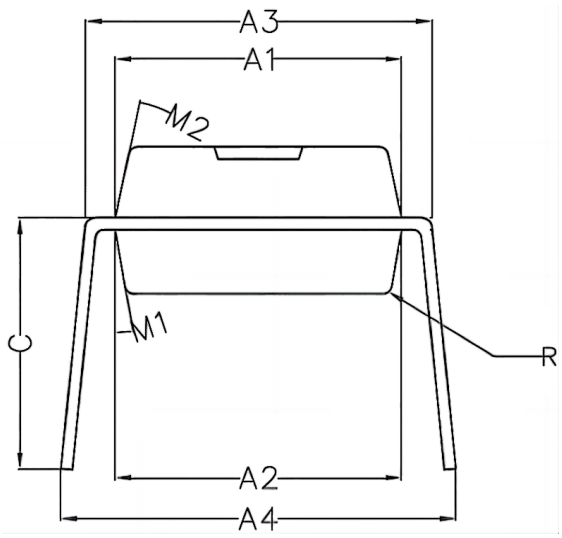


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8

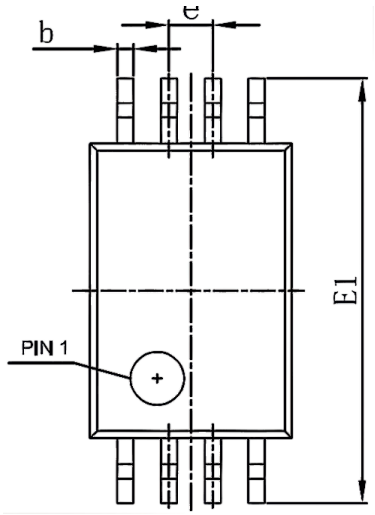


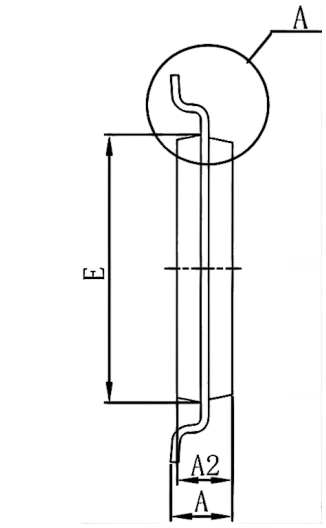


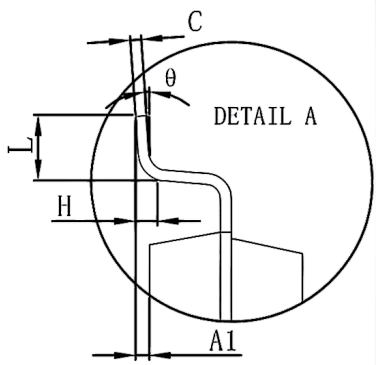


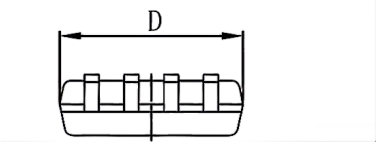
Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

Package TSSOP8









Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
C	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°		1°	

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