

钍地半导体
Tudi Semiconductor

Product Specification

TUDI- AT24C256C

I² C-Compatible (2-Wire) Serial EEPROM 256-Kbit

网址 www.sztdbdt.com

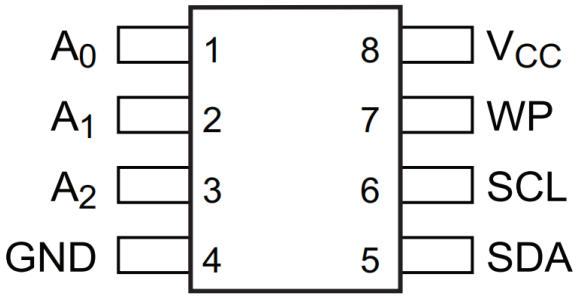
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Low-voltage and standard-voltage operation
- V_{CC} = 1.7V to 5.5V
- Internally organized as 32,768 x 8
- 2-wire serial interface
- Schmitt Trigger, filtered inputs for noise suppression
- Bidirectional data transfer protocol
- 400kHz (1.7V) and 1MHz (2.5V, 2.7V, 5.0V) compatibility
- Write Protect pin for hardware protection
- 64-byte page write mode
- Partial page writes allowed
- Self-timed write cycle (5ms max)
- High reliability
- Endurance: 1,000,000 write cycles
- Data retention: 40 years
- Lead-free/Halogen-free devices available
- Green package options (Pb/Halide-free/RoHS compliant)
- 8-lead JEDEC SOIC and 8-lead TSSOP packages
- Die sale options: wafer form, waffle pack, and bumped wafers



SOP8/TSSOP8

Description

The AT24C256C provides 262,144-bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 32,768 words of eight bits each. The device ' s cascading feature allows up to eight devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.The devices are available in space-saving 8-lead JEDEC SOIC and 8-lead TSSOP packages. In addition, this device operates from 1.7V to 5.5V.

Table 1. Pin Configuration

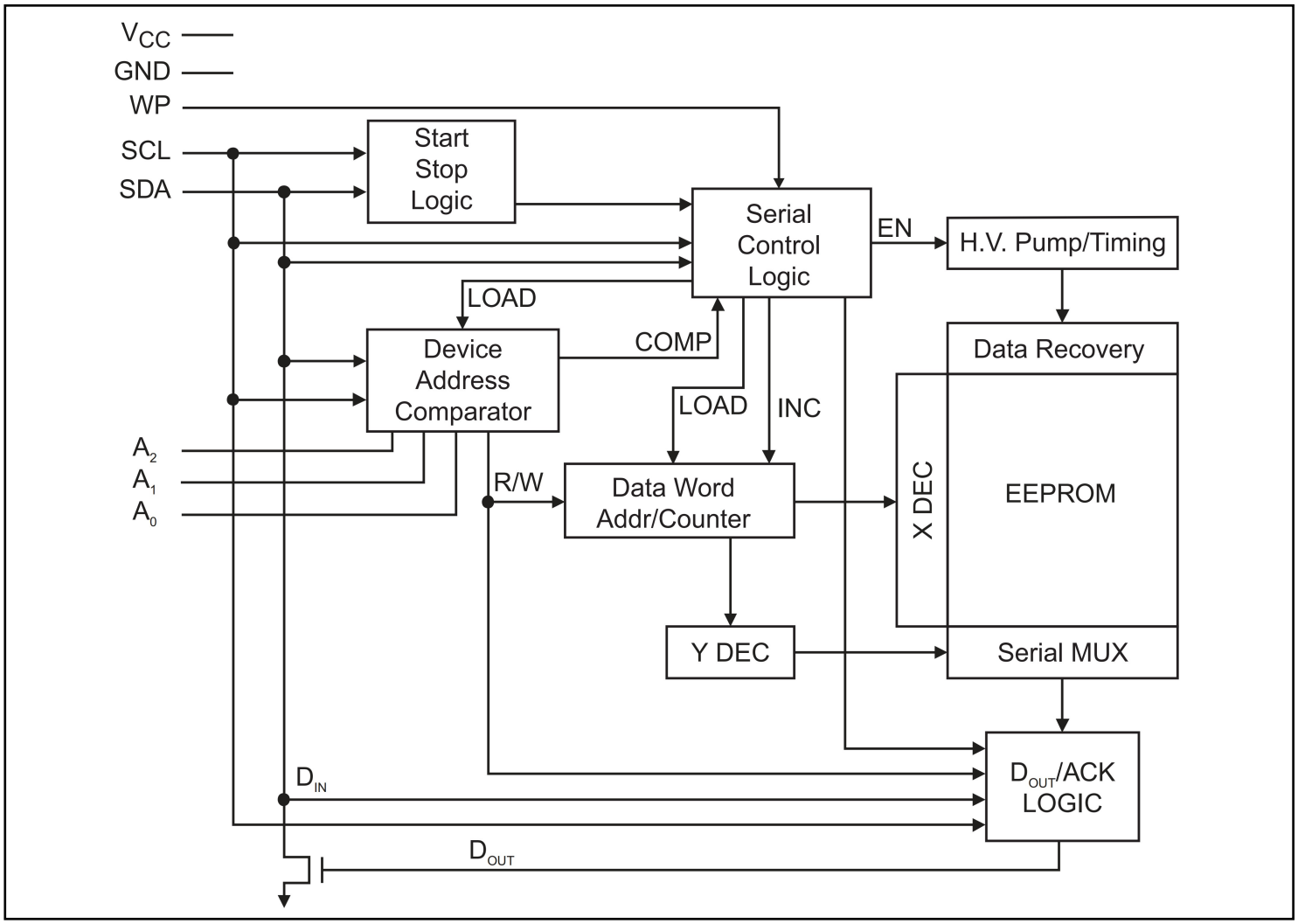
Pin	Function
A_0	Address Input
A_1	Address Input
A_2	Address Input
GND	Ground
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
V_{CC}	Device Power Supply

Absolute Maximum Ratings

Operating Temperature . . . . . .-55°C to +125°C
Storage Temperature . . . . . .-65°C to + 150°C
Voltage on any pin
with respect to ground . . . . . -1.0 V +7.0V
Maximum Operating Voltage. 6.25V
DC Output Current. 5.0mA

Notice: Stresses beyond those listed under “ Absolute Maximum Ratings ” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Descriptions

Serial Clock (SCL): The SCL input is used to positive-edge clock data into each EEPROM device and negative-edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

Device Addresses (A_2, A_1, A_0): The A_2, A_1, and A_0 pins are device address inputs that are hard wired (directly to GND or to V_{CC}) for compatibility with other TUDI AT24C devices. When the pins are hard wired, as many as eight 256K devices may be addressed on a single bus system. (Device addressing is discussed in detail in " Device Addressing "). A device is selected when a corresponding hardware and software match is true. If these pins are left floating, the A_2, A_1, and A_0 pins will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, TUDI recommends always connecting the address pins to a known state. When using a pull-up resistor, TUDI recommends using 10kΩ or less.

Write Protect (WP): The Write Protect input, when connected to GND, allows normal write operations. When WP is connected directly to V_{CC}, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, TUDI recommends always connecting the WP pins to a known state. When using a pull-up resistor, TUDI recommends using 10kΩ or less.

Table 2. Write Protect

WP PinStatus	Part of the Array Protected
	AT24C256C
At V_{cc}	FullArray
At GND	Normal Read/Write Operations

Memory Organization

AT24C256C, 256K Serial EEPROM: The 256K is internally organized as 512 pages of 64-bytes each. Random word addressing requires a 15-bit data word address.

Table 3. Pin Capacitance(1)

Applicable over recommended operating range from: T_A = 25°C, f = 1.0MHz, V_{CC} = 1.7V to 5.5V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance(SDA)	8	pF	$V_{I/O}$ =0V
C_{IN}	Input Capacitance (A_0,A_1,A_2,and SCL)	6	pF	V_{IN}=0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 4. DC Characteristics

Applicable over recommended operating range from: T_{AI} = - 40°C to +85°C, V_{CC} = 1.7V to 5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.7		5.5	V
I_{CC1}	Supply Current	V_{cc}=5.0V	Read at 400kHz		1.0	2.0	mA
I_{CC2}	Supply Current	V_{cc}=5.0V	Write at 400kHz		2.0	3.0	mA
I_{SB1}	Standby Current	V_{cc}=1.7V	VIN=V_{cc} or Vss			1.0	μ A
		V_{cc}=5.0V				6.0	μA
I_{LI}	Input Leakage Current V_{cc}=5.0V	V_{IN}=V_{cc}or V_{SS}			0.10	3.0	μA
I_{LO}	Output Leakage Current V_{cc}=5.0V	V_{OUT}=V_{cc} or V_{SS}			0.05	3.0	μ A
V_{IL}	Input Low Level(1)			-0.6		V_{cc}×0.3	V
V_{IH}	Input High Level(1)			V_{cc}×0.7		V_{cc}+0.5	V
V_{OL1}	Output Low Level	V_{cc}=1.7V	I_{OL}=0.15mA			0.2	V
V_{OL2}	Output Low Level	V_{cc}=3.0V	I_{OL}=2.1mA			0.4	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 5. AC Characteristics (Industrial Temperature)

Applicable over recommended operating range from: T_{AI} = - 40°C to +85°C, V_{CC} = 1.7V to 5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	1.7V		2.5V,5.0V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency,SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1300		400		ns
t_{HIGH}	Clock Pulse Width High	600		400		ns
t_I	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	50	900	50	550	ns
BUF	Time the bus must be free before a new transmission canstart(1)	1300		500		ns
$t_{HD.STA}$	Start Hold Time	600		250		ns
$t_{SU.STA}$	Start Set-up Time	600		250		ns
$t_{HD.DAT}$	Data In Hold Time	0		0		ns
$t_{SU.DAT}$	Data In Set-up Time	100		100		ns
t_R	Inputs Rise Time(1)		300		300	ns
t_F	Inputs Fall Time(1)		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	600		250		ns
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance(1)	25℃,Page Mode,3.3V	1,000,000				Write Cycles

Notes: 1. This parameter is ensured by characterization and is not 100% tested.
2. AC measurement conditions:

- R_L (connects to V_{CC}): 1.3kΩ (2.5V, 5.5V), 10kΩ (1.7V)
- Input pulse voltages: 0.3V_{CC} to 0.7V_{CC}
- Input rise and fall times: ≤ 50ns
- Input and output timing reference voltages: 0.5 x V_{CC}

Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (See Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

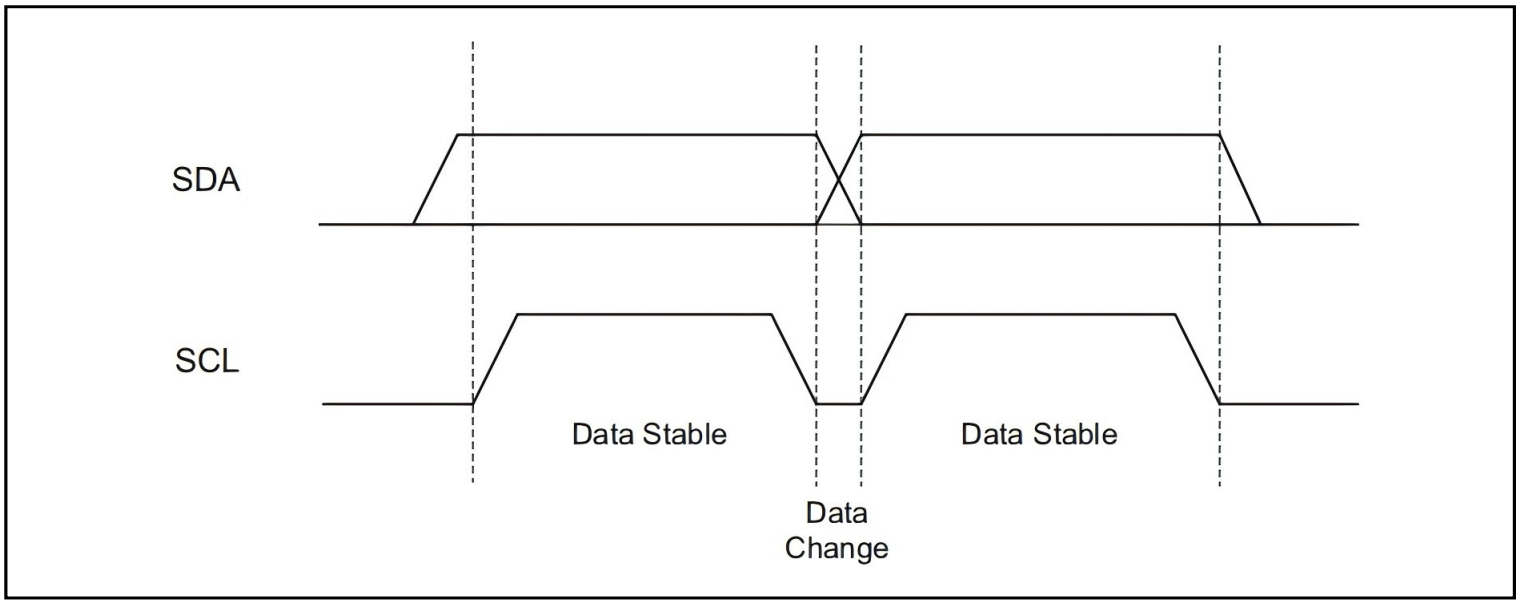


Figure 1. Data Validity

Start Condition: A high-to-low transition of SDA with SCL high is a start condition that must precede any other command (See Figure 2).

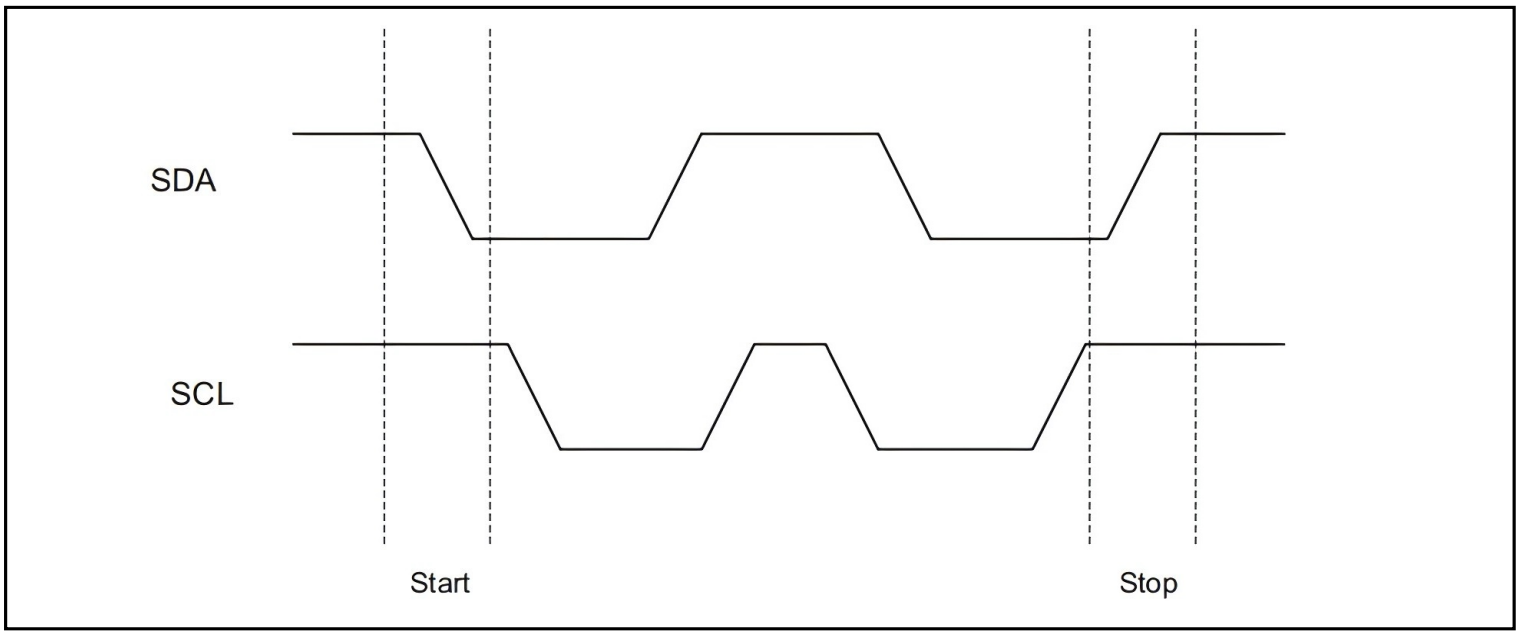


Figure 2. Start and Stop Definition

Stop Condition: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (See Figure 2).

Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word. Standby Mode: AT24C256C features a low-power standby mode that is enabled upon power-up and after the receipt of the stop bit and the completion of any internal operations.

Software Reset: After an interruption in protocol, power loss or system reset, any 2-wire part can be protocol reset by following these steps:

1. Create a Start bit condition
2. Clock nine cycles
3. Create another Start bit followed by stop bit condition as shown below.

The device is ready for next communication after above steps has been completed.

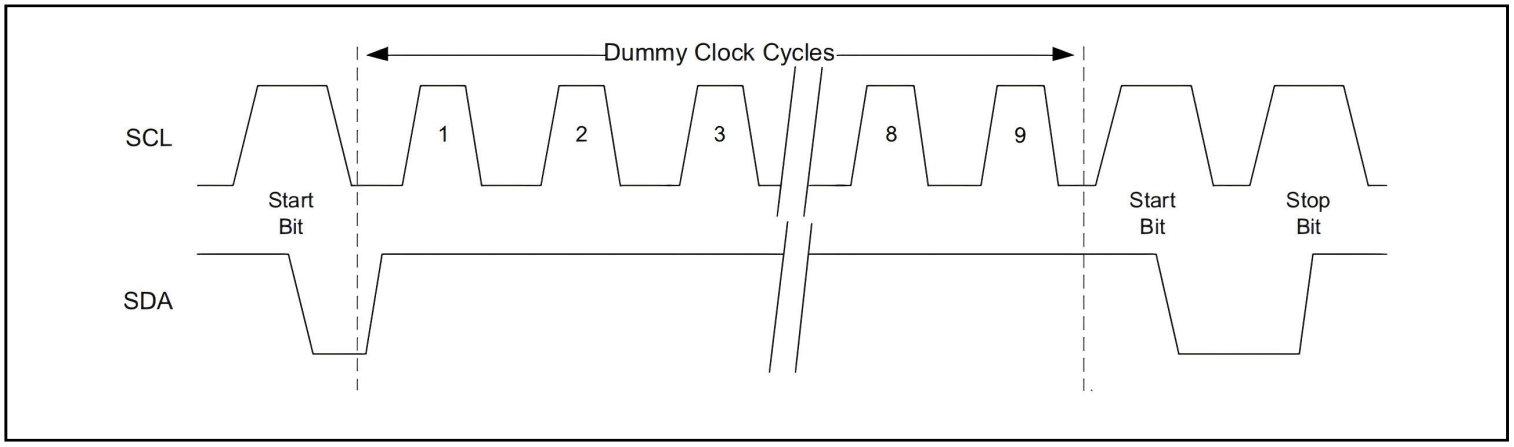


Figure 3. Software Reset

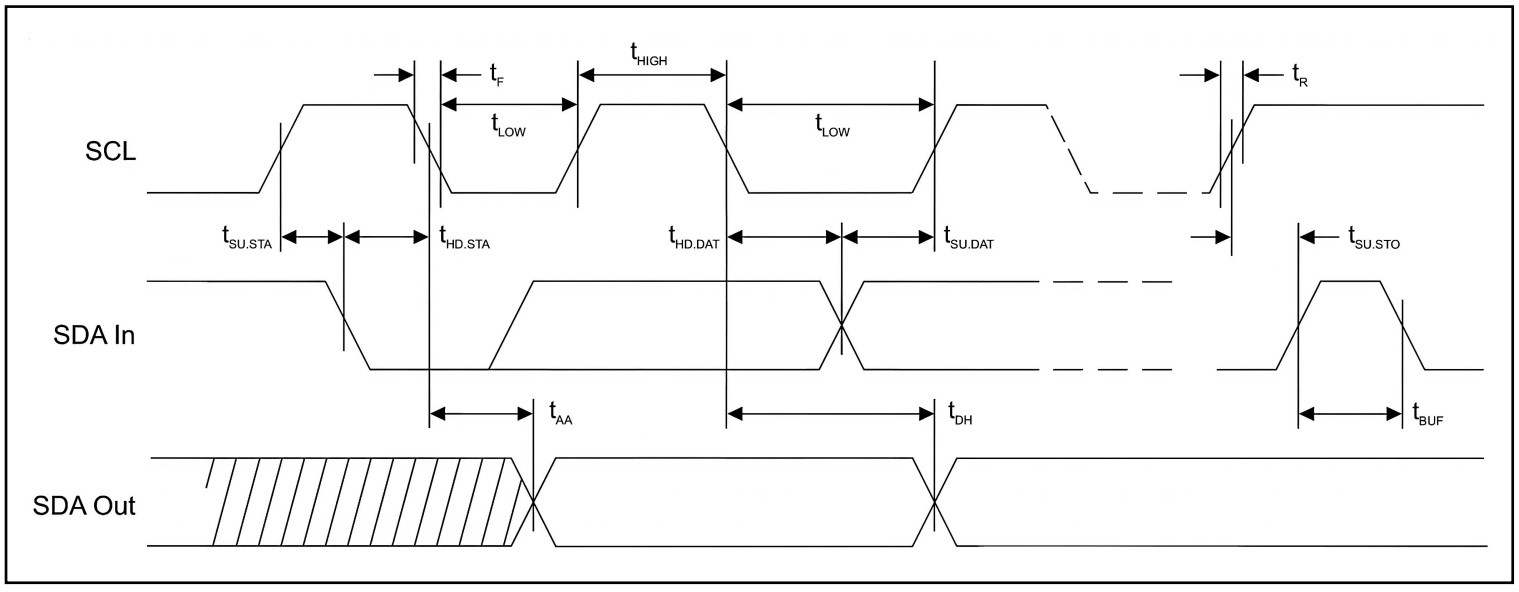


Figure 4. Bus Timing

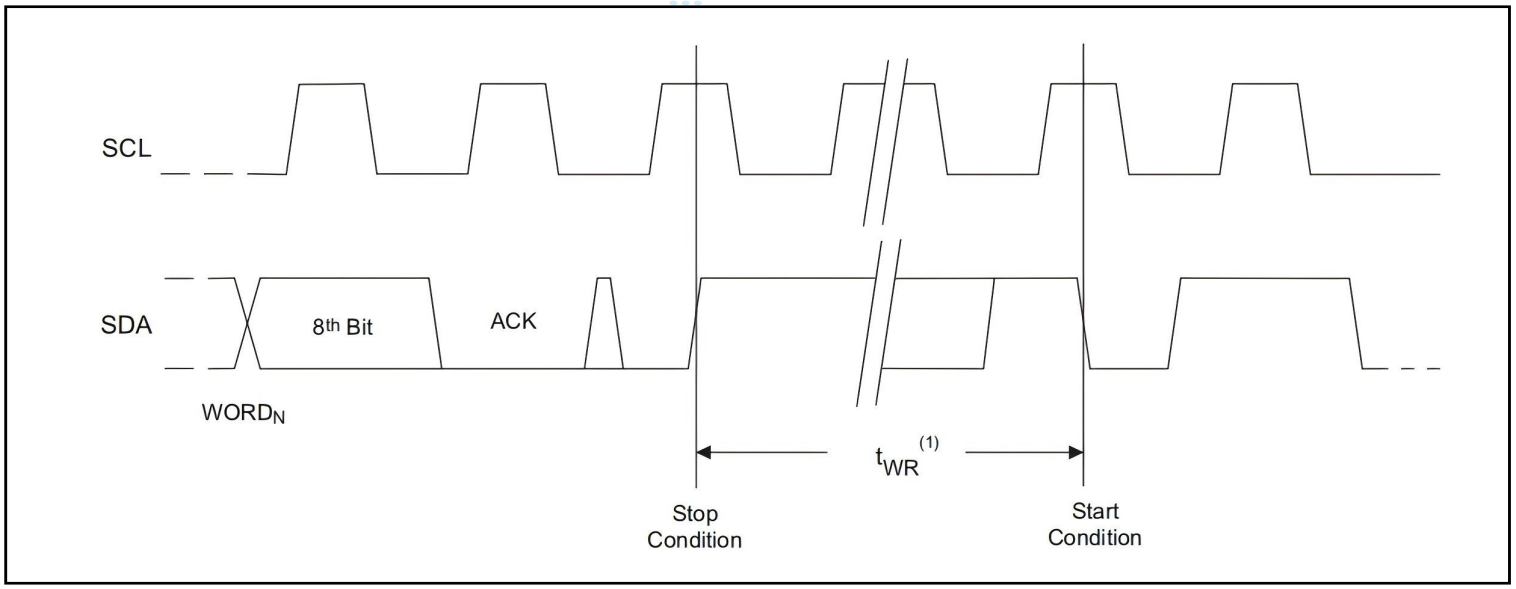


Figure 5. Write Cycle Timing

Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

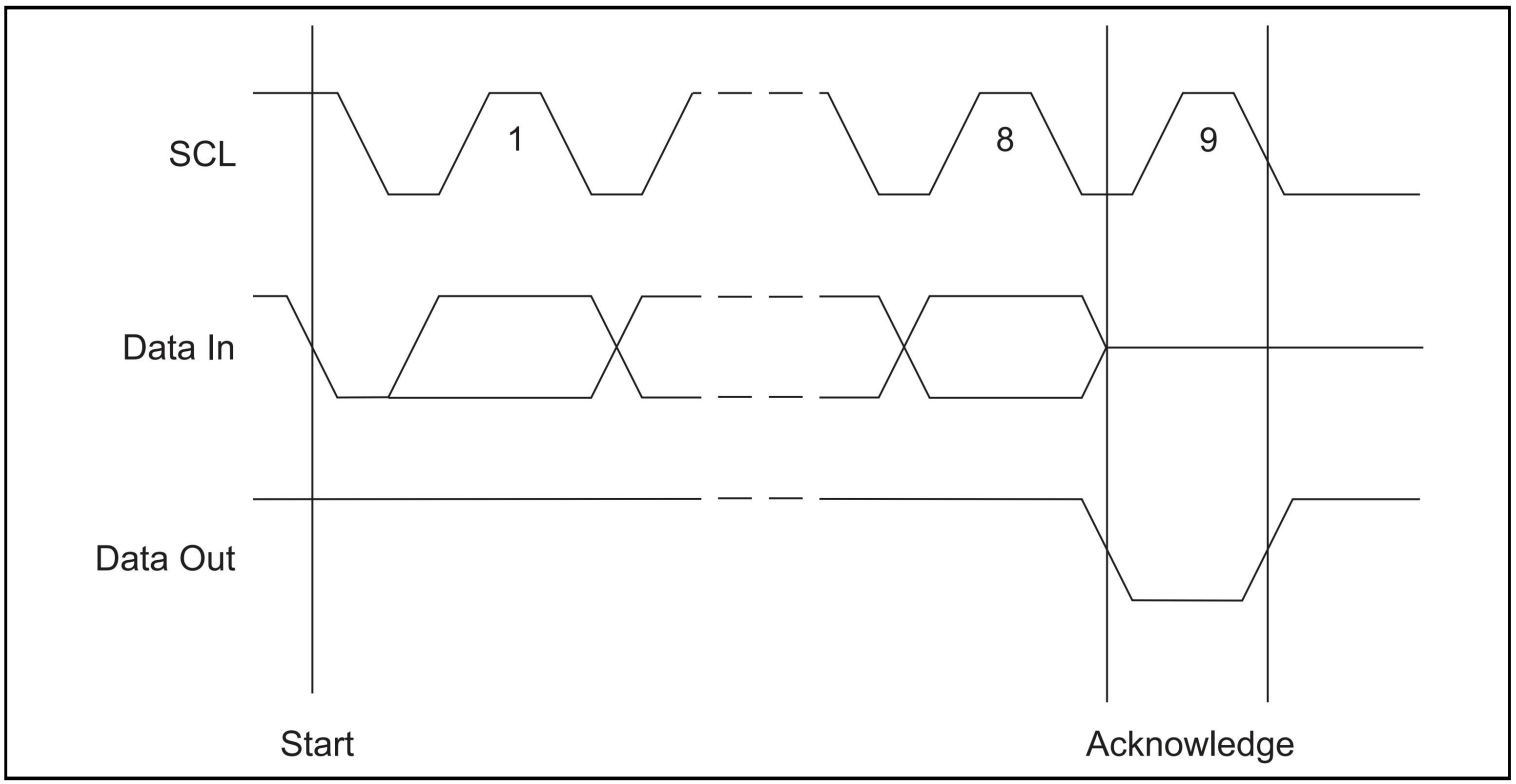


Figure 6. Output Acknowledge

Device Addressing

The 256K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (Figure 7). The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all 2-wire EEPROM devices.

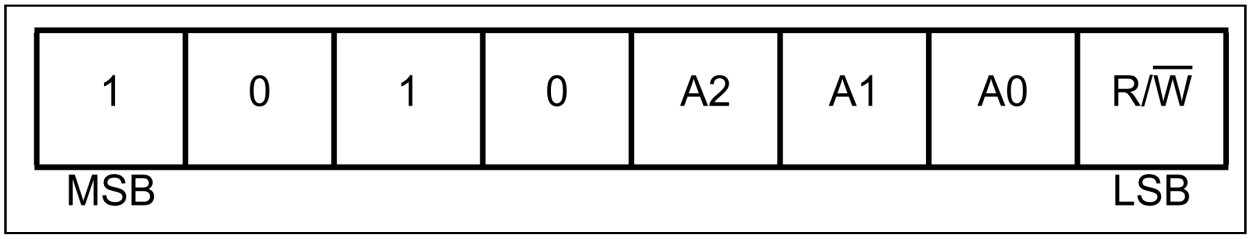


Figure 7. Device Addressing

The next three bits are the A2, A1, and A0 device address bits to allow as many as eight devices on the same bus. These bits must compare to their corresponding hard wired input pins. The A_2, A_1, and A_0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.
The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high, and a write operation is initiated if this bit is low.
Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made , the device will return to a standby state.

Data Security: AT24C256C has a hardware data protection scheme that allows the user to write protect the whole memory when the WP pin is at V_{CC}.

Write Operations

Byte Write: A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero, and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero. The addressing device, such as a microcontroller, must then terminate the write sequence with a stop condition. At this time, the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (See Figure 7).

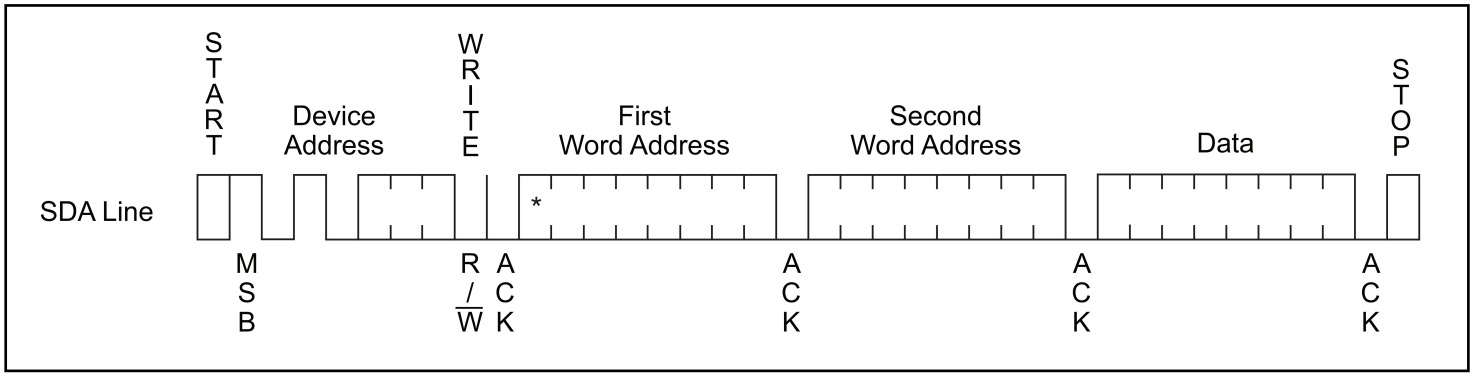


Figure 8. Byte Write

Note: * = Don ’ t care bit

Page Write: The 256K EEPROM is capable of 64-byte page writes.
A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 63 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (See Figure 9).

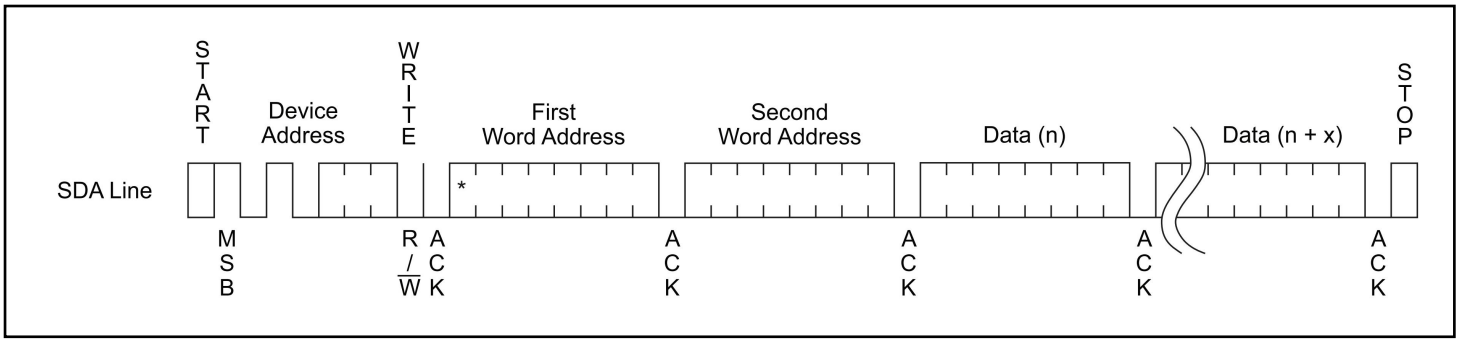


Figure 9. Page Write

Note: * = Don ’ t care bit

The data word address lower six bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data words are transmitted to the EEPROM, the data word address will roll-over and the previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

Acknowledge Polling: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations:

- Current Address Read
- Random Address Read
- Sequential Read

Current Address Read: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page, to the first byte of the first page.

Once the device address with the read/write select bit set to one is clocked in andacknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (See Figure10).

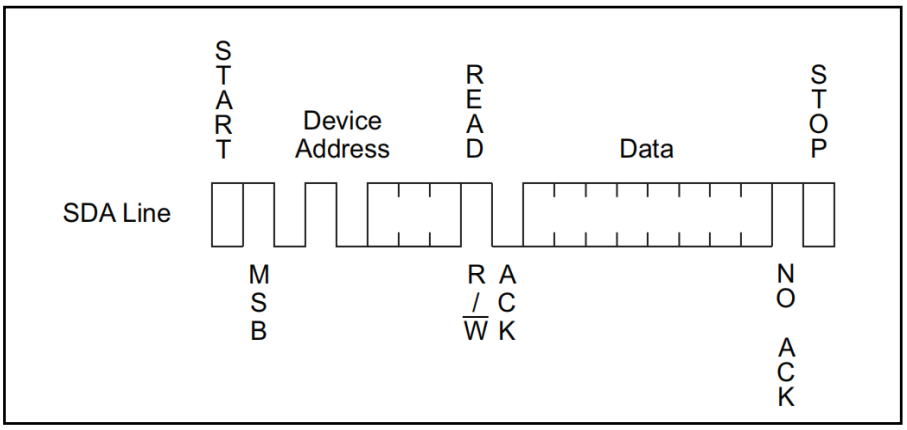


Figure 10. Current Address Read

Random Read: A Random Read requires a dummy byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition. (See Figure 11).

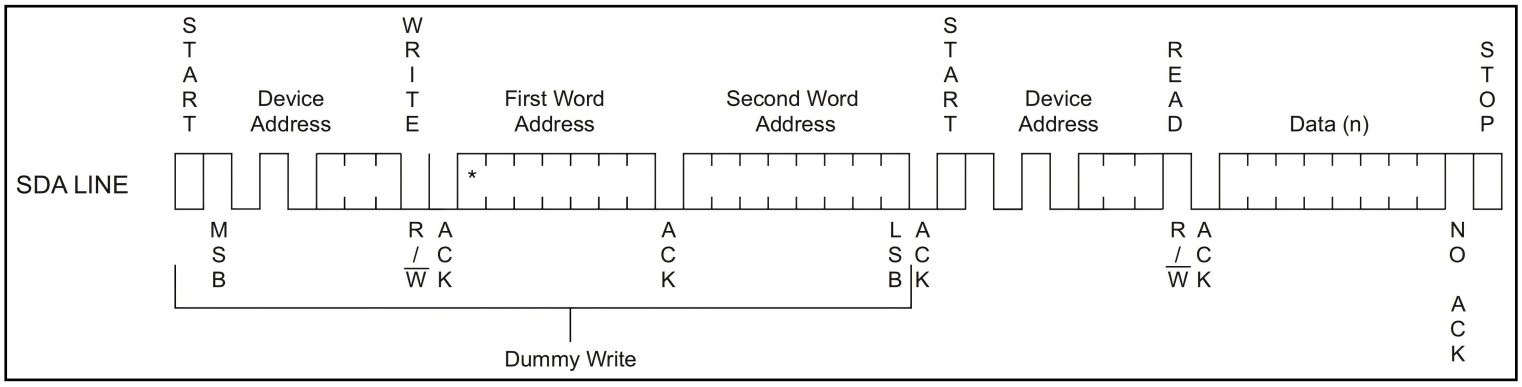


Figure 11. Random Read

Note: * = Don ’ t care bit

Sequential Read: Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over, and the sequential read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (See Figure 12).

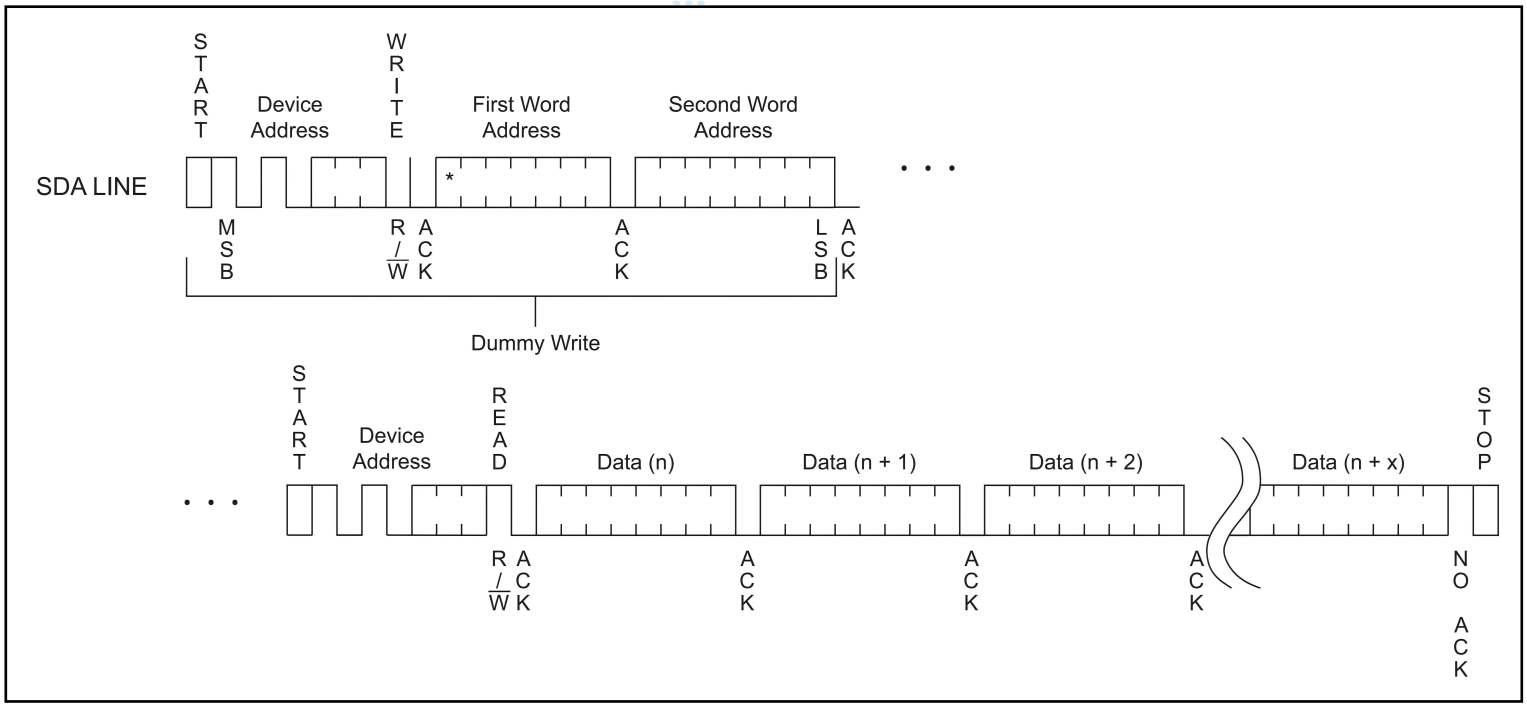


Figure 12. Sequential Read

Note: * = Don ’ t care bit

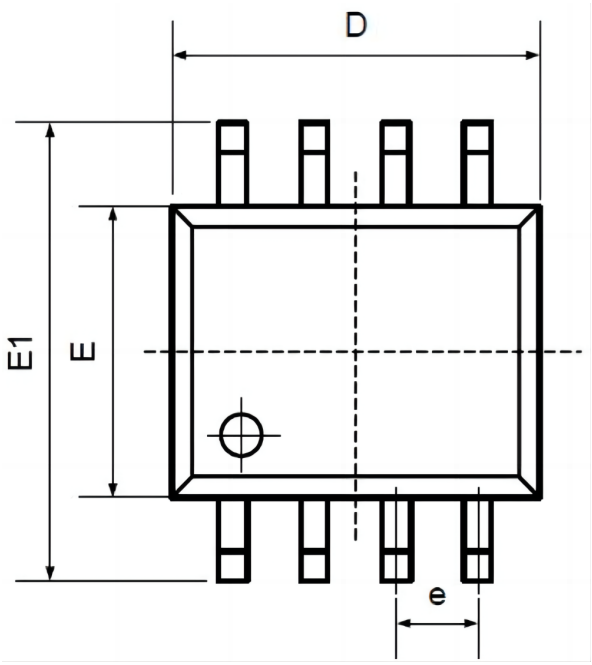
Order information

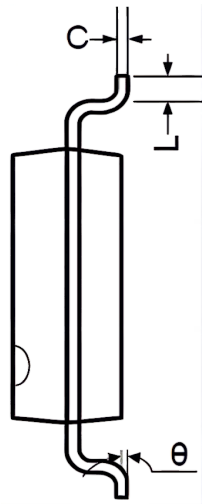
Order Number	Package	Package Quantity	Marking On The park	Temperature
AT24C256C-SSHL-T-TUDI	SOP8	Tape,Reel,4000	2EB	-40°C to 85°C
			2ECL	
AT24C256C-XHL-T-TUDI	TSSOP8	Tape,Reel,4000	2ECL	
AT24C256C-XHM-T-TUDI	TSSOP8	Tape,Reel,4000	24C256C	

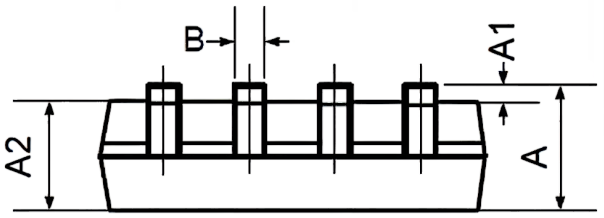
Revision history

	Date	Revision	Page
V1.0	2022/9	New	1-15
V1.1	2025/6	Update model and PDF template	1-19

Package SOP8

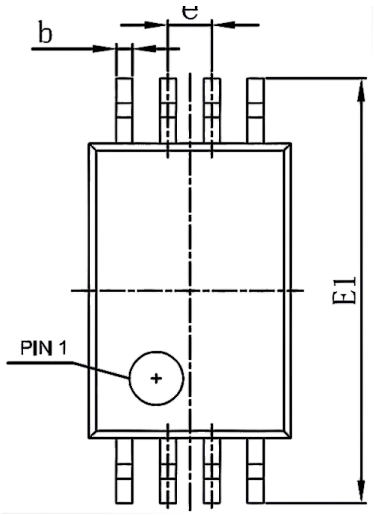


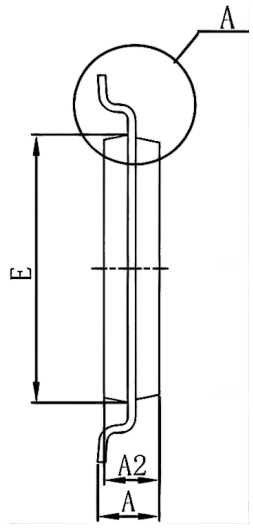


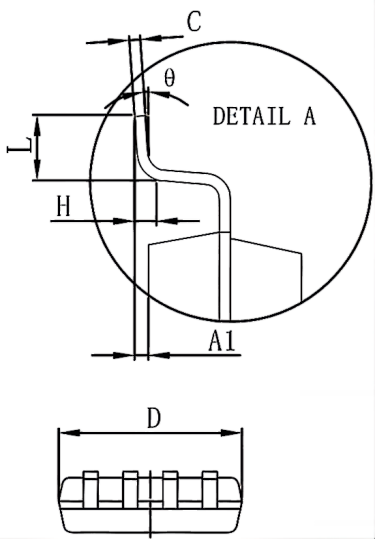


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package TSSOP8







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
C	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°		1°	

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