

钍地半导体
Tudi Semiconductor

Product Specification

TUDI-CAT24C256

256 kb I^2C CMOS Serial EEPROM

网址 www.sztdbdt.com

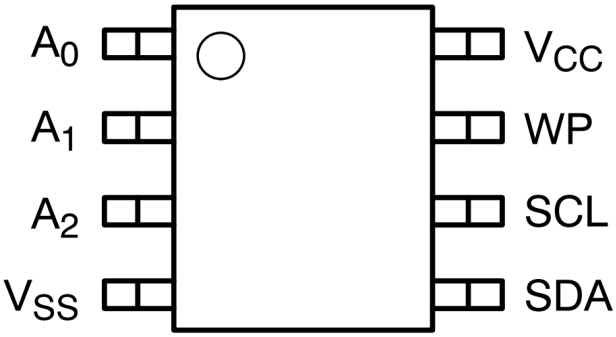
用芯智造·卓越品质

semiconductor device manufacturer

- Design
- research and development
- production
- and sales

Features

- Supports Standard, Fast and Fast-Plus I^2C Protocol
- 1.8 V to 5.5 V Supply Voltage Range
- 64Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I^2C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- PDIP, SOIC, TSSOP Packages
- This Device is PbFree, Halogen Free/BFR Free, and RoHS Compliant



SOP8/DIP8/TSSOP8

Description

The CAT24C256 is a 256 kb Serial CMOS EEPROM, internally organized as 32,768 words of 8 bits each.
It features a 64-byte page write buffer and supports the Standard (100 kHz), Fast (400 kHz) and Fast-Plus (1 MHz) I2C protocol. Write operations can be inhibited by taking the WP pin High (this protects the entire memory).
External address pins make it possible to address up to eight CAT24C256 devices on the same bus.
On-Chip ECC (Error Correction Code) makes the device suitable for high reliability applications.

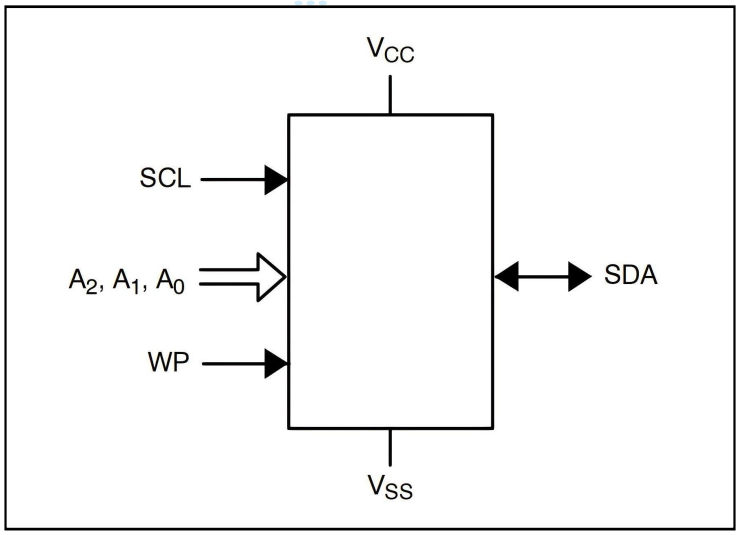


Figure 1. Functional Symbol

* Available for New Product (Rev. E)

Table 1.PIN FUNCTION

Pin Namet	Function
A_0,A_1,A_2	Device Address
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V_{CC}	Power Supply
V_{SS}	Ground

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	65 to+150	℃
Voltage on any Pin with Respect to Ground(Note 1)	-0.5 to+6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. The DC input voltage on any pin should not be lower than -0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 3. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END}(Notes 3,4)	Endurance	1,000,000	Program/Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
3. Page Mode, V_{CC} = 5 V, 25°C.
4. The new product revision (E) uses ECC (Error Correction Code) logic with 6 ECC bits to correct one bit error in 4 data bytes. Therefore, when a single byte has to be written, 4 bytes (including the ECC bits) are re-programmed. It is recommended to write by multiple of 4 bytes in order to benefit from the maximum number of write cycles.

Table 4. D.C. OPERATING CHARACTERISTICS-Mature Product (Rev D)

(V_{CC} = 2.5 V to 5.5 V, T_A =-40°C to +125°C, and V_{CC} = 1.8 V to 5.5 V, T_A =-40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CCR}	Read Current	Read,f_{SCL}=400 kHz			1	mA
I_{CC}	Write Current	Write,f_{SCL}=400 kHz			3	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}	T_A=-40℃ to+85℃		1	μA
			T_A=-40℃ to+125℃		2	
I_L	I/O Pin Leakage	Pin at GND or V_{CC}	T_A=-40℃ to+85℃		1	μA
			T_A=-40℃ to+125℃		2	
V_{IL}	Input Low Voltage			-0.5	V_{CC}×0.3	V
V_{IH}	Input High Voltage			V_{CC}×0.7	V_{CC}+0.5	V
V_{OL1}	Output Low Voltage	V_{CC}≥2.5 V,I_{OL}=3.0 mA			0.4	V
V_{OL2}	Output Low Voltage	V_{CC}<2.5 V,I_{OL}=1.0 mA			0.2	V

Table 5. PIN IMPEDANCE CHARACTERISTICS-Mature Product (Rev D)

(V_{CC} = 2.5 V to 5.5 V, T_A = 40°C to +125°C, and V_{CC} = 1.8 V to 5.5 V, T_A = 40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
C_{IN}(Note 5)	SDA I/O Pin Capacitance	V_{IN}=0V	8	pF
C_{IN}(Note 5)	Input Capacitance (other pins)	V_{IN}=0V	6	pF
I_{WP}(Note 6)	WP Input Current	$V_{IN}<V_{IH}$,V_{CC}=5.5V	130	μA
		$V_{IN}<V_{IH}$,V_{CC}=3.3 V	120	
		$V_{IN}<V_{IH}$,V_{CC}=1.8V	80	
		$V_{IN}>V_{IH}$	1	

5. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AECQ100 and JEDEC test methods.
6. When not driven, the WP pin is pulled down to GND internally. For improved noise immunity, the internal pulldown is relatively strong;therefore the external driver must be able to supply the pulldown current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pulldown reverts to a weak current source. The variable WP input impedance is available only for Die Rev. C and higher.

Table 6. D.C. OPERATING CHARACTERISTICS New Product (Rev E) (Note7)

(V_{CC} = 1.8 V to 5.5 V, T_A = 40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = 40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CCR}	Read Current	Read,fscL=400 kHz/1 MHz			1	mA
I_{CCW}	Write Current				3	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}	T_A=-40℃ to +85℃		2	μA
			T_A=-40℃ to+125℃		5	
I_L	I/O Pin Leakage	Pin at GND or V_{CC}	T_A=-40℃ to+85℃		1	μA
			T_A=-40℃ to+125℃		2	
V_{IL1}	Input Low Voltage	2.5V≤V_{CC}≤5.5V		-0.5	0.3 V_{CC}	V
V_{IL2}	Input Low Voltage	1.8V≤V_{CC}<2.5 V		-0.5	0.25 V_{CC}	V
V_{IH1}	Input High Voltage	2.5V≤V_{CC}≤5.5V		0.7 V_{CC}	V_{CC}+0.5	V
V_{IH2}	Input High Voltage	1.8V≤V_{CC}<2.5V		0.75 V_{CC}	V_{CC}+0.5	V
V_{OL1}	Output Low Voltage	V_{CC}≥2.5 V,I_{OL}=3.0 mA			0.4	V
V_{OL2}	Output Low Voltage	V_{CC}<2.5 V,I_{OL}=1.0 mA			0.2	V

Table 7. PIN IMPEDANCE CHARACTERISTICS New Product (Rev E) (Note 7)

(V_{CC} = 1.8 V to 5.5 V, T_A = 40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = 40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
C_{IN}(Note 8)	SDA I/O Pin Capacitance	V_{IN}=0V	8	pF
C_{IN}(Note 8)	Input Capacitance (other pins)	V_{IN}=0V	6	pF
$I_{WP,IA}$(Note 9)	WP Input Current,Address Input Current(A_0,A_1,A_2)	$V_{IN}<V_{IH}$,V_{CC}=5.5V	75	μA
		$V_{IN}<V_{IH}$,V_{CC}=3.3V	50	
		$V_{IN}<V_{IH}$,V_{CC}=1.8V	25	
		$V_{IN}>V_{IH}$	2	

7. The new product Rev E is identified by letter “E” or a dedicated marking code on top of the package.
8. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AECQ100 and JEDEC test methods.
9. When not driven, the WP, A_0, A_1, A_2 pins are pulled down to GND internally. For improved noise immunity, the internal pulldown is relatively strong; therefore the external driver must be able to supply the pulldown current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pulldown reverts to a weak current source.

Table 8. A.C. CHARACTERISTICS Mature Product (Rev D) (Notes 10, 11)

(V_{CC} = 2.5 V to 5.5 V, T_A =-40°C to +125°C, and V_{CC} = 1.8 V to 5.5 V, T_A =-40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Standard		Fast		Fast-Plus Vcc=2.5V-5.5V TA=-40°°C to +85°C		Units
		Min	Max	Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400		1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		0.25		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		0.55		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		0.25		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		0.25		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		50		ns

Symbol	Parameter	Standard		Fast		Fast-Plus Vcc=2.5V-5.5V TA=-40°℃ to +85℃		Units
		Min	Max	Min	Max	Min	Max	
t_R(Note 12)	SDA and SCL Rise Time		1,000		300		100	ns
t_F(Note 12)	SDA and SCL Fall Time		300		300		100	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		0.25		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9		0.50	μs
t_{DH}	Data Out Hold Time	100		100		50		ns
Ti(Note 12)	Noise Pulse Filtered at SCLand SDA Inputs		100		100		100	ns
$t_{SU:WP}$	WP Setup Time	0		0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		1		μs
t_{WR}	Write Cycle Time		5		5		5	ms
t_{PU} (Notes 12,13)	Power-up to Ready Mode		1		1	0.1	1	ms

10.The product Rev D is identified by letter “ D ” or a dedicated marking code on top of the package.
11. Test conditions according to “ A.C. Test Conditions ” table.
12.Tested initially and after a design or process change that affects this parameter.
13.tPU is the delay between the time VCC is stable and the device is ready to accept commands.
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 9. A.C. TEST CONDITIONS

Input Levels	Input Rise and Fall Times	Input Reference Levels	Output Reference Levels	Output Load
0.2×Vcc to 0.8×Vcc	≤50 ns	0.3×Vcc,0.7×Vcc	0.5×Vcc	Current Source:I_L=3mA (Vcc≥2.5V);I_L=1mA(Vcc<2.5V);C_L=100 pF

Table 10. A.C. CHARACTERISTICS-New Product (Rev E) (Notes 14, 15)

(V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = -40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Standard Vcc=1.8V-5.5V		Fast Vcc=1.8V-5.5V		Fast-Plus Vcc=2.5V-5.5V TA=-40℃ to +85℃		Units
		Min	Max	Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400		1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		0.25		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		0.45		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		0.40		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		0.25		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		50		ns
t_R(Note 16)	SDA and SCL Rise Time		1,000		300		100	ns
t_F(Note 16)	SDA and SCL Fall Time		300		300		100	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		0.25		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9		0.40	μs
t_{DH}	Data Out Hold Time	50		50		50		ns
Ti(Note 16)	Noise Pulse Filtered at SCLand SDA Inputs		50		50		50	ns
$t_{SU:WP}$	WP Setup Time	0		0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		1		μs
t_{WR}	Write Cycle Time		5		5		5	ms
t_{PU} (Notes 16,17)	Power-up to Ready Mode		1		1	0.1	1	ms

14.Test conditions according to “A.C. Test Conditions” table.
15.The New product Rev E is identified by letter “E” or a dedicated marking code on top of the package.
16.Tested initially and after a design or process change that affects this parameter.
17.t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.2

Power-On Reset (POR)：The CAT24C256 Die Rev. C incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.
The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi-directional POR behavior protects the device against brown-out failure, following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock signal generated by the Master.
SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.
A_0, A_1 and A_2: The Address pins accept the device address. These pins have on-chip pull-down res istors.
WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. This pin has an on -chip pull-down resistor

Functional Description: The CAT24C256 supports the Inter-Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24C256 acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 8 devices may be connected to the bus as determined by the device address inputs A_0,A_1 and A_2.

I^2C Bus Protocol: The I^2C bus consists of two ‘ wires ’, SCL and SDA. The two wires are connected to the VCC supply via pull-up resistors. Master and Slave devices connect to the 2-wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to ‘ transmit ’ a ‘ 0 ’ and releases it to ‘ transmit ’ a ‘ 1 ’.
Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).
During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 2).

START: The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a ‘ wake-up ’ call to all receivers. Absent a START, a Slave will not respond to commands.

STOP: The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP starts the internal Write cycle (when following a Write command) or sends the Slave into standby mode (when following a Read command)

Device Addressing: The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations (Figure 3). The next 3 bits, A_2, A_1 and A_0, select one of 8 possible Slave devices. The last bit, R/W, specifies whether a Read (1) or Write (0) operation is to be performed.

Acknowledge: After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 4). The Slave will also acknowledge the byteaddress and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9th clock cycle. If the Master acknowledges the data, then the Slave continues transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by sending a STOP to the Slave. Bus timing is illustrated in Figure 5.

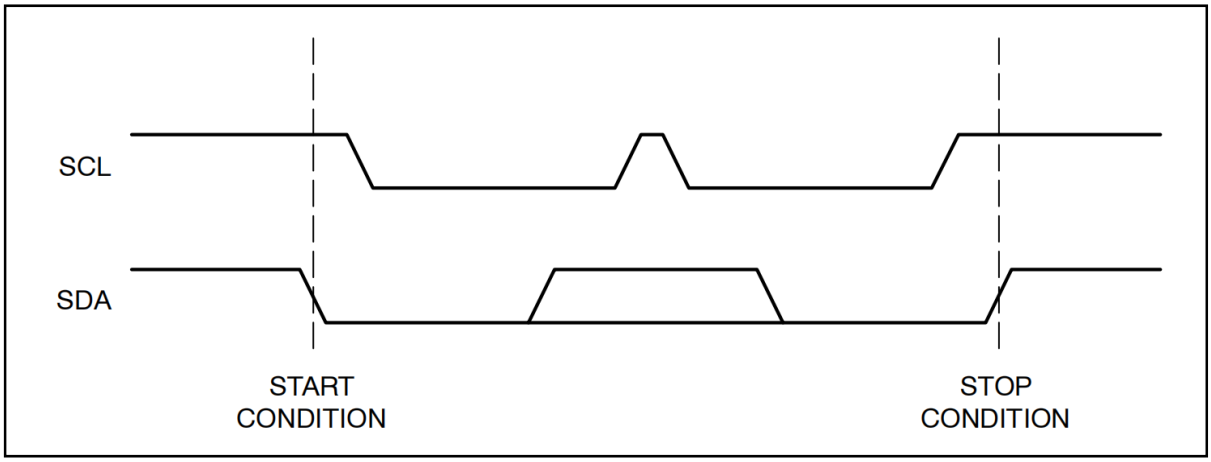


Figure 2. Start/Stop Timing

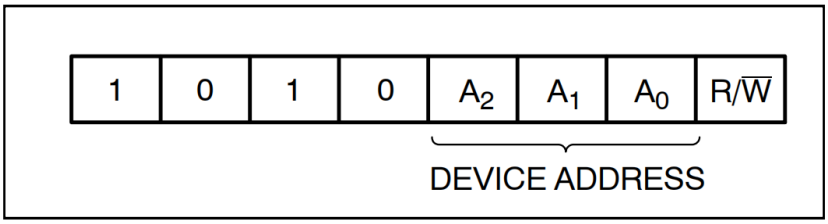


Figure 3. Slave Address Bits

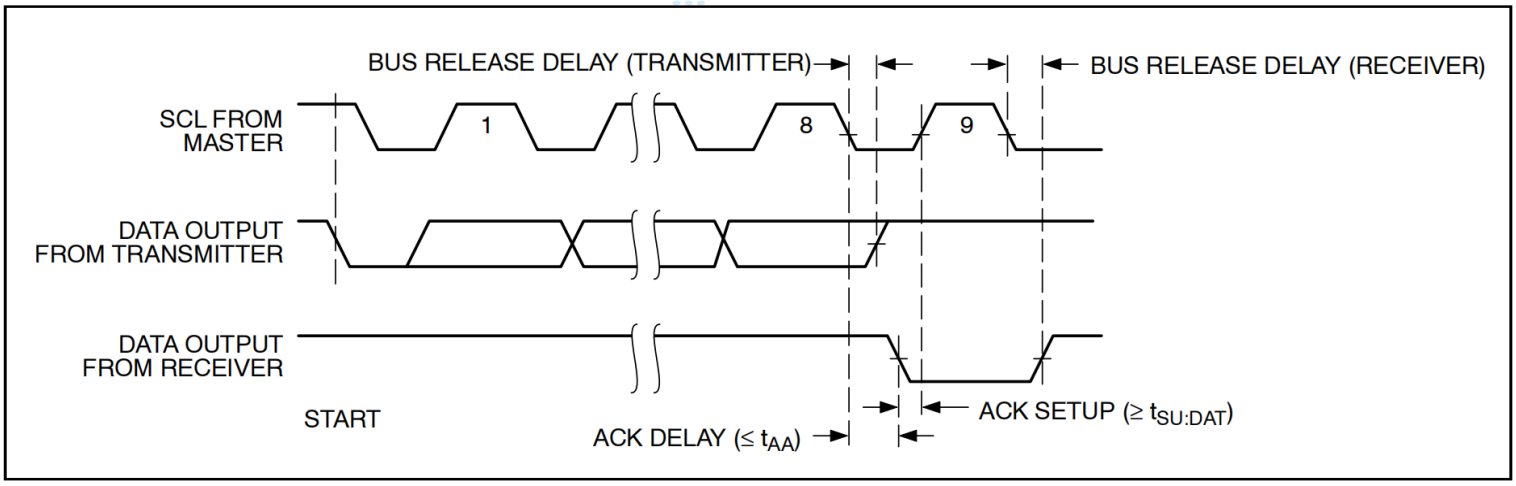


Figure 4. Acknowledge Timing

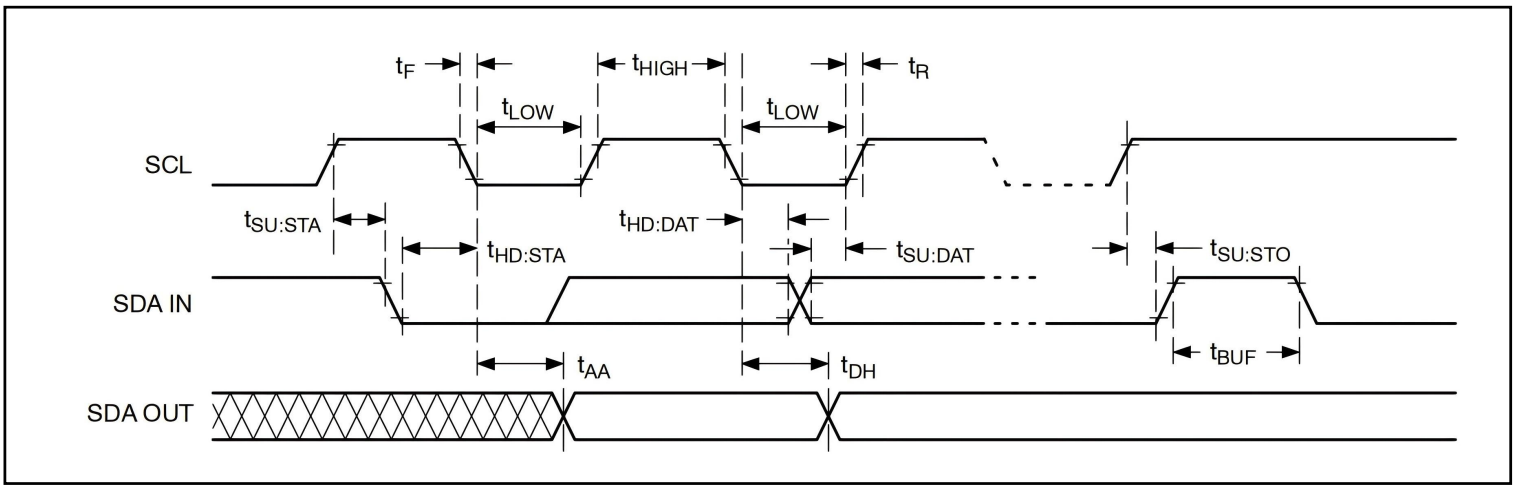


Figure 5. Bus Timing

WRITE OPERATIONS

Byte Write: In Byte Write mode the Master sends a START, followed by Slave address, two byte address and data to be written (Figure 6). The Slave acknowledges all 4 bytes, and the Master then follows up with a STOP, which in turn starts the internal Write operation (Figure 7). During internal Write, the Slave will not acknowledge any Read or Write request from the Master.

Page Write: The CAT24C256 contains 32,768 bytes of data, arranged in 512 pages of 64 bytes each. A two byte address word, following the Slave address, points to the first byte to be written . The most significant bit of the address word is ‘ don ’ t care ’ , the next 9 bits identify the page and the last 6 bits identify the byte within the page. Up to 64 bytes can be written in one Write cycle (Figure 8).
The internal byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 64 data bytes, then earlier bytes will be overwritten by later bytes in a ‘ wrap-around ’ fashion (within the selected page). The internal Write cycle starts immediately following the STOP.

Acknowledge Polling: Acknowledge polling can be used to determine if the CAT24C256 is busy writing or is ready to accept commands. Polling is implemented by interrogating the device with a ‘ Selective Read ’ command (see READ OPERATIONS). The CAT24C256 will not acknowledge the Slave address, as long as internal Write is in progress.

Hardware Write Protection: With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAT24C256. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the CAT24C256 will not acknowledge the data byte and the Write request will be rejected.

Delivery State: The CAT24C256 is shipped erased, i.e., all bytes are FFh.

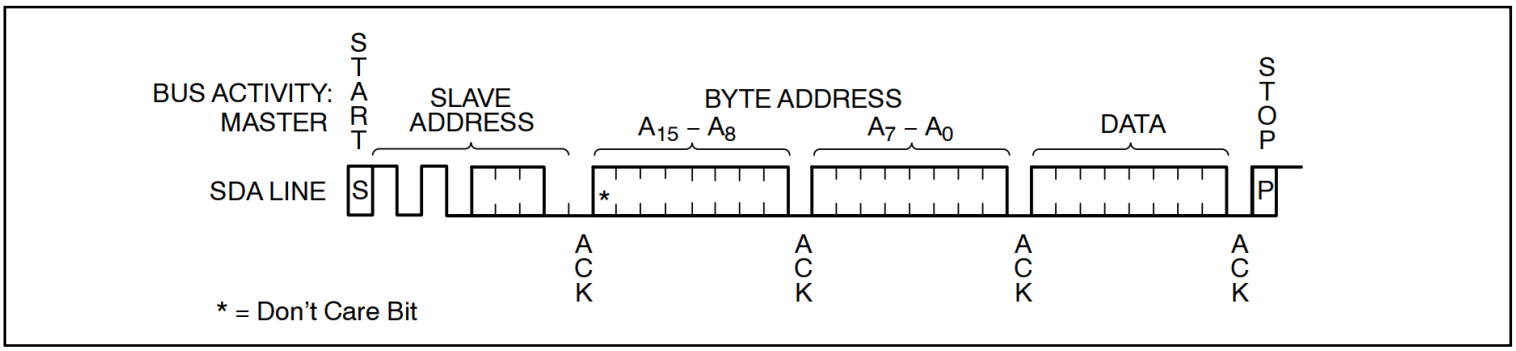


Figure 6. Byte Write Timing

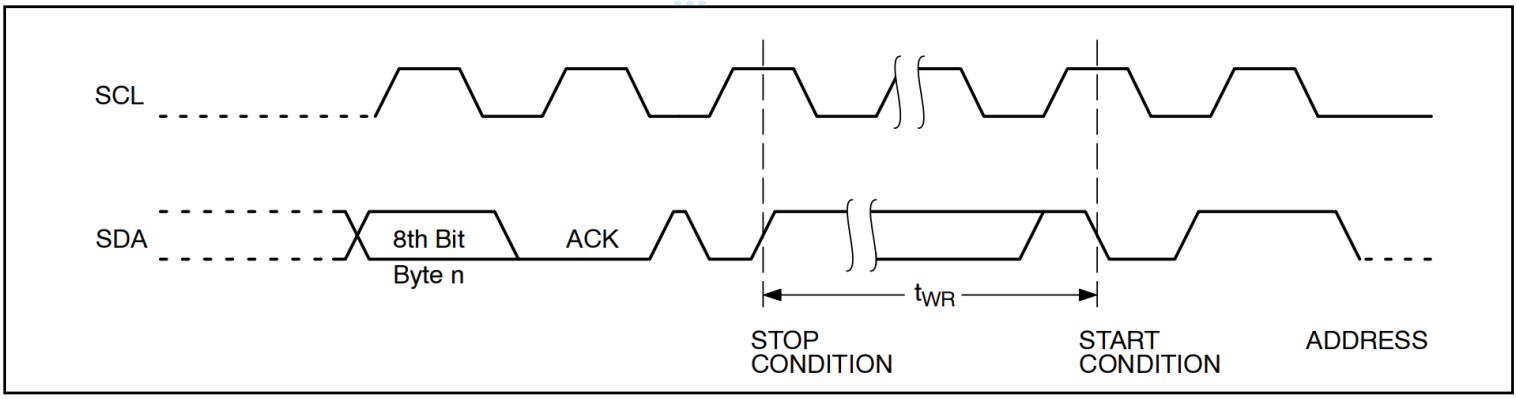


Figure 7. Write Cycle Timing

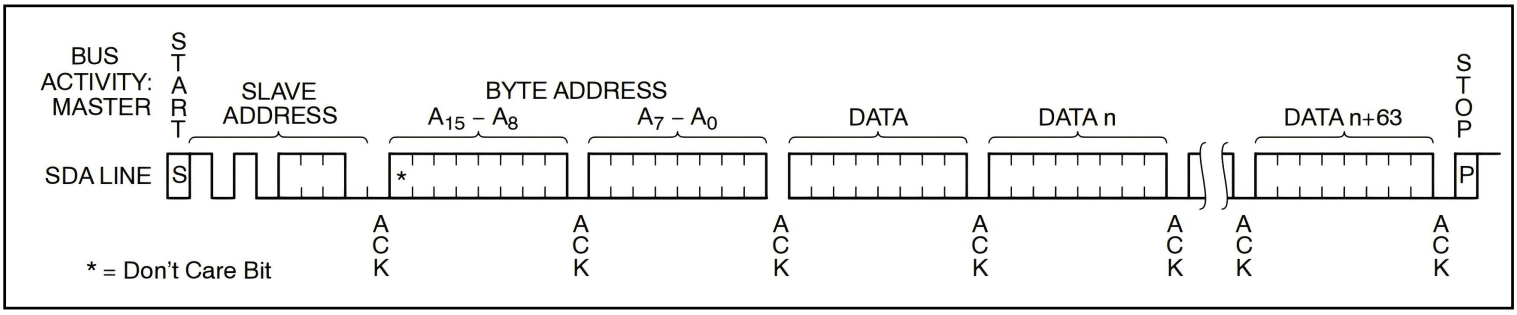


Figure 8. Page Write Timing

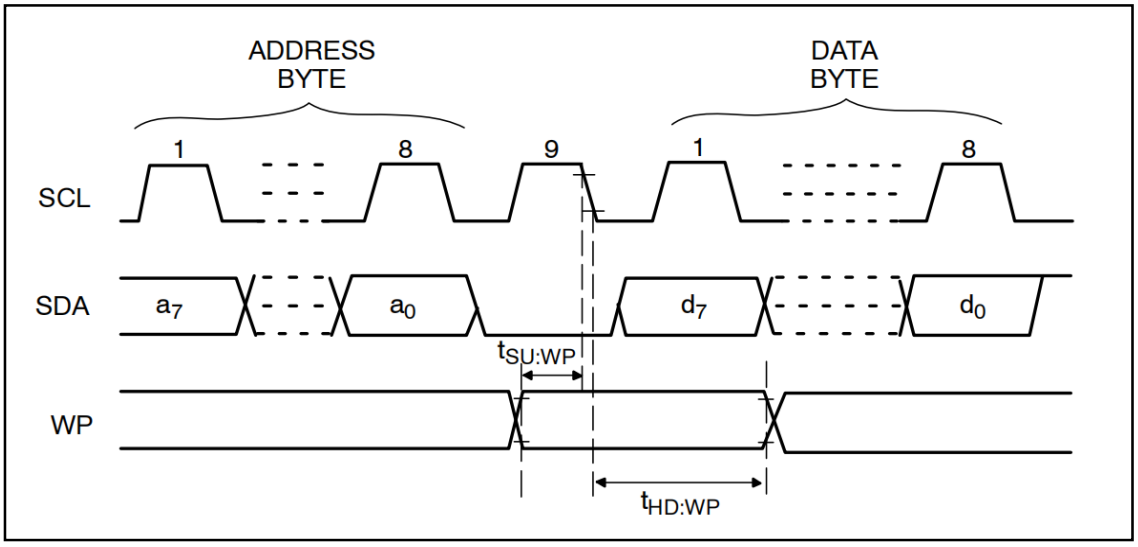


Figure 9. WP Timing

READ OPERATIONS

Immediate Address Read: In standby mode, the CAT24C256 internal address counter points to the data byte immediately following the last byte accessed by a previous operation. If that ‘ previous ’ byte was the last byte in memory, then the address counter will point to the 1st memory byte, etc. When, following a START, the CAT24C256 is presented with a Slave address containing a ‘ 1 ’ inthe R/W bit position (Figure 10), it will acknowledge (ACK) in the 9th clock cycle, and will then transmit data being pointed at by the internal address counter. The Master can stop further transmission by issuing a NoACK, followed by a STOP condition.

Selective Read: The Read operation can also be started at an address different from the one stored in the internal address counter. The address counter can be initialized by performing a ‘ dummy ’ Write operatio n (Figure 11). Here the START is followed by the Slave address (with the R/W bit set to ‘ 0 ’) and the desired two byte address. Instead of following up with data, the Master then issues a 2nd START, followed by the ‘ Immediate Address Read ’ sequence, as described earlier.

Sequential Read: If the Master acknowledges the 1st data byte transmitted by the CAT24C256, then the device will continue transmitting as long as each data byte is acknowledged by the Master (Figure 12). If the end of memory is reached during sequential Read, then the address counter will ‘ wrap?around ’ to the beginning of memory, etc. Sequential Read works with either ‘ Immediate Address Read ’ or ‘ Selective Read ’, the only difference being the starting byte address.

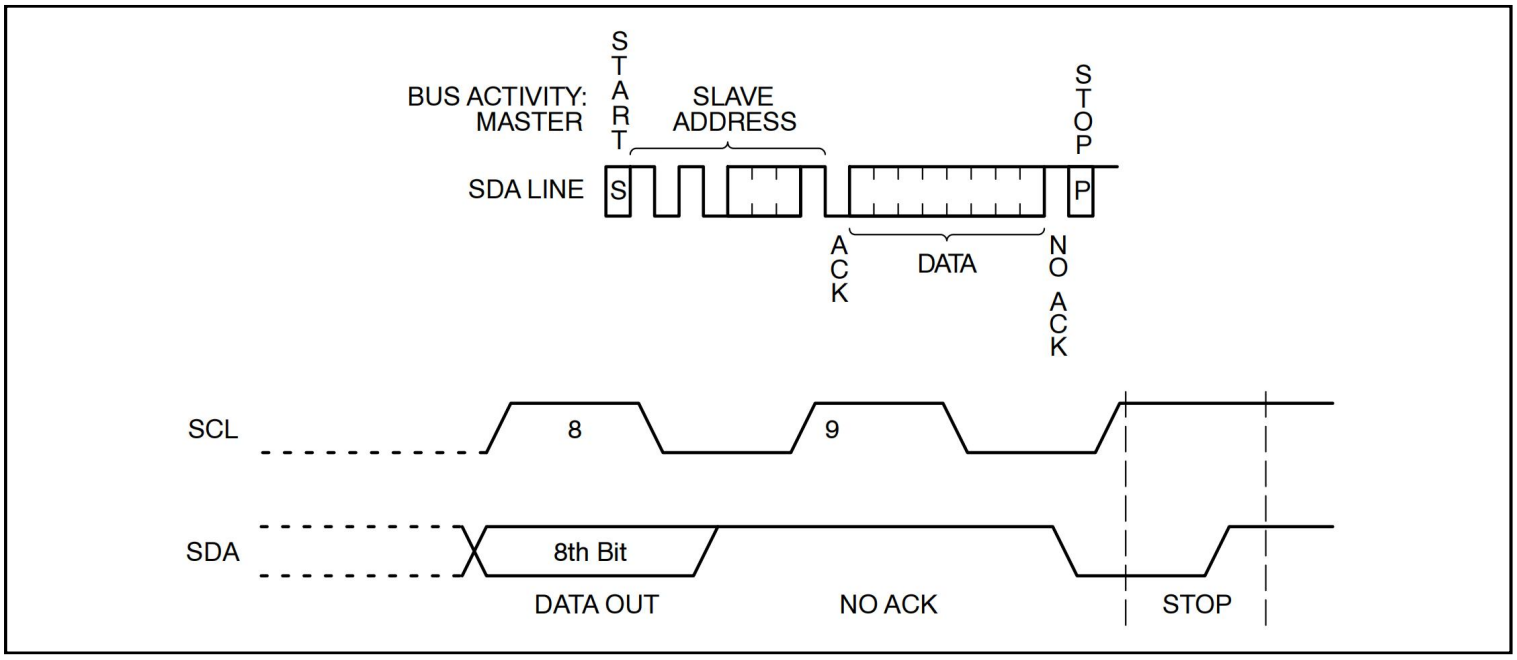


Figure 10. Immediate Address Read Timing

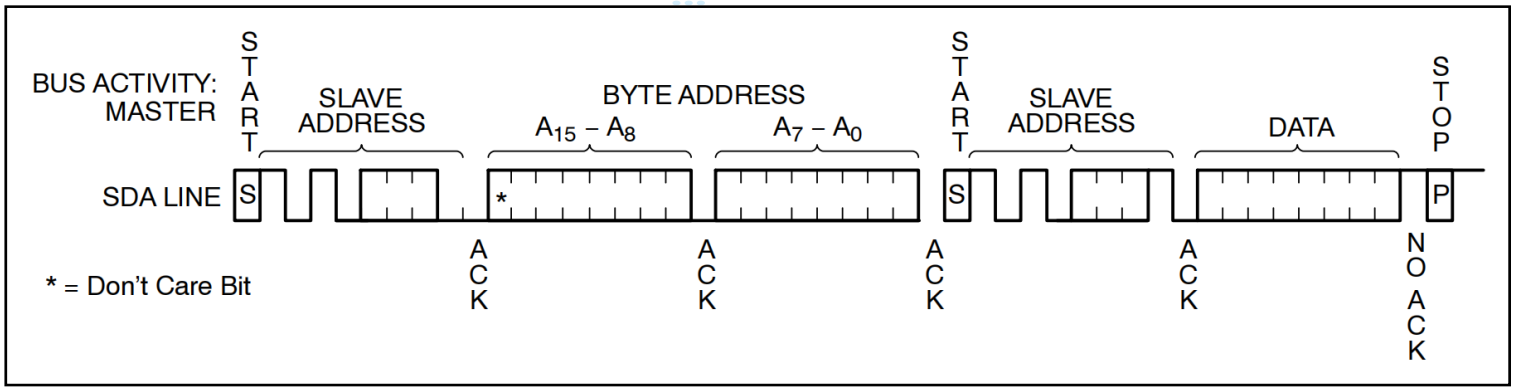


Figure 11. Selective Read Timing

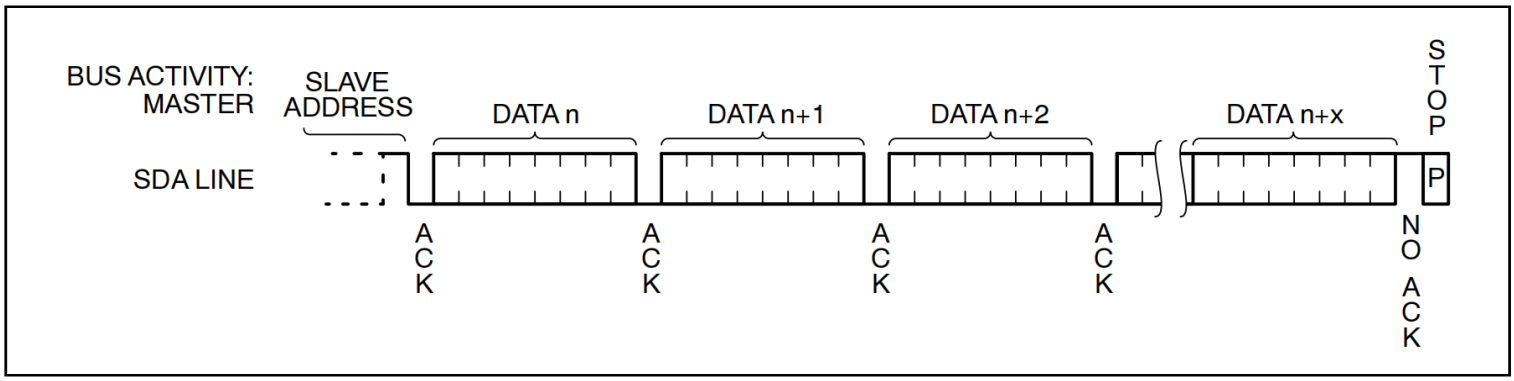


Figure 12. Sequential Read Timing

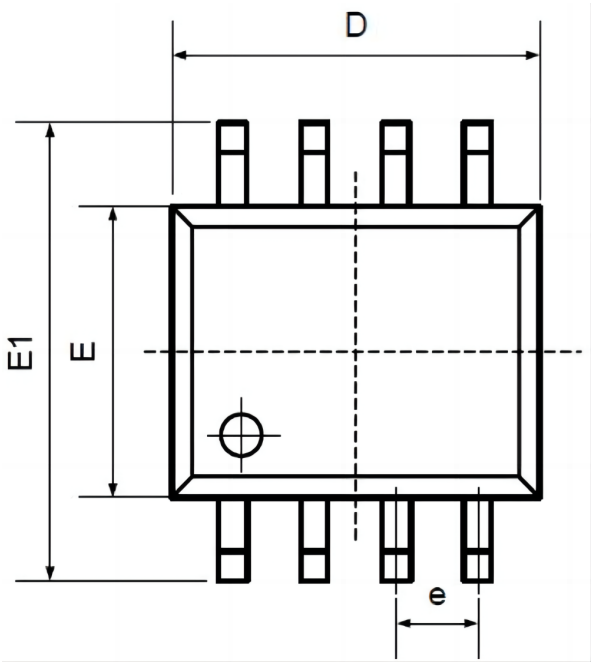
Order information

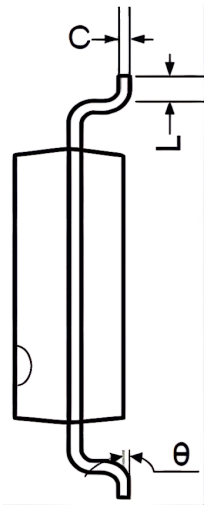
Order Number	Package	Package Quantity	Marking On The park	Temperature
CAT24C256LI-G-TUDI	DIP8	Tube,50,A box of 2000	24256E 24C256LI	-40°C to 85°C
CAT24C256WI-GT3-TUDI	SOP8	Tape,Reel,4000	24256E	
CAT24C256YI-GT3-TUDI	TSSOP8	Tape,Reel,4000	C56E 24256C	

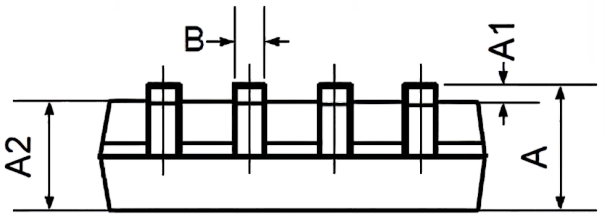
Revision history

	Date	Revision	Page
V1.0	2022/12	New	1-15
V1.1	2024/8	Update model and PDF template	1-20

Package SOP8

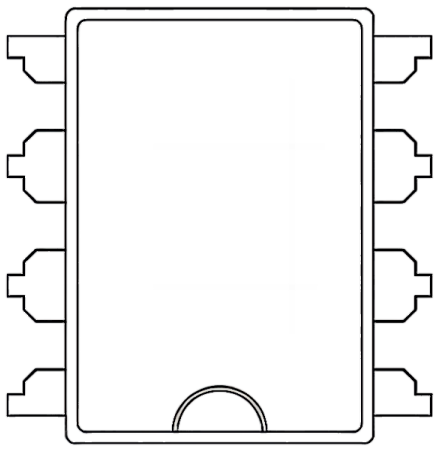


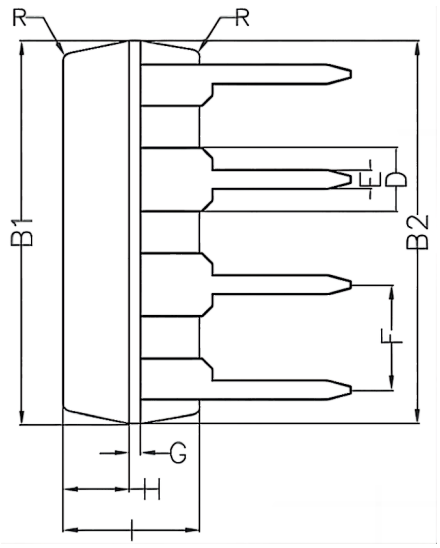


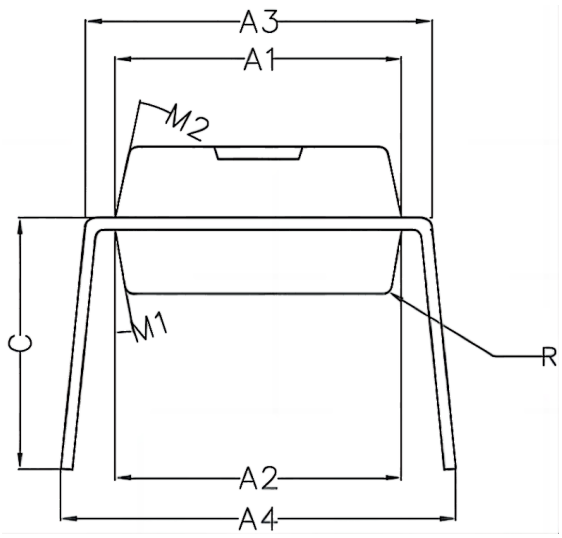


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package DIP8

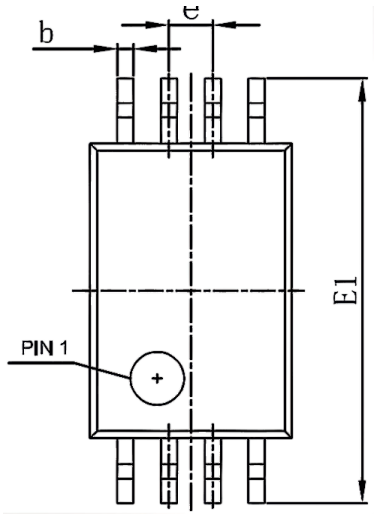


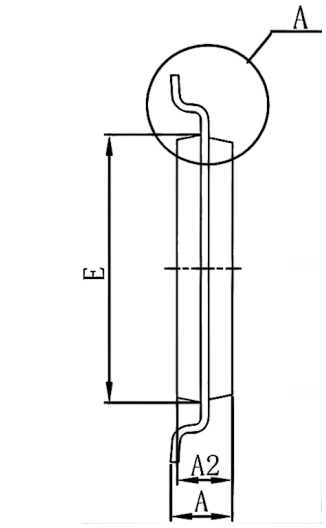


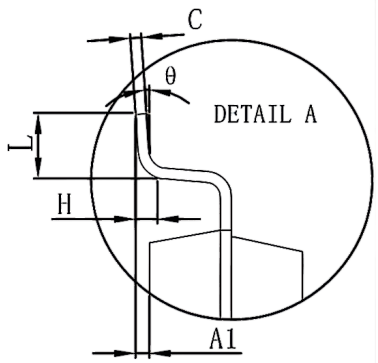


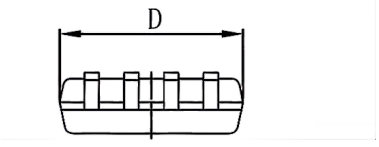
Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

Package TSSOP8









Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
C	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°		1°	

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