

钛地半导体
Tudi Semiconductor

# Product Specification

## TUDI-AT24C512C

## I² C-Compatiable (2-wire) Serial EEPROM 512-Kbit

网址 www.sztdbdt.com

**用芯智造·卓越品质**

**semiconductor device manufacturer**

- Design
- research and development
- production
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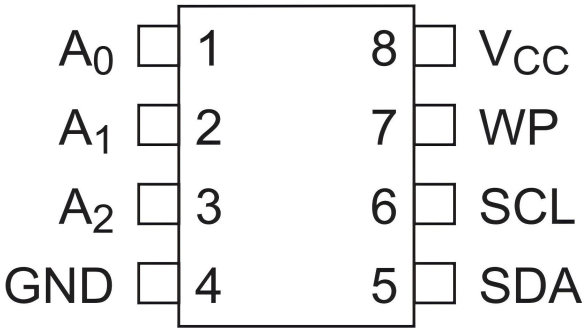
## Features



SOP8/TSSOP8

- Low-voltage and standard-voltage operation
- 1.7V (Vcc = 1.7V to 3.6V)
- 2.5V (Vcc = 2.5V to 5.5V)
- Internally organized as 65,536 x 8
- 2-wire serial interface
- Schmitt Triggers, filtered inputs for noise suppression
- Bidirectional data transfer protocol
- 400kHz (1.7V) and 1MHz (2.5V, 5.5V) compatibility
- Write Protect pin for hardware data protection
- 128-byte page write mode
- partial page writes allowed
- Random and sequential read modes
- Self-timed write cycle (5ms max)
- High reliability
- Endurance: 1,000,000 write cycles
- Data retention: 40 years
- Green package options (Pb/Halide-free/RoHS Compliant)
- 8-lead JEDEC SOIC, 8-lead EIAJ SOIC and 8-lead TSSOP packages
- Die sale options: wafer form and tape and reel available

## Description

The AT24C512C provides 524,288 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 65,536 words of eight bits each. The cascadable feature of the device allows up to eight devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space-saving 8-lead JEDEC SOIC, 8-lead EIAJ SOIC and 8-lead TSSOP packages. In addition, the entire family is available in 1.7V (1.7V to 3.6V) and 2.5V (2.5V to 5.5V) versions.

## Pin Configurations and Pinouts

Table 1. Pin Configurations

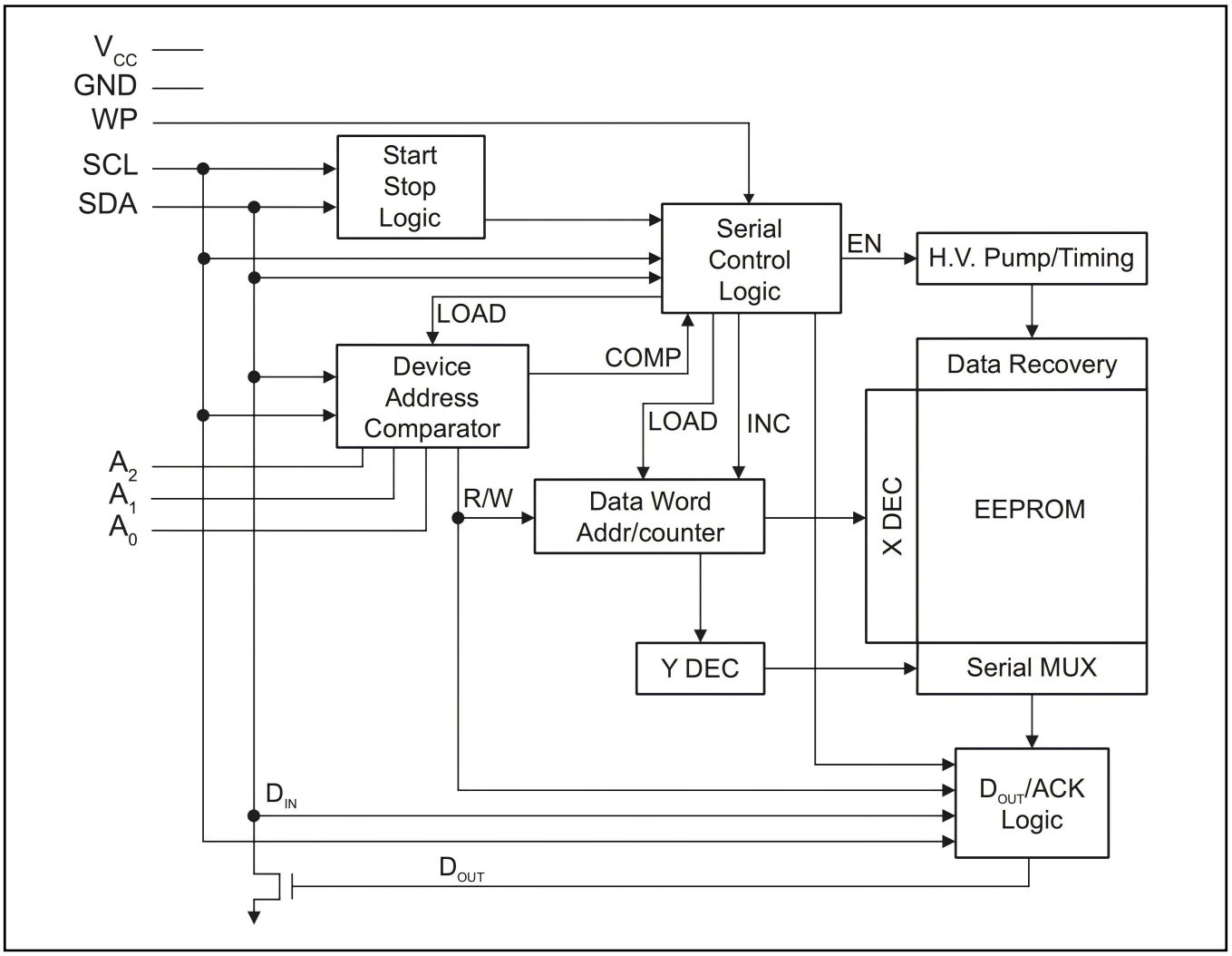
| Pin Name | Function |
|---|---|
| $A_0$-$A_2$ | Address Inputs |
| GND | Ground |
| SDA | Serial Data |
| SCL | Serial Clock Input |
| WP | Write Protect |
| $V_{CC}$ | Power Supply |

## Absolute Maximum Ratings

Operating Temperature . . . . . – 55°C to +125°C
Storage Temperature . . . . . – 65°C to +150°C
Voltage on any pin
with respect to ground . . . . . – 1.0V to +7.0V
Maximum Operating Voltage. . . . . 6.25V
DC Output Current. . . . . 5.0mA

Notice: Stresses beyond those listed under “ Absolute Maximum Ratings ” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Block Diagram




## Pin Descriptions

**Serial Clock (SCL)** :The SCL input is used to positive-edge clock data into each EEPROM device and negative-edge clock data out of each device.

**Serial Data (SDA)** : The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven, and may be wire-ORed with any number of other open-drain or open-collector devices.

**Device Addresses ($A_2$, $A_1$, $A_0$)** :The $A_2$, $A_1$, and $A_0$ pins are device address inputs that are hardwired or left not connected for compatibility with other TUDI AT24Cxx devices. When the pins are hardwired, as many as eight 512K devices may be addressed on a single bus system (see “ Device Addressing ” for more details). If these pins are left floating, the $A_2$, $A_1$, and $A_0$ pins will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, TUDI recommends always connecting the address pins to a known state. When using a pull-up resistor, TUDI recommends using 10kΩ or less.

**Write Protect (WP):**The Write Protect input, when connected to GND, allows normal write operations. When WP pin is connected directly to $V_{CC}$, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND; however, due to capacitive coupling that may appear during customer applications, TUDI recommends always connecting the WP pin to a known state. When using a pull-up resistor, TUDI recommends using 10kΩ or less.

**Table 2. Write Protect**

| WP Pin Status | Part of the Array Protected |
|---|---|
| | AT24C512C |
| At $V_{CC}$ | Full Array |
| At GND | Normal Read/Write Operations |

## Memory Organization

**AT24C512C, 512-Kbit Serial EEPROM:** The 512K is internally organized as 512 pages of 128 bytes each. Random word addressing requires a 16-bit data word address.

**Table 3. Pin Capacitance(1)**

Applicable over recommended operating range from $T_A$ = 25°C, f = 1.0MHz, $V_{CC}$ = 1.7V to 3.6V or 2.5V to 5.5V

| Symbol | Test Condition | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{I/O}$ | Input/Output Capacitance(SDA) | 8 | pF | $V_{I/O}$=0V |
| $C_{IN}$ | Input Capacitance($A_0$,$A_1$,$A_2$,SCL) | 6 | pF | $V_{IN}$=0V |

Note: 1. This parameter is characterized and is not 100% tested.

## Table 4. DC Characteristics

Applicable over recommended operating range from: $T_{AI}$ = −40°C to +85°C, $V_{CC}$ = 1.7V to 3.6V or 2.5V to 5.5V (unless otherwise noted)

| Symbol | Parameter | Test Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{CC1}$ | Supply Voltage | | | 1.7 | | 3.6 | V |
| $V_{CC2}$ | Supply Voltage | | | 2.5 | | 5.5 | V |
| $I_{CC1}$ | Supply Current | $V_{CC}$=5.0V | Read at 400kHz | | | 2.0 | mA |
| $I_{CC2}$ | Supply Current | $V_{CC}$=5.0V | Write at 400kHz | | | 3.0 | mA |
| $I_{SB1}$ | Standby Current | $V_{CC}$=1.7V | $V_{IN}$=$V_{CC}$ or Vss | | | 1.0 | μA |
| | | $V_{CC}$=3.6V | | | | 3.0 | μA |
| $I_{SB2}$ | Standby Current | $V_{CC}$=2.5V | $V_{IN}$=$V_{CC}$ or Vss | | | 2.0 | μA |
| | | $V_{CC}$=5.5V | | | | 6.0 | μA |
| $I_{LI}$ | Input Leakage Current | $V_{IN}$=$V_{CC}$ orVss | | | 0.10 | 3.0 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$=$V_{CC}$ orVss | | | 0.05 | 3.0 | μA |
| $V_{IL}$ | Input Low Level(1) | | | -0.6 | | $V_{CC}$×0.3 | V |
| $V_{IH}$ | Input High Level(1) | | | $V_{CC}$×0.7 | | $V_{CC}$+0.5 | V |
| $V_{OL1}$ | Output Low Level | $V_{CC}$=1.7V | $I_{OL}$=0.15mA | | | 0.2 | V |
| $V_{OL2}$ | Output Low Level | $V_{CC}$=3.0V | $I_{OL}$=2.1mA | | | 0.4 | V |

Note: 1. $V_{IL}$ min and $V_{IH}$ max are reference only, and are not tested

## Table 5. AC Characteristics

Applicable over recommended operating range from $T_{AI}$ = -40°C to +85°C, $V_{CC}$ = 1.7V to 3.6V or 2.5V to 5.5V (where applicable), CL = 100pF (unless otherwise noted). Test conditions are listed in Note 2.

| Symbol | Parameter | 1.7V | | 2.5V,5.0V | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $f_{SCL}$ | Clock Frequency,SCL | | 400 | | 1000 | kHz |
| $t_{LOW}$ | Clock Pulse Width Low | 1.3 | | 0.4 | | μ s |
| $t_{HIGH}$ | Clock Pulse Width High | 0.6 | | 0.4 | | μ s |
| $t_I$ | Noise Suppression Time(1) | | 100 | | 50 | ns |
| $t_{AA}$ | Clock Low to Data Out Valid | 0.05 | 0.9 | 0.05 | 0.55 | μs |
| $t_{BUF}$ | Time the bus must be free before a new transmission can start(1) | 1.3 | | 0.5 | | μ s |
| $t_{HD.STA}$ | Start Hold Time | 0.6 | | 0.25 | | μs |
| $t_{SU.STA}$ | Start Set-up Time | 0.6 | | 0.25 | | μ s |
| $t_{HD.DAT}$ | Data In Hold Time | 0 | | 0 | | μ s |
| $t_{SU.DAT}$ | Data In Set-up Time | 100 | | 100 | | ns |
| $t_R$ | Inputs Rise Time(1) | | 0.3 | | 0.3 | μ s |
| $t_F$ | Inputs Fall Time(1) | | 300 | | 100 | ns |
| $t_{SU.STO}$ | Stop Set-up Time | 0.6 | | 0.25 | | μs |
| $t_{DH}$ | Data Out Hold Time | 50 | | 50 | | ns |
| $t_{WR}$ | Write Cycle Time | | 5 | | 5 | ms |
| Endurance(1) | 25℃,Page Mode,3.3V | 1,000,000 | | | | Write Cycles |

Notes: 1. This parameter is ensured by characterization only.
2. AC measurement conditions:

- $R_L$ (connects to $V_{CC}$): 1.3kΩ (2.5V, 5V), 10kΩ (1.7V)
- Input pulse voltages: 0.3$V_{CC}$ to 0.7$V_{CC}$
- Input rise and fall times:≦50ns
- Input and output timing reference voltages: 0.5$V_{CC}$

## Device Operation

**Clock and Data Transitions:** The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 4 ). Data changes during SCL high periods will indicate a Start or Stop condition as defined below.
**Start Condition:** A high-to-low transition of SDA with SCL high is a Start condition, which must precede any other command (see Figure 5 ).
**Stop Condition:** A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 5 ).
**Acknowledge:** All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.
**Standby Mode:** The AT24C512C features a low-power standby mode, which is enabled:
●Upon power-up and
●After the receipt of the Stop bit and the completion of any internal operations.
**Software Reset:** After an interruption in protocol, power loss, or system reset, any 2-wire part can be protocol reset by following these steps:
1. Create a Start condition
2. Clock nine cycles
3. Create another Start condition followed by a Stop condition, as shown in Figure 1 below.
The device is ready for the next communication after the above steps have been completed.

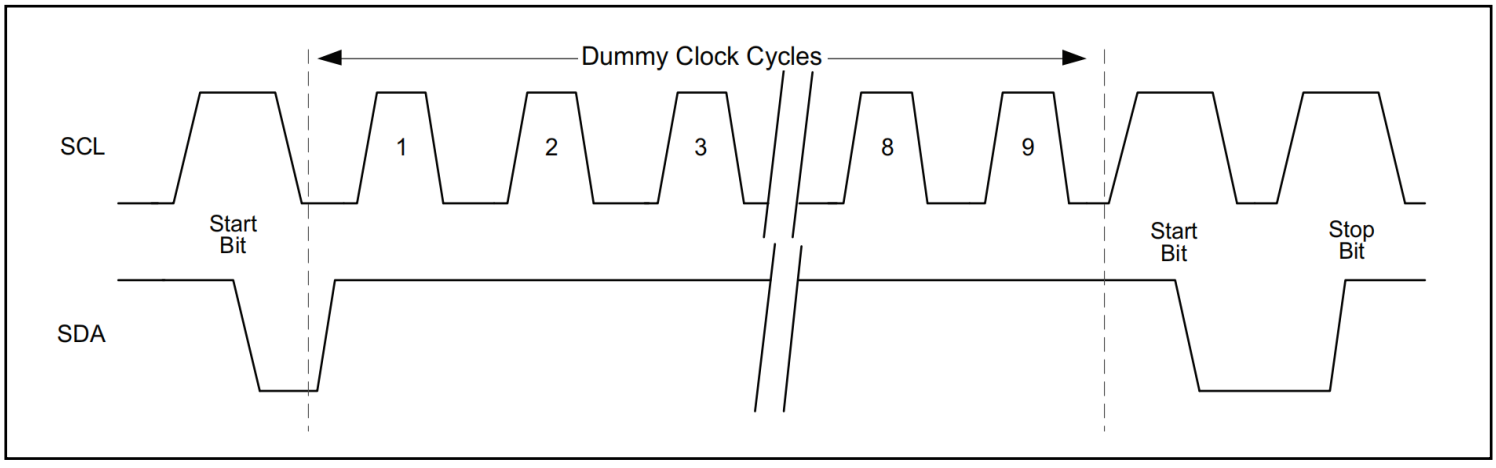



Figure 1. Software Reset

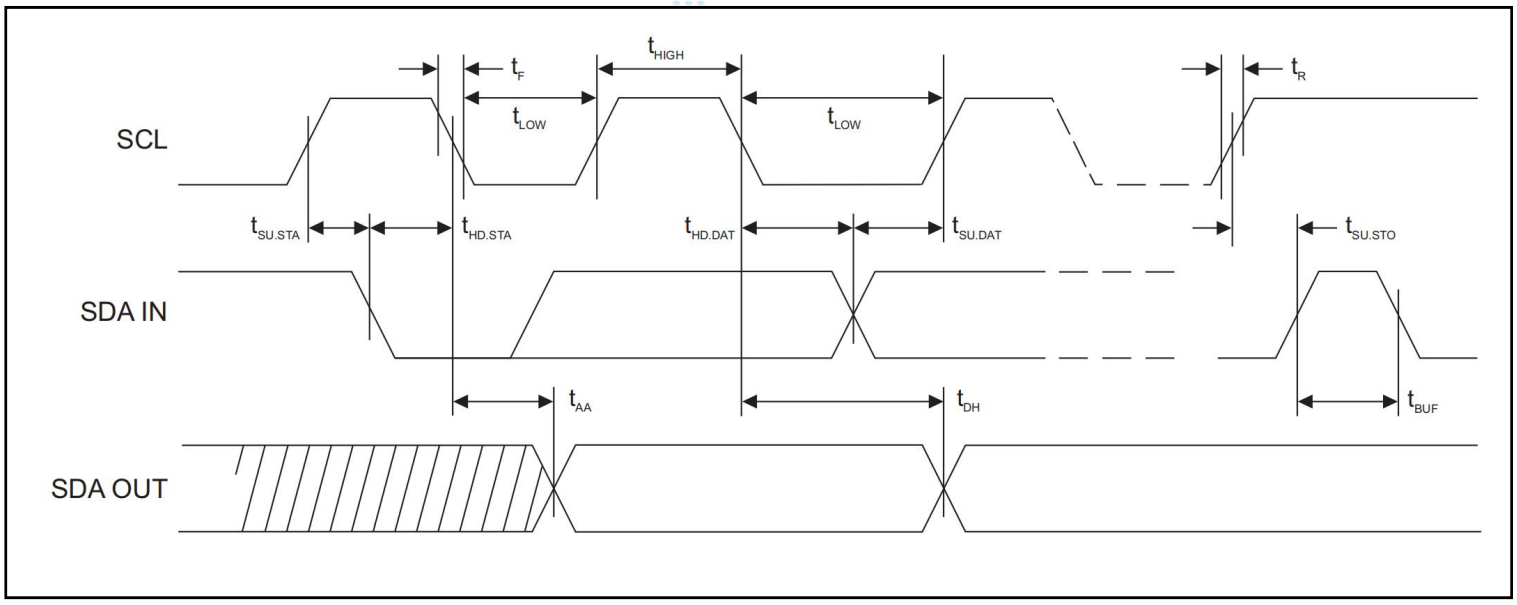



Figure 2. Bus Timing

SCL: Serial Clock, SDA: Serial Data I/O

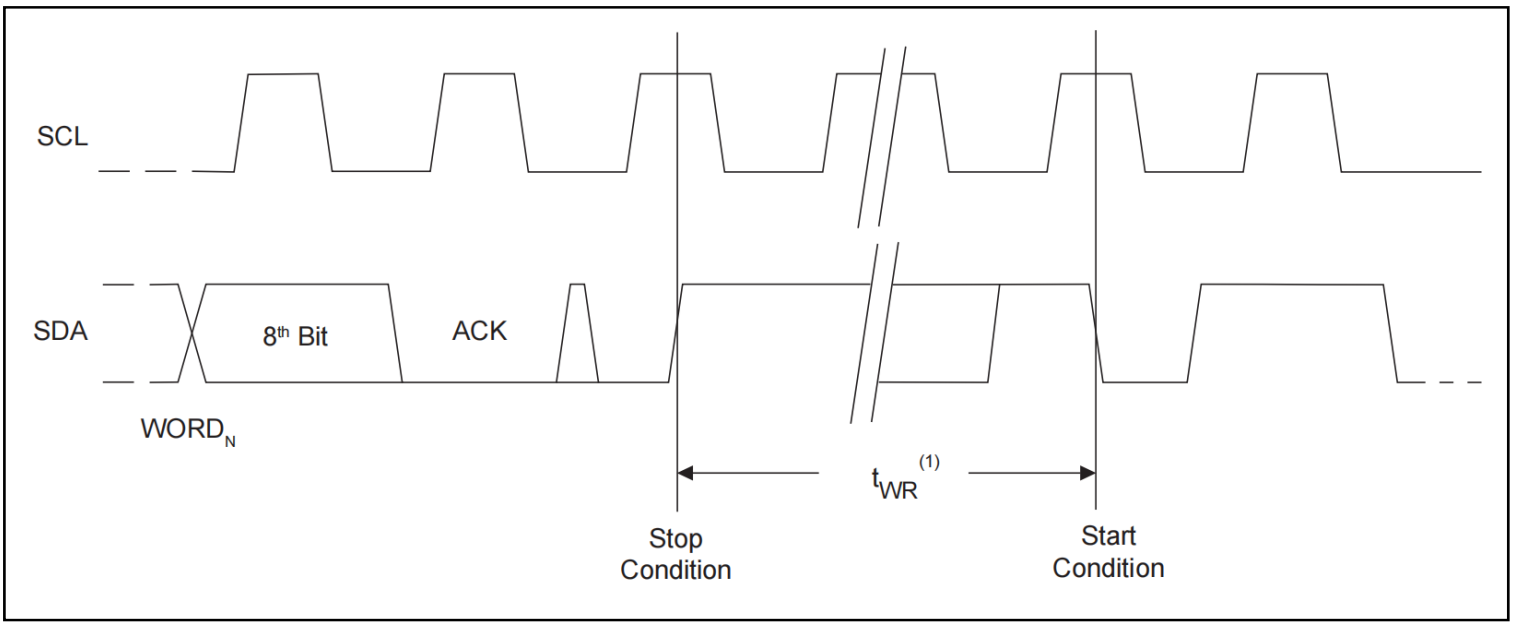



Figure 3. Write Cycle Timing

SCL: Serial Clock, SDA: Serial Data I/O

Notes: 1. The write cycle time, $t_{WR}$, is the time from a valid Stop condition of a write sequence to the end of the internal clear/ write cycle.

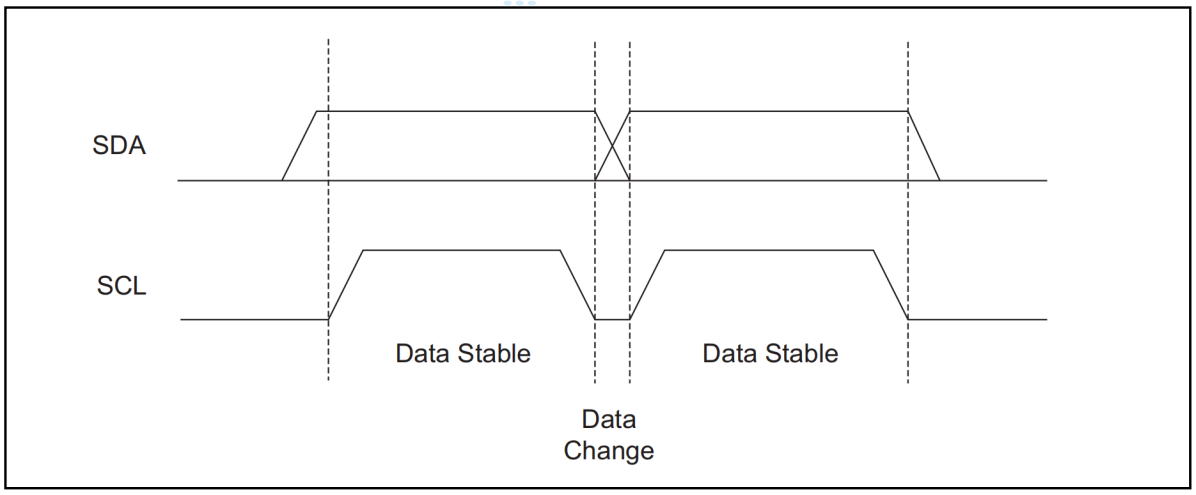



Figure 4. Data Validity

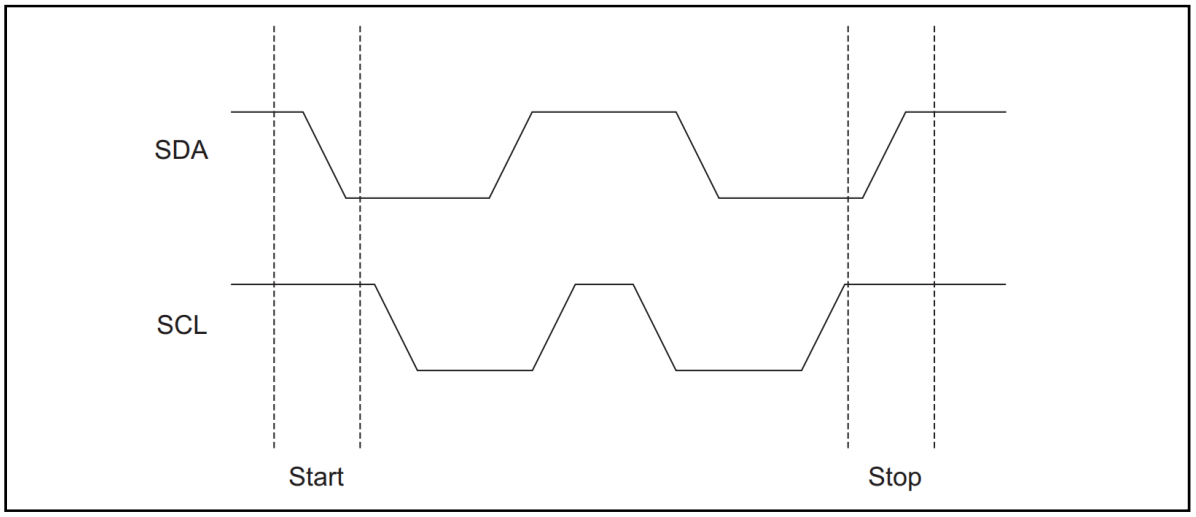



Figure 5. Start and Stop Definition

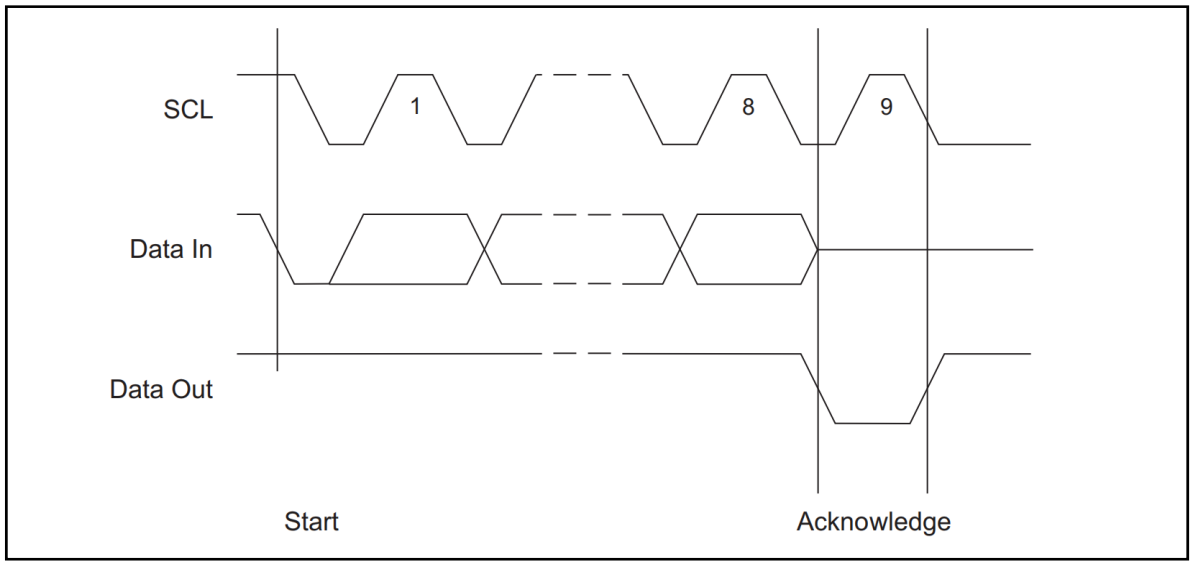



Figure 6. Output Acknowledge

## Device Addressing

The 512K EEPROM requires an 8-bit device address word following a Start condition to enable the chip for a read or write operation. The device address word consists of a mandatory ‘ 1010 ’ sequence for the first four most-significant bits (see Figure 7 below). This is common to all 2-wire EEPROM devices.
The 512K uses the three device address bits, A2, A1, and A0, to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The $A_2$, $A_1$, and $A_0$ pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.
The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high, and a write operation is initiated if this bit is low.
Upon a compare of the device address, the EEPROM will output a zero. If a valid compare is not made, the device will return to a standby state.

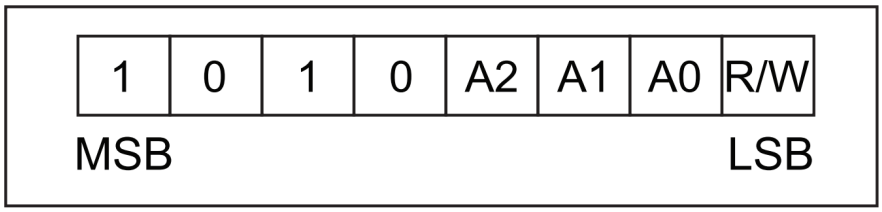



Figure 7. Device Address

## Write Operations

**Byte Write:** A Byte Write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero, and then the part is to receive an 8-bit data word. Following receipt of the 8 -bit data word, the EEPROM will output a zero. The addressing device, such as a microcontroller, then must terminate the write sequence with a Stop condition. At this time, the EEPROM enters an internally-timed write cycle, $t_{WR}$, to the nonvolatile memory. All inputs are disabled during this write cycle, and the EEPROM will not respond until the write is complete (see Figure 8).
**Page Write:** The 512-Kbit EEPROM is capable of 128-byte page writes.
A Page Write is initiated the same way as a byte write, but the microcontroller does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 127 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a Stop condition (see Figure 9) and the internally timed write cycle will begin.
The lower seven bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 128 data words are

transmitted to the EEPROM, the data word address will roll-over, and the previous data will be overwritten. The address roll over during write is from the last byte of the current page to the first byte of the same page.

**Acknowledge Polling:** Once the internally-timed write cycle has started and the EEPROM inputs are disabled, Acknowledge Polling can be initiated. This involves sending a Start condition followed by the device address word. The read/write select bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

**Data Security:** AT24C512C has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at $V_{CC}$.

## Read Operations

Read operations are initiated the same way as write operations with the exception that the read/ write select bit in the device address word is set to one. There are three types of read operations : Current Address Read, Random Address Read, and Sequential Read.

**Current Address Read:** The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out on the SDA line. The microcontroller does not respond with an zero, but does generate a following Stop condition (see Figure 10 ).

**Random Read:** A Random Read requires an initial byte write sequence to load in the data word address. This is known as a “ dummy write ” operation. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another Start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero, but does generate a following Stop condition (see Figure 11 ).

**Sequential Read:** Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the sequential read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a zero but does generate a following Stop condition (see Figure 12 ).

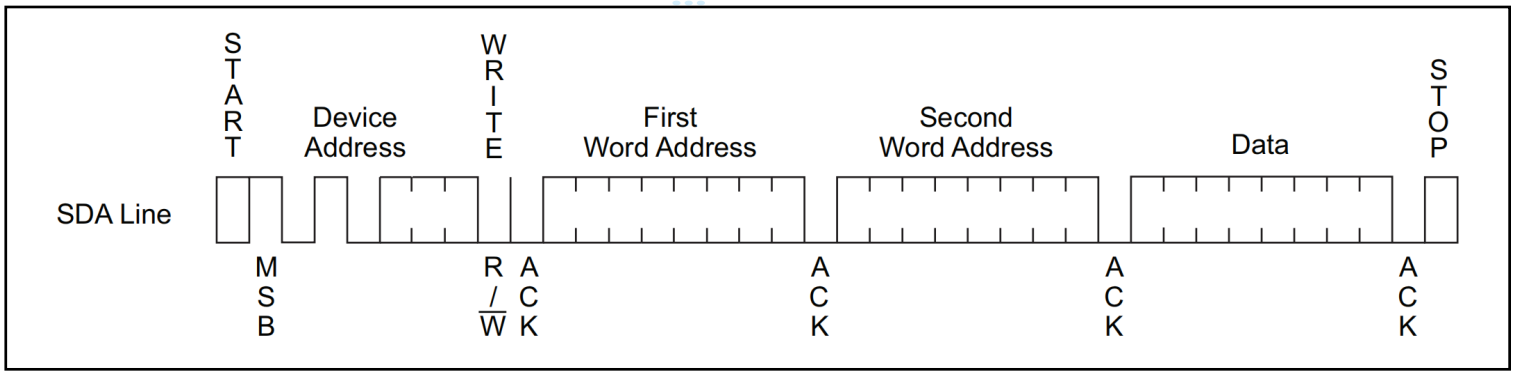



Figure 8. Byte Write

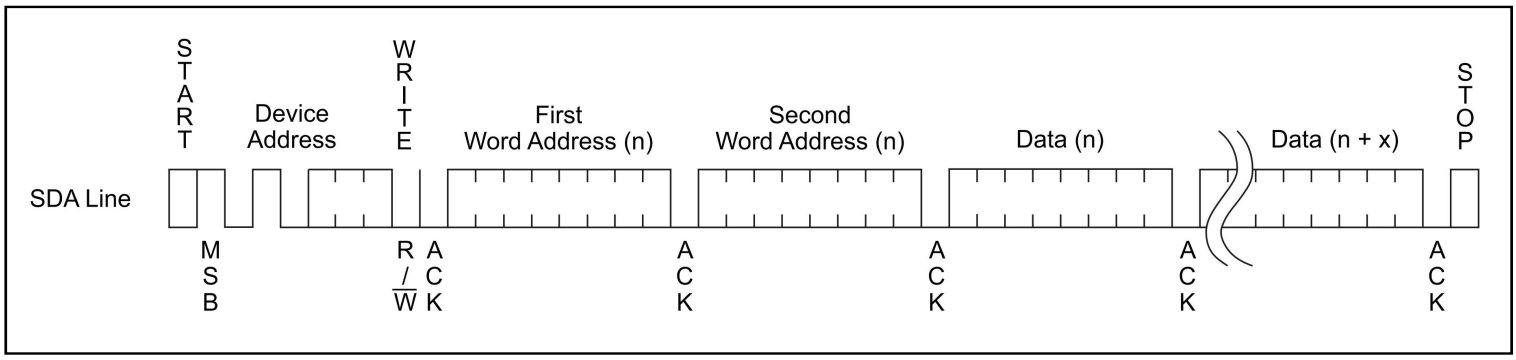



Figure 9. Page Write

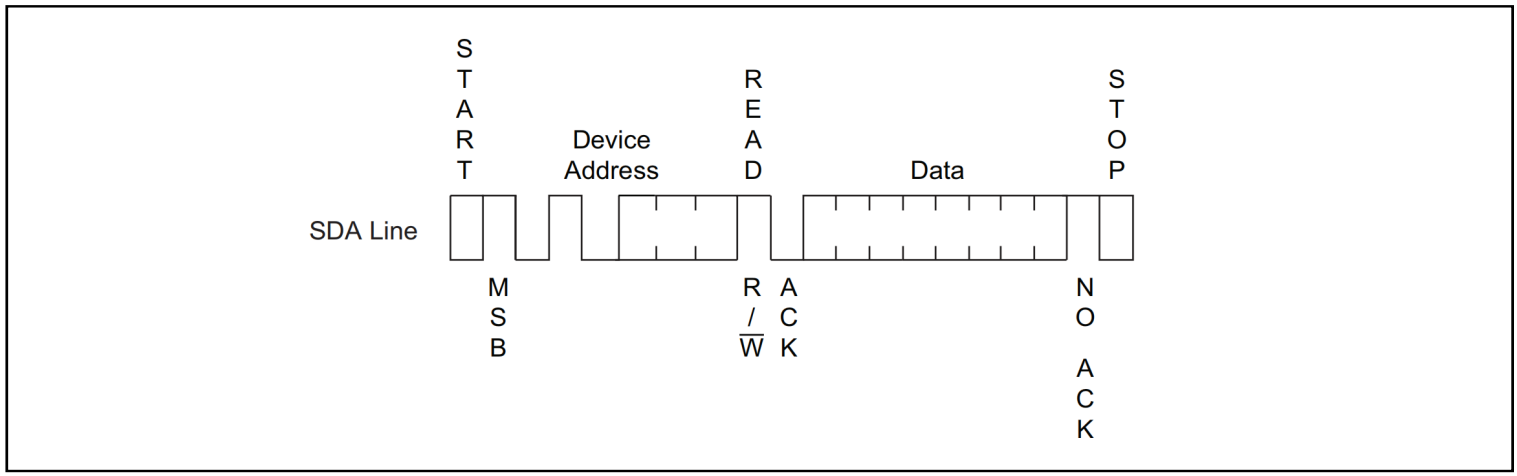



Figure 10. Current Address Read

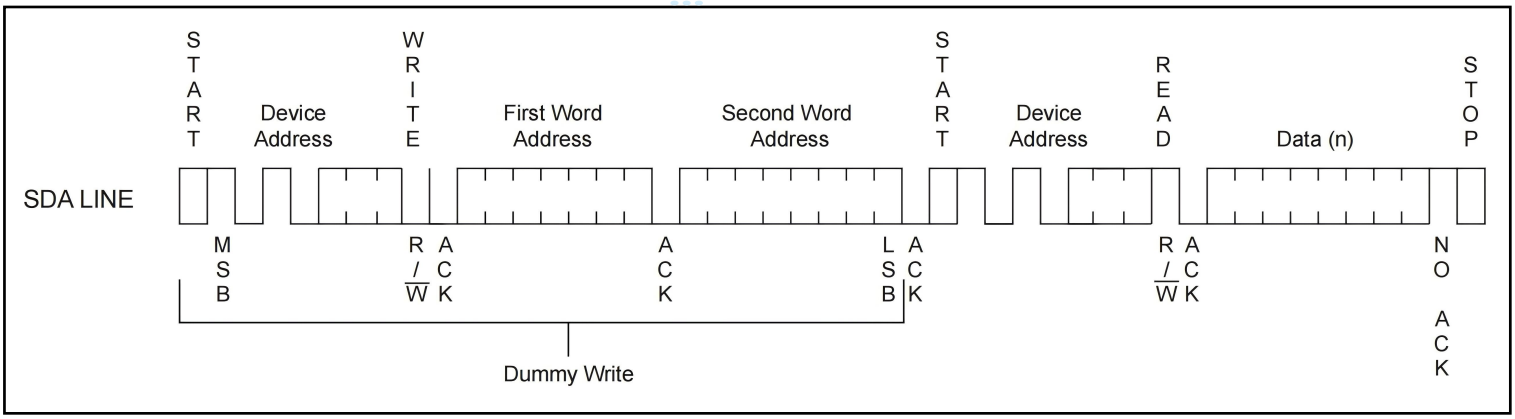



Figure 11. Random Read

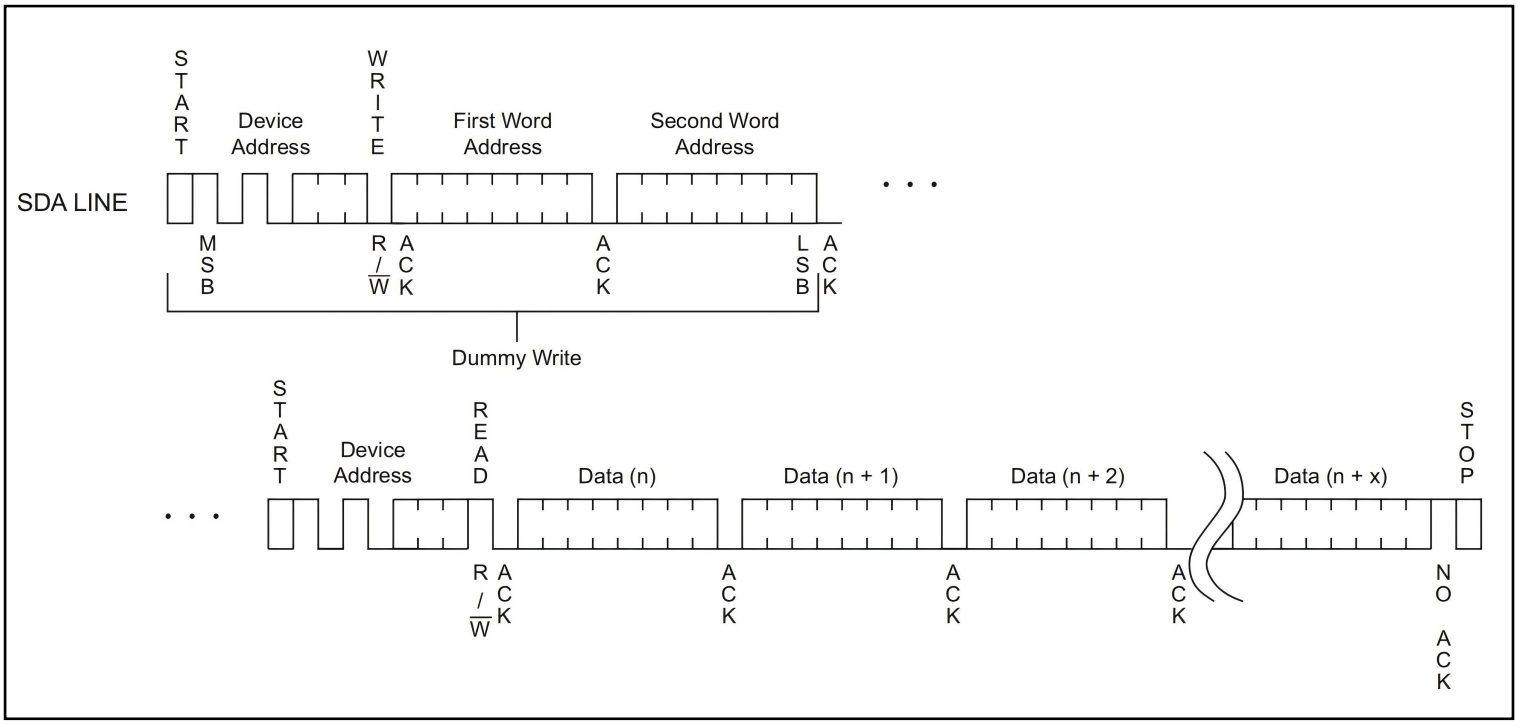



Figure 12. Sequential Read

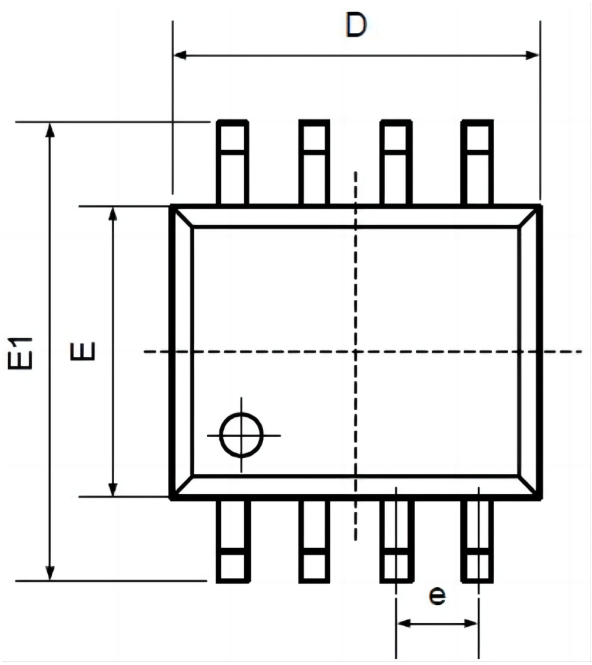
# Order information

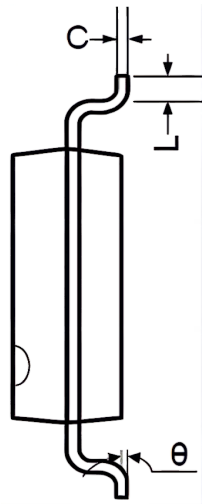
| Order Number | Package | Package Quantity | Marking On The park | Temperature |
|---|---|---|---|---|
| AT24C512C-SSHM-T-TUDI | SOP8 | Tape,Reel,4000 | 24C512C | -40°C to 85°C |
| | | | 2FCM | |
| AT24C512C-SSHD-T-TUDI | SOP8 | Tape,Reel,4000 | 24C512D | |
| | | | 2FCD | |
| AT24C512C-XHM-T-TUDI | TSSOP8 | Tape,Reel,4000 | 2FCM | |

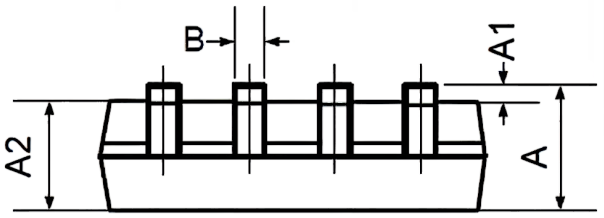
# Revision history

| | Date | Revision | Page |
|---|---|---|---|
| V1.0 | 2022/9 | New | 1-15 |
| V1.1 | 2025/6 | Update model and PDF template | 1-18 |

# Package SOP8

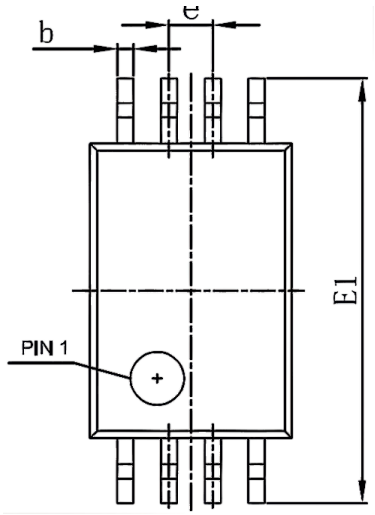


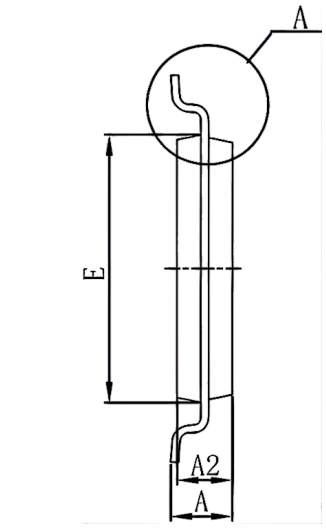



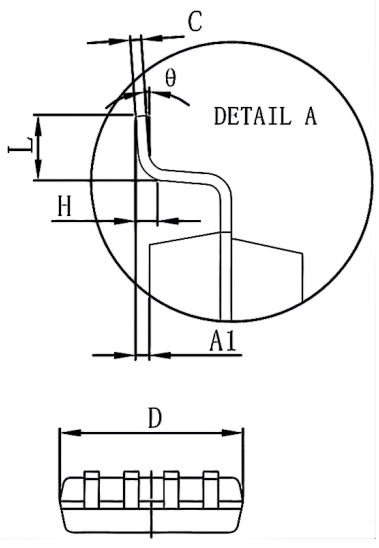




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| B | 0.330 | 0.510 | 0.013 | 0.020 |
| C | 0.190 | 0.250 | 0.007 | 0.010 |
| D | 4.780 | 5.000 | 0.188 | 0.197 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.300 | 0.228 | 0.248 |
| e | 1.270TYP | | 0.050TYP | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

# Package TSSOP8







| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| E | 4.300 | 4.500 | 0.169 | 0.177 |
| b | 0.190 | 0.300 | 0.007 | 0.012 |
| C | 0.090 | 0.200 | 0.004 | 0.008 |
| E1 | 6.250 | 6.550 | 0.246 | 0.258 |
| A | | 1.200 | | 0.047 |
| A2 | 0.800 | 1.000 | 0.031 | 0.039 |
| A1 | 0.050 | 0.150 | 0.002 | 0.006 |
| e | 0.65(BSC) | | 0.026(BSC) | |
| L | 0.500 | 0.700 | 0.020 | 0.028 |
| H | 0.25(TYP) | | 0.01(TYP) | |
| θ | 1° | | 1° | |

# Important statement:

●TUDI Semiconductor reserves the right to modify the product manual without prior notice! Before placing an order, customers need to confirm whether the obtained information is the latest version and verify the completeness of the relevant information.

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