General Description

The LTC324H of quad-channel amplifiers provides input offset voltage correction for positive low offset (2.5 mV maximum) and drift (1 µV/℃) through the use of proprietary techniques. Featuring rail-to-rail input and output swings, and low quiescent current (total 375 µA typically) combined with a wide bandwidth of 1.2 MHz and low noise (30 nV/√Hz at 1 kHz) makes this family very attractive for a variety of battery-powered applications such as handsets, tablets, notebooks, and portable medical devices. The low input bias current supports these amplifiers to be used in applications with mega-ohm source impedances.

The robust design of the LTC324H amplifiers provides ease-of-use to the circuit designer: unity-gain stability with capacitive loads of up to 500 pF, integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electro-static discharge (ESD) protection (5-kV HBM). The LTC324H amplifiers are optimized for operation at voltages as low as +1.8 V (±0.9 V) and up to +5.5 V (±2.75 V) at the temperature range of 0 ℃ to 70 ℃, and operation at voltages from +2.0 V (±1.0 V) to +5.5 V (±2.75 V) over the extended temperature range of −40 ℃ to +125 ℃.

The quad-channel LTC324H is offered in both SOIC-14L and TSSOP-14L packages.

Features and Benefits

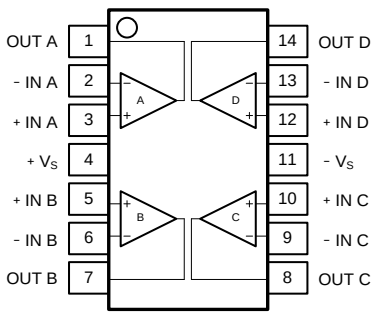
- Precision: 2.5 mV Maximum Positive Input Offset Voltage
- Low Noise: 30 nV/√Hz at 1 kHz
- 1.2 MHz GBW for Unity-Gain Stable
- Micro-Power: Total 375 µA Supply Current
- Single 1.8 V to 5.5 V Supply Voltage Range at 0 ℃ to 70 ℃
- Rail-to-Rail Input and Output
- Internal RF/EMI Filter
- Extended Temperature Range: −40℃ to +125℃

Applications

- Battery-Powered Instruments:
  - Consumer, Industrial, Medical, Notebooks
- Wireless Chargers
- Audio Outputs
- Sensor Signal Conditioning:
  - Sensor Interfaces, Loop-Powered, Active Filters
- Wireless Sensors:
  - Home Security, Remote Sensing, Wireless Metering

Pin Configurations (Top View)

LTC324H
SOIC-14L / TSSOP-14L



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Pin Description

Symbol	Description
–IN	Inverting input of the amplifier. The voltage range is from (V_{S-} – 0.1V) to (V_{S+} + 0.1V).
+IN	Non-inverting input of the amplifier. This pin has the same voltage range as –IN.
$+V_S$	Positive power supply. The voltage is from 2.0V to 5.5V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is from 2.0V to 5.5V.
$-V_S$	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 2.0V to 5.5V.
OUT	Amplifier output.

Ordering Information

Type Number	Package Name	Package Quantity	Marking Code (1)
LTC324HXS14/R5	SO-14	Tape and Reel, 2 500	324 T, AG4IX
LTC324HXT14/R6	TSSOP-14	Tape and Reel, 3 000	324 T, AG4IX

(1) There may be multiple device markings, a varied marking character of "x" , or additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

Limiting Value

In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameter	Absolute Maximum Rating
Supply Voltage, V_{S+} to V_{S-}	10.0 V
Signal Input Terminals: Voltage, Current	V_{S-} – 0.3 V to V_{S+} + 0.3 V, ±10 mA
Output Short-Circuit	Continuous
Storage Temperature Range, T_{stg}	–65 ℃ to +150 ℃
Junction Temperature, T_J	150 ℃
Lead Temperature Range (Soldering 10 sec)	260 ℃

ESD Rating

Parameter	Item	Value	Unit
Electrostatic Discharge Voltage	Human body model (HBM), per MIL-STD-883J / Method 3015.9 (1)	±5 000	V
	Charged device model (CDM), per ESDA/JEDEC JS-002-2014 (2)	±2 000	
	Machine model (MM), per JESD22-A115C	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

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Electrical Characteristics

V_S = 5.0V, T_A = +25°C, V_{CM} = V_S/2, V_O = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40 to +125 °C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OFFSET VOLTAGE						
V_{OS}	Input offset voltage		0		+2.5	mV
V_{OS} TC	Offset voltage drift	T_A = −40 to +125 °C		±1	3	µV/°C
PSRR	Power supply rejection ratio	V_S = 2.0 to 5.5 V, V_{CM} < V_{S+} − 2V	80	106		dB
		T_A = −40 to +125 °C	75			
INPUT BIAS CURRENT						
I_B	Input bias current			1		pA
		T_A = +85 °C		150		
		T_A = +125 °C		500		
I_{OS}	Input offset current			5		pA
NOISE						
V_n	Input voltage noise	f = 0.1 to 10 Hz		6		μV_{P-P}
e_n	Input voltage noise density	f = 10 kHz		27		nV/√Hz
		f = 1 kHz		30		
I_n	Input current noise density	f = 1 kHz		10		fA/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		V_{S-}−0.1		V_{S+}+0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, V_{CM} = −0.1 to 5.6 V	80	94		dB
		V_{CM} = 0 to 5.3 V, T_A = −40 to +125 °C	72			
		V_S = 2.0 V, V_{CM} = −0.1 to 2.1 V	74	86		
		V_{CM} = 0 to 1.8 V, T_A = −40 to +125 °C	66			
INPUT IMPEDANCE						
C_{IN}	Input capacitance	Differential		2.0		pF
		Common mode		3.5		
OPEN-LOOP GAIN						
A_{VOL}	Open-loop voltage gain	R_L = 10 kΩ, V_O = 0.05 to 3.5 V	90	105		dB
		T_A = −40 to +125 °C	85			
		R_L = 600 Ω, V_O = 0.15 to 3.5 V	85	100		
		T_A = −40 to +125 °C	80			
FREQUENCY RESPONSE						
GBW	Gain bandwidth product			1.2		MHz
SR	Slew rate	G = +1, C_L = 100 pF, V_O = 1.5 to 3.5 V		1.0		V/µs
THD+N	Total harmonic distortion + noise	G = +1, f = 1 kHz, V_O = 1 V_{RMS}		0.003		%
t_S	Settling time	To 0.1%, G = +1, 1V step		1.5		µs
		To 0.01%, G = +1, 1V step		1.8		
t_{OR}	Overload recovery time	To 0.1%, V_{IN} * Gain > V_S		2.5		µs

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Electrical Characteristics (continued)

V_S = 5.0V, T_A = +25°C, V_{CM} = V_S/2, V_O = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40 to +125 °C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OUTPUT						
V_{OH}	High output voltage swing	R_L = 50 kΩ	V_{S+}−6	V_{S+}−3		mV
		R_L = 2 kΩ	V_{S+}−100	V_{S+}−65		
V_{OL}	Low output voltage swing	R_L = 50 kΩ		V_{S-}+2	V_{S-}+4	mV
		R_L = 2 kΩ		V_{S-}+42	V_{S-}+65	
I_{SC}	Short-circuit current	Source current through 10Ω		45		mA
		Sink current through 10Ω		55		
POWER SUPPLY						
V_S	Operating supply voltage	T_A = 0 to +70 °C	1.8		5.5	V
		T_A = −40 to +125 °C	**2.0**		**5.5**	
I_Q	Quiescent current			375	490	µA
THERMAL CHARACTERISTICS						
T_A	Operating temperature range		−40		+125	°C
$θ_{JA}$	Package Thermal Resistance	TSSOP-14L		112		°C/W
		SOIC-14L		115		

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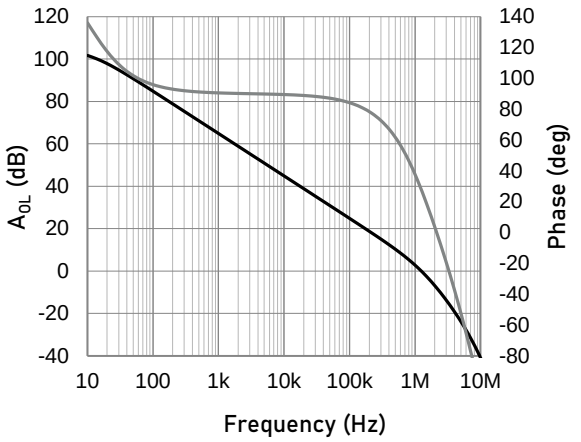
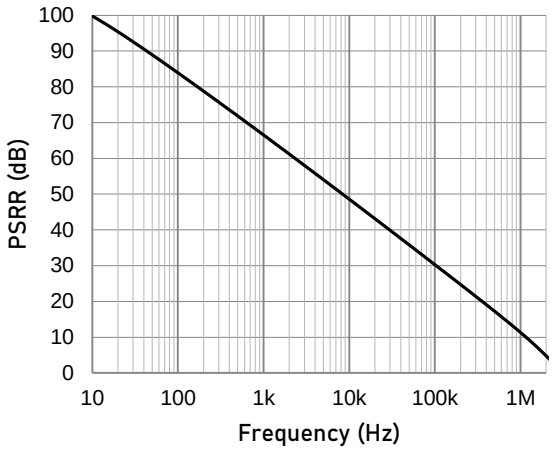
Typical Performance Characteristics

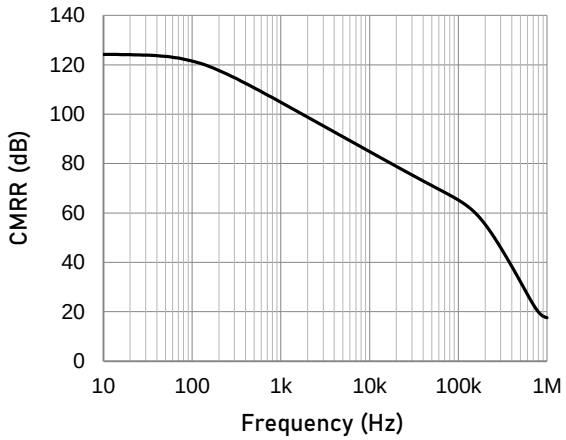
At T_A = +25°C, V_{CM} = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.



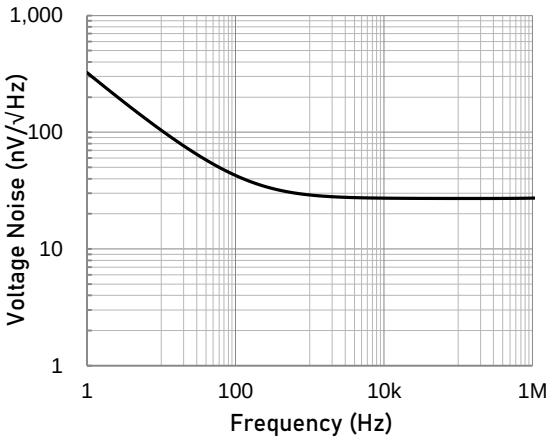
Open-loop Gain and Phase as a function of Frequency.



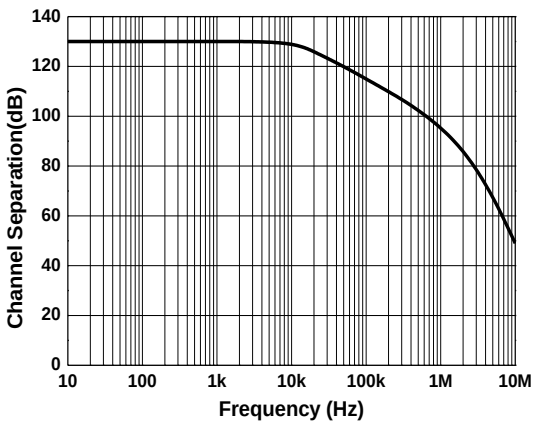
Power Supply Rejection Ratio as a function of Frequency.



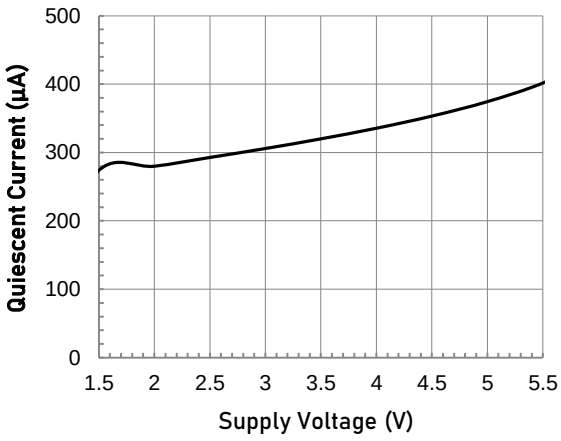
Common-mode Rejection Ratio as a function of Frequency.



Input Voltage Noise Spectral Density as a function of Frequency.



Channel Separation as a function of Frequency.



Quiescent Current as a function of Supply Voltage.

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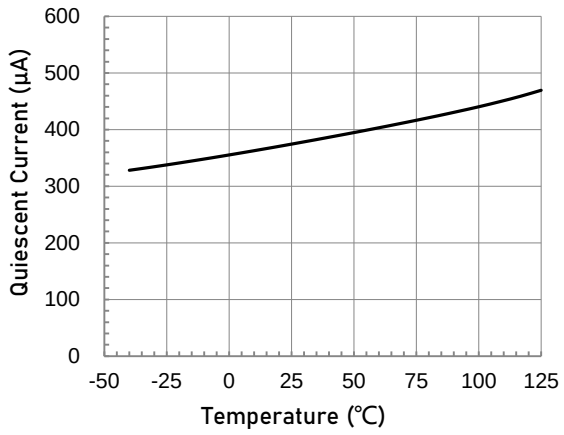
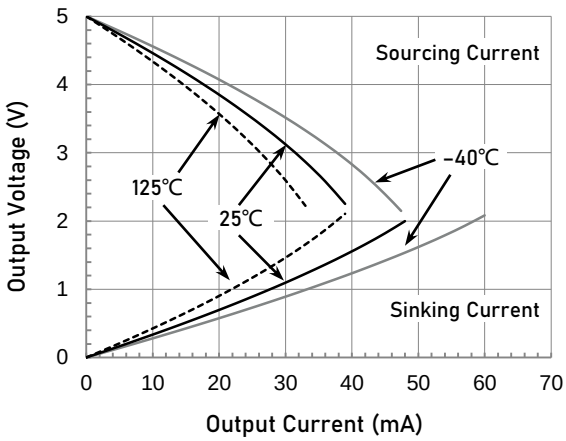
Typical Performance Characteristics (continued)

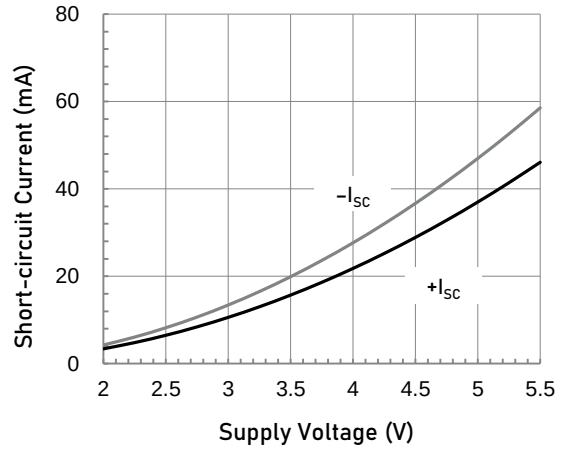
At T_A = +25°C, V_{CM} = V_S/2, and R_L = 10kΩ connected to V_S/2, unless otherwise noted.



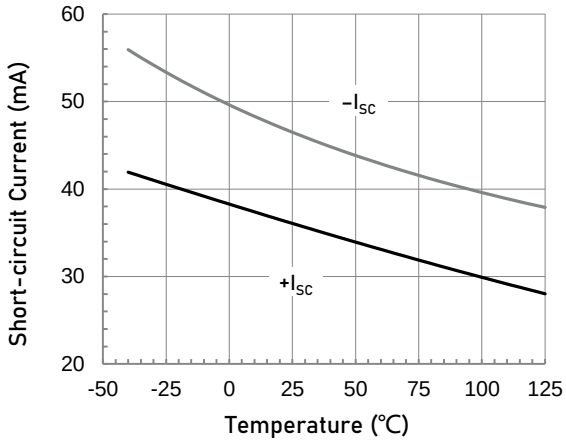
Quiescent Current as a function of Temperature.



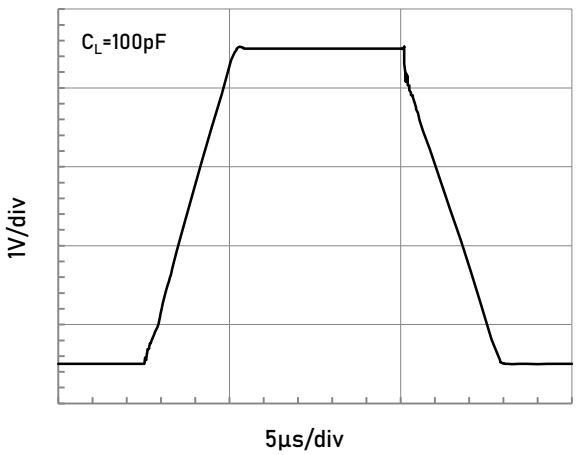
Output Voltage Swing as a function of Output Current.



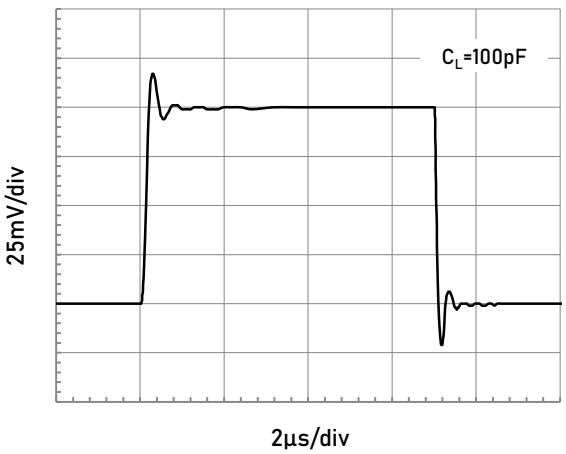
Short-circuit Current as a function of Supply Voltage.



Short-circuit Current as a function of Temperature.



Large Signal Step Response.



Small Signal Step Response.

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Application Notes

The LTC324H operational amplifier is unity-gain stable and free from unexpected output phase reversal. These devices use proprietary techniques to provide positive low offset voltage and low drift over temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifiers and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1µV/°C or higher, depending on materials used.

OPERATING VOLTAGE

The LTC324H family is fully specified and ensured for operation from 2.0 V to 5.5 V (±1.0 V to ±2.75 V). In addition, many specifications apply from –40 °C to +125 °C. Parameters that vary significantly with operating voltages or temperature are illustrated in the typical characteristics graphs.

NOTE: Supply voltages (V_{S+} to V_{S-}) higher than +10 V can permanently damage the device.

RAIL-TO-RAIL INPUT

The input common-mode voltage range of the LTC324H series extends 100 mV beyond the negative and positive supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically V_{S+}–1.4 V to the positive supply, whereas the P-channel pair is active for inputs from 100 mV below the negative supply to approximately V_{S+}–1.4 V. There is a small transition region, typically V_{S+}–1.2 V to V_{S+}–1 V, in which both pairs are on. This 200 mV transition region can vary up to 200 mV with process variation. Thus, the transition region (both stages on) can range from V_{S+}–1.4 V to V_{S+}–1.2 V on the low end, up to V_{S+}–1 V to V_{S+}–0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

The typical input bias current of the LTC324H during normal operation is approximately 1 pA. In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with electromagnetic interference (EMI) filter resistors to create the equivalent circuit. Notice that the input bias current remains within specification in the linear region.

INPUT EMI FILTER AND CLAMP CIRCUIT

Figure 1 shows the input EMI filter and clamp circuit. The LTC324H op-amps have internal ESD protection diodes (D1, D2, D3, and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 500 mV beyond the rails to be applied at the input of either terminal without causing permanent damage. These ESD protection current-steering diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 20 mA as stated in the Absolute Maximum Ratings.

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The EMI filter of the LTC324H family is composed of two 5 kΩ input series resistors (R_{S1} and R_{S2}), two common-mode capacitors (C_{CM1} and C_{CM2}), and a differential capacitor (C_{DM}). These RC networks set the –3dB low-pass cutoff frequencies at 35 MHz for common-mode signals, and at 22 MHz for differential signals.

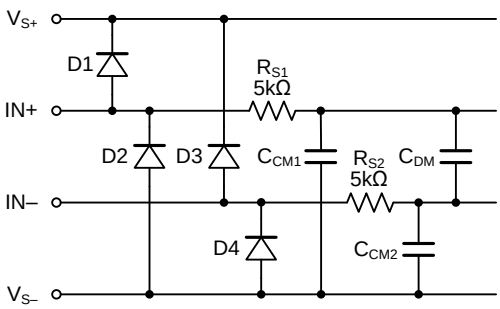

Figure 1. Input EMI Filter and Clamp Circuit

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Application Notes (continued)

RAIL-TO-RAIL OUTPUT

Designed as a micro-power, low-noise operational amplifier, the LTC324H delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 100 kΩ, the output swings typically to within 5 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails. For resistive loads up to 2 kΩ, the output swings typically to within 65 mV of the positive supply rail and within 42 mV of the negative supply rail.

CAPACITIVE LOAD AND STABILITY

The LTC324H family can safely drive capacitive loads of up to 500 pF in any configuration. As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces the phase margin and causes the amplifier frequency response to peak. Peaking corresponds to over-shooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if the LTC324H op-amps must drive a load exceeding 500 pF. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op-amp for capacitive load drive is by adding a series resistor, R_{ISO}, between the amplifier output terminal and the load capacitance, as shown in Figure 2. R_{ISO} isolates the amplifier output and feedback network from the capacitive load. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_L.

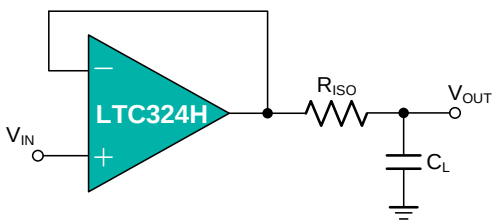

Figure 2. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 3. It provides DC accuracy as well as AC stability. The R_F provides the DC accuracy by connecting the inverting signal with the output.

The C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

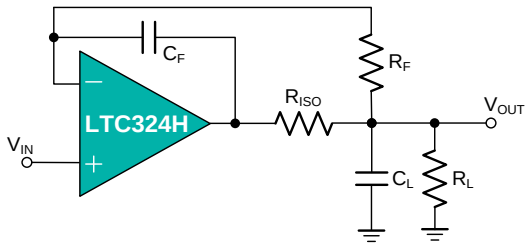

Figure 3. Indirectly Driving Heavy Capacitive Load with DC Accuracy

OVERLOAD RECOVERY

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the LTC324H family is approximately 2.5 µs.

EMI REJECTION RATIO

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an op-amp must accurately amplify the input signals. However, all op-amp pins — the non-inverting input, inverting input, positive supply, negative supply, and output pins — are susceptible to EMI signals. These high frequency signals are coupled into an op-amp by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op-amps can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

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Application Notes (continued)

The LTC324H op-amps have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20 \log (V_{IN_PEAK} / \Delta V_{OS})$$

INPUT-TO-OUTPUT COUPLING

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

MAXIMIZING PERFORMANCE THROUGH PROPER LAYOUT

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the LTC324H op-amps, care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs further reduces leakage currents. Figure 4 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

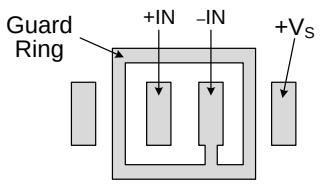

Figure 4. Use a guard ring around sensitive pins

Other potential sources of offset error are thermoelectric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

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Typical Application Circuits

DIFFERENTIAL AMPLIFIER

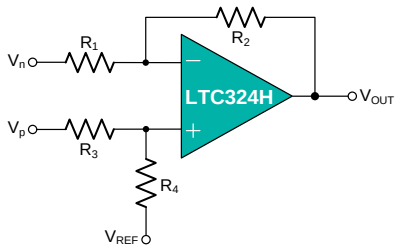
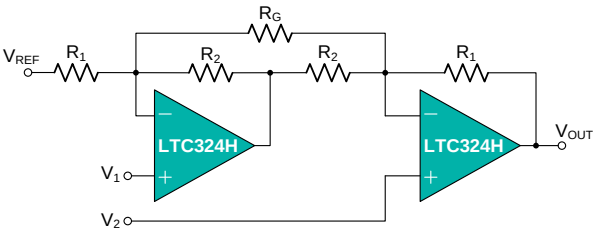


Figure 5. Differential Amplifier

The circuit shown in Figure 5 performs the difference function. If the resistors ratios are equal $R_4/R_3 = R_2/R_1$, then:

$$V_{OUT} = (V_p - V_n) \times R_2/R_1 + V_{REF}$$

INSTRUMENTATION AMPLIFIER

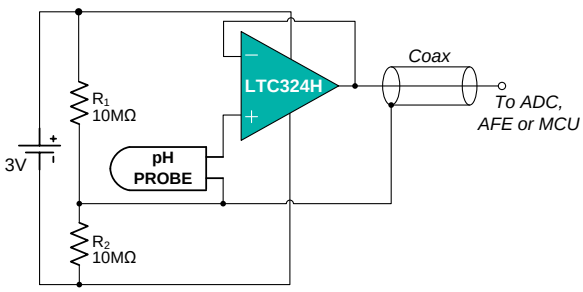


$$V_{OUT} = (V_1 - V_2)\left(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}\right) + V_{REF}$$

Figure 6. Instrumentation Amplifier

The LTC324H family is well suited for conditioning sensor signals in battery-powered applications. Figure 6 shows a two op-amp instrumentation amplifier, using the LTC324H op-amps. The circuit works well for applications requiring rejection of common-mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single voltage supply applications, the V_{REF} is typically $V_S/2$.

BUFFERED CHEMICAL SENSORS



All components contained within the pH probe

Figure 7. Buffered pH Probe

The LTC324H family has input bias current in the pA range. This is ideal in buffering high impedance chemical sensors, such as pH probes. As an example, the circuit in Figure 7 eliminates expansive low-leakage cables that that is required to connect a pH probe (general purpose combination pH probes, e.g Corning 476540) to metering ICs such as ADC, AFE and/or MCU. A LTC324H op-amp and a lithium battery are housed in the probe assembly. A conventional low-cost coaxial cable can be used to carry the op-amp's output signal to subsequent ICs for pH reading.

MOTOR PHASE CURRENT SENSING AMPLIFIER

The current sensing amplification shown in Figure 8 has a slew rate of $2\pi f V_{PP}$ for the output of sine wave signal, and has a slew rate of $2fV_{PP}$ for the output of triangular wave signal. In most of motor control systems, the PWM frequency is at 10 kHz to 20 kHz, and one cycle time is 100 µs for a 10 kHz of PWM frequency. In current shunt monitoring for a motor phase, the phase current is converted to a phase voltage signal for ADC sampling. This sampling voltage signal must be settled before entering the ADC. As the Figure 8 shown, the total settling time of a current shunt monitor circuit includes: the rising edge delay time (t_{SR}) due to the op-amp's slew rate, and the measurement settling time (t_{SET}). For a 3-shunt solution in motor phase current sensing, if the smaller duty cycle of the PWM is defined at 45% (In fact, the phase with minimum PWM duty cycle, such as 5%, is not detected current directly, and it can be calculated from the other two phase currents), and the t_{SR} is required at 20% of a total time window for a phase current monitoring, in case of a 3.3 V motor control system (3.3 V MCU with 12-bit ADC), the op-amp's slew rate should be more than:

$$3.3V / (100\mu s \times 45\% \times 20\%) = 0.37\ V/\mu s$$

At the same time, the op-amp's bandwidth should be much greater than the PWM frequency, like 10 time at least.

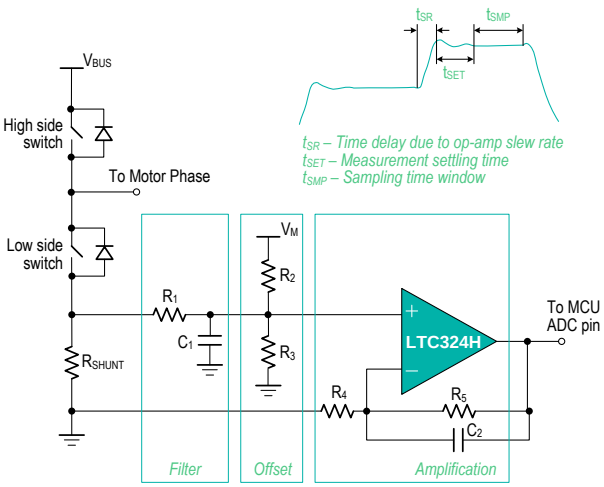


Figure 8. Current Shunt Monitor Circuit

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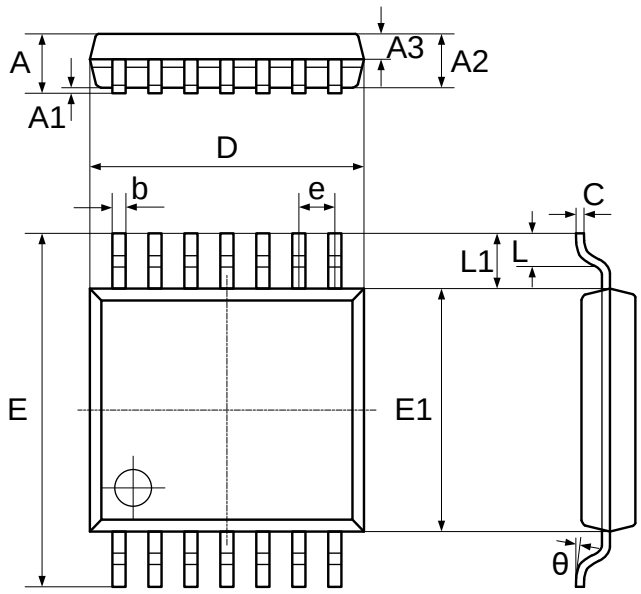
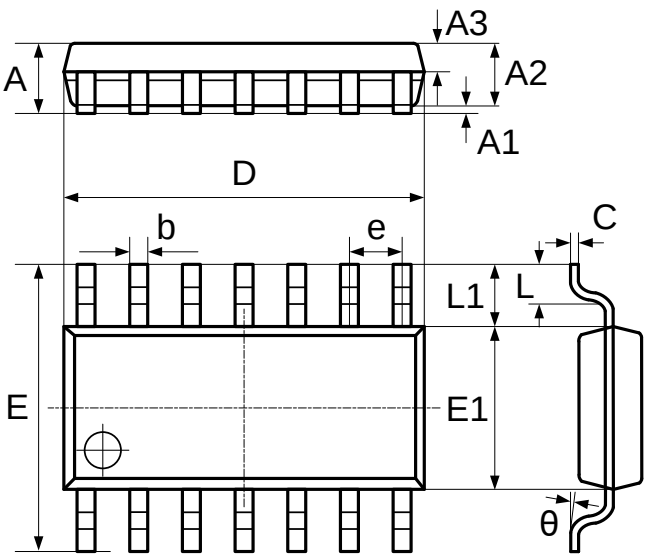
Package Outlines (continued)

TSSOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.0472
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.037	0.043
A3	0.390	0.490	0.016	0.020
b	0.200	0.290	0.008	0.012
C	0.130	0.180	0.005	0.007
D	4.860	5.060	0.198	0.207
E	6.200	6.600	0.253	0.269
E1	4.300	4.500	0.176	0.184
e	0.650 TYP.		0.0256 TYP.	
L1	1.000 REF.		0.0393 REF.	
L	0.450	0.750	0.018	0.031
θ	0°	8°	0°	8°

SOIC-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.450	1.850	0.059	0.076
A1	0.100	0.300	0.004	0.012
A2	1.350	1.550	0.055	0.063
A3	0.550	0.750	0.022	0.031
b	0.406 TYP.		0.017 TYP.	
C	0.203 TYP.		0.008 TYP.	
D	8.630	8.830	0.352	0.360
E	5.840	6.240	0.238	0.255
E1	3.850	4.050	0.157	0.165
e	1.270 TYP.		0.050 TYP.	
L1	1.040 REF.		0.041 REF.	
L	0.350	0.750	0.014	0.031
θ	2°	8°	2°	8°

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