DRV3946-Q1 Dual Channel Automotive Solenoid Driver with Current Regulation, Clamping and Diagnostics

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation to aid ISO26262 system design is available
  - Systematic integrity up to ASIL D
  - Hardware integrity up to ASIL C
- Highly integrated solenoid driver targeted at automotive EV contactor relay and solenoid control applications
  - Integration of power supplies, current regulation, diagnostics, and safety functions
  - High-efficiency solenoid driving with configurable peak and hold current settings
  - Built-in-self-test and diagnostic functions for power supplies, interfaces, drivers, and monitors
  - Architecture for reliable operation with redundant power supplies, low-side and high-side drivers, and secondary monitoring logic
- Up to 28V (40V abs. max) operating voltage
- Integrated modified half-bridge
  - For charging, recirculation and clamping
  - Typical $R_{DS(ON)}$: 37mΩ (low-side), 57mΩ (high-side)
  - Quick Turn Off with integrated clamp circuits
  - High-side clamp with redundant low-side clamp
- Low-side load control by single wire connection
  - Allows external high-side switch for redundant shut-off
- ± 5% accurate Low and High-side current sense
  - Analog load current feedback pin (IPROPI)
- Internal control mode:
  - Closed loop PWM current regulation
  - Configurable peak time, peak and hold currents
- External control mode:
  - Vary duty cycle at fixed PWM frequency
  - Vary PWM frequency at fixed duty cycle
- 4-wire, addressable, 24-bit SPI with CRC
  - Allows multiple devices to operate on same SPI
  - All devices on shared SPI bus can receive broadcast commands
- Comprehensive protection and diagnostics:
  - Device built-in-self-test
  - Load monitoring for open/short detection
  - Sensing loss of control during driver ON and OFF
  - Forced relay open for undercurrent or undervoltage
  - Redundant pin shut-off
  - Fault notification on nFAULT pin

2 Applications

- EV Contactor relays
- Peak and hold solenoids
- On and off relays
- Proportional solenoids
- Battery Disconnect Units (BDUs)
- Battery Junction Boxes (BJBs)
- Power Distribution Boxes (PDBs)
- Active Suspension Systems
- Vehicle Control Units (VCUs)

Package Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE (NOM)(2)
DRV3946-Q1	HTSSOP (28)	9.7mm X 4.4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length x width) is a nominal value and includes pins, where applicable.

Device Information

KEY FEATURES
Can drive two solenoids with high-efficiency
Low on-resistance power stage
Integrated clamp circuits for quick turn off
Closed-loop PWM current regulation
Configurable peak and hold currents and timing parameters
Up to 20kHz PWM frequency options
Comprehensive on and off-state diagnostics
Addressable 24-bit SPI

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

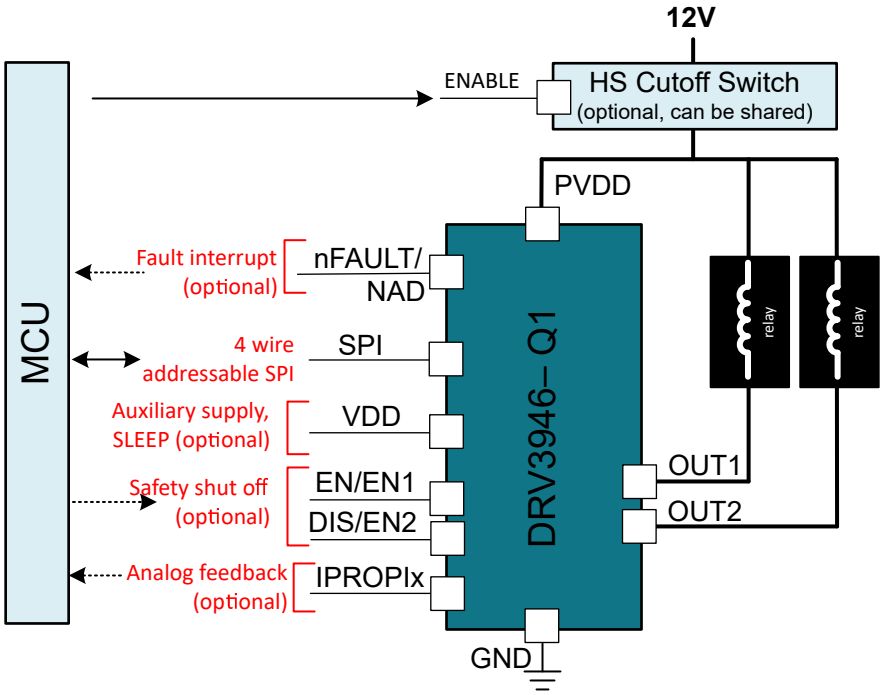
3 Description

The DRV3946-Q1 is a highly integrated solution to drive two solenoids for automotive applications such as contactor relays in EV battery management systems. It includes power supplies, current sensing and current regulation, configurable peak and hold currents and associated timings, and diagnostics and protection functions. It also incorporates several unique functions that enhance performance compared to traditional discrete solenoid drivers. These functions include integrated redundant clamp circuits to quickly discharge the load current, an addressable SPI, and modified half-bridge driver stage with low on-resistance switches.

The device controls solenoid loads through a single wire low-side connection and can pair with an external high-side switch (that can be shared) for redundant shut-off function. Integrated switches perform charging, recirculation and clamping. The device supports internal and external current control modes. The PWM frequency is configurable, with added low frequency dithering using automatic pseudo random frequencies generation and wave shaping. Internal PWM current control loop leads to reduced software development, since MCU current control loop is not needed. The DRV3946-Q1 supports flexible current control parameters to support wide range of solenoid types. Configurable peak and hold current and corresponding timing parameters allow system level power saving.

The DRV3946-Q1 is targeted to be functional safety-compliant, with ASIL-C rated functional safety goal for relay control and avoiding unintended operation. The device supports comprehensive protection and diagnostic features, such as continuous monitoring of load for open and short detection, on and off-state diagnostics, voltage monitors, short protection and high voltage rated IOs.

An addressable SPI allows multiple devices to be controlled on a shared SPI bus. In addition to reducing required MCU resources, the addressable SPI incorporates a broadcast command structure that can enable all devices on the shared addressed bus to take certain actions simultaneously. The SPI incorporates multiple robustness functions including a CRC, address readback capability, and various bus fault detection mechanisms.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2023) to Revision A (June 2024)	Page
• Updated Functional Safety text	1
• Updated text on broadcast command	1

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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5.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
DRV3946QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	3946

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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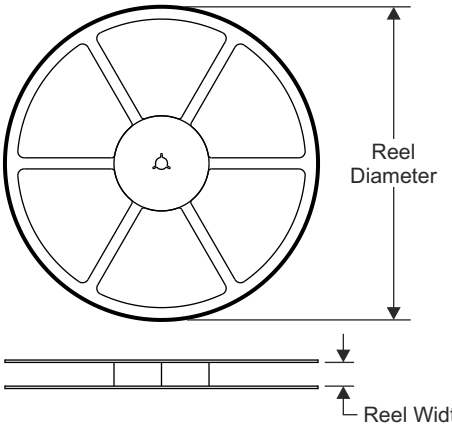
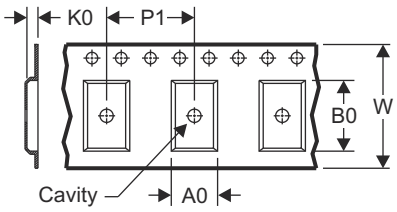
5.2 Tape and Reel Information

REEL DIMENSIONS

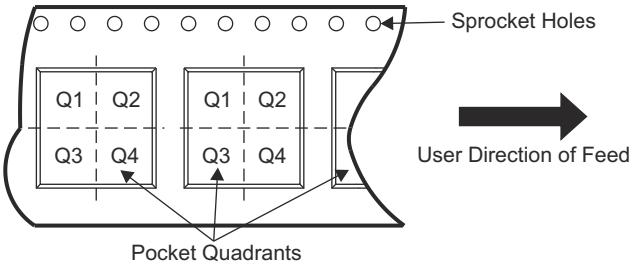


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV3946QPWPRQ1	HTSSOP	PWP	28	2500	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1

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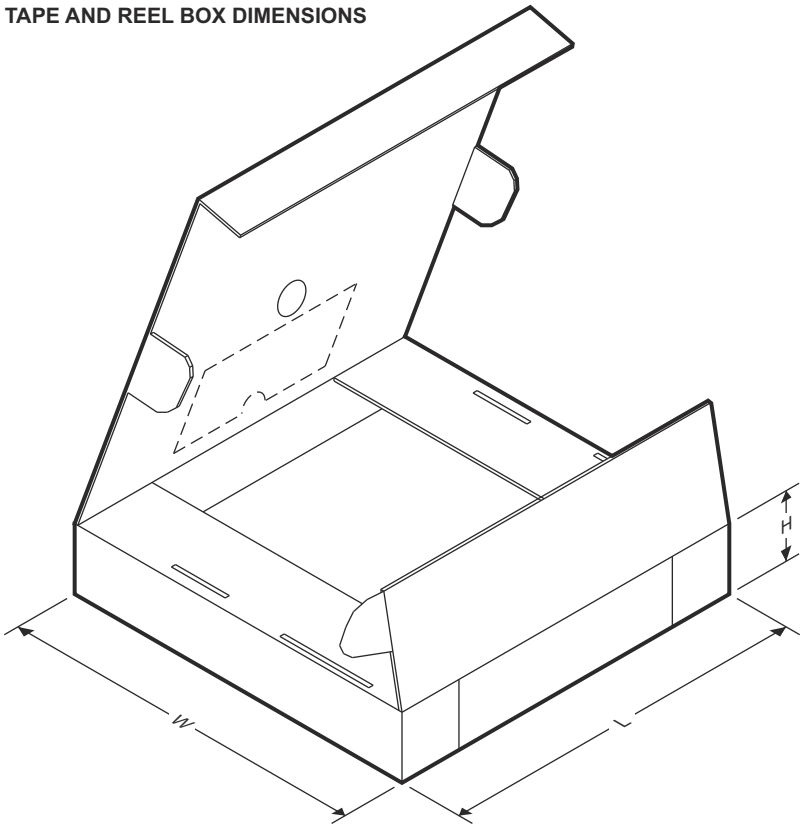
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV3946QPWPRQ1	HTSSOP	PWP	28	2500	356.0	356.0	35.0

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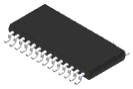
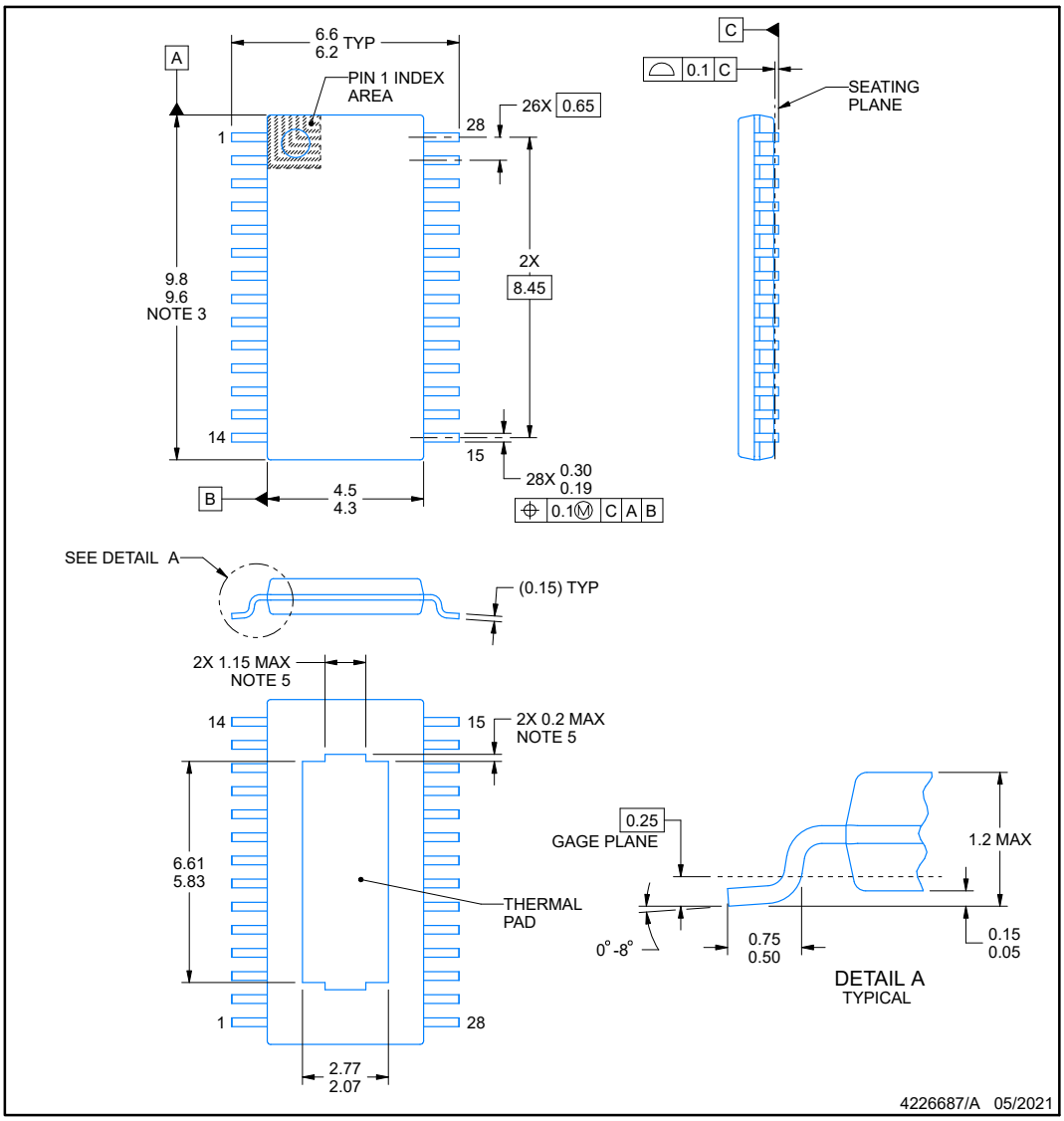
PACKAGE OUTLINE

PWP0028T



PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

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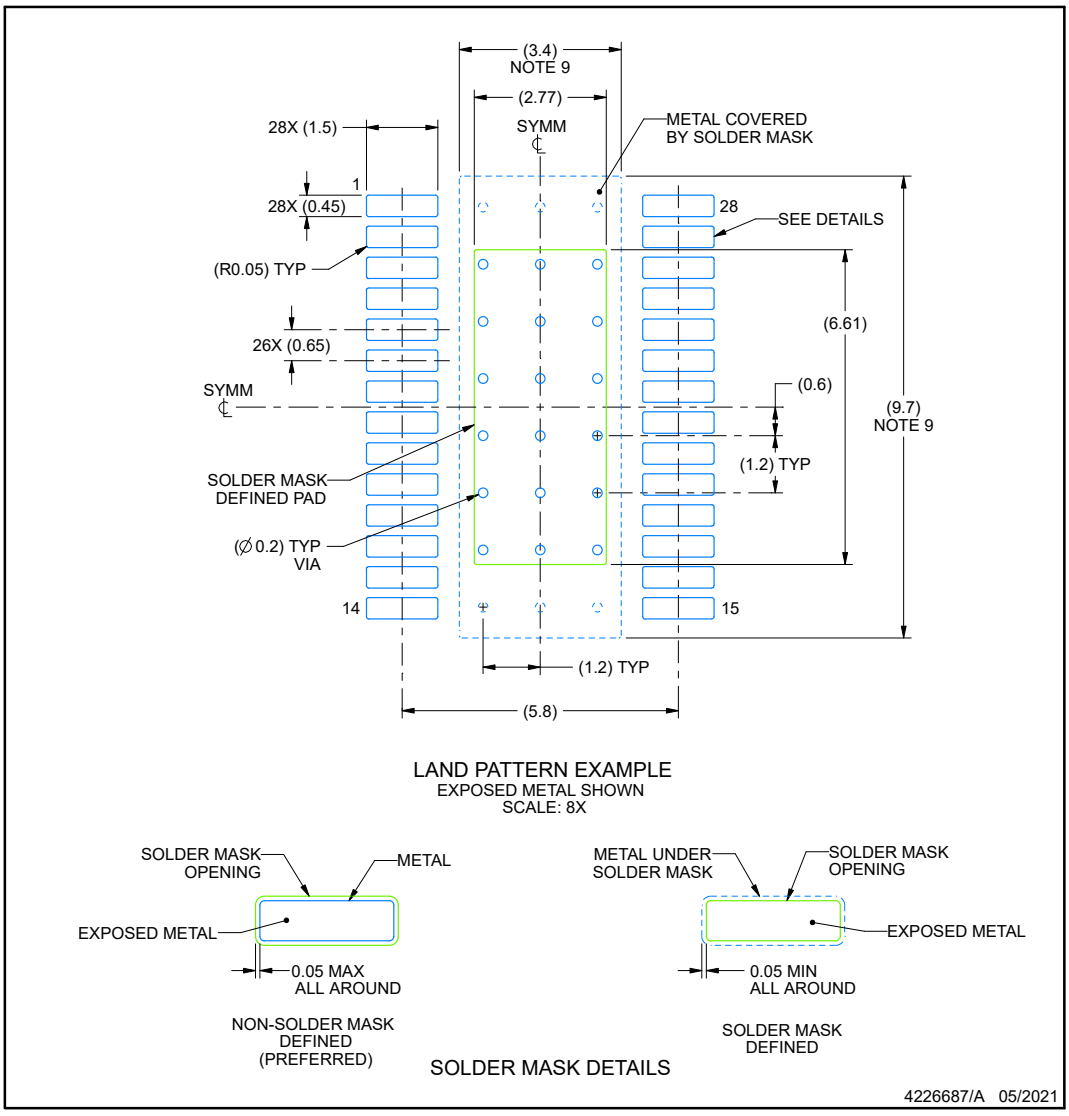
EXAMPLE BOARD LAYOUT

PWP0028T — **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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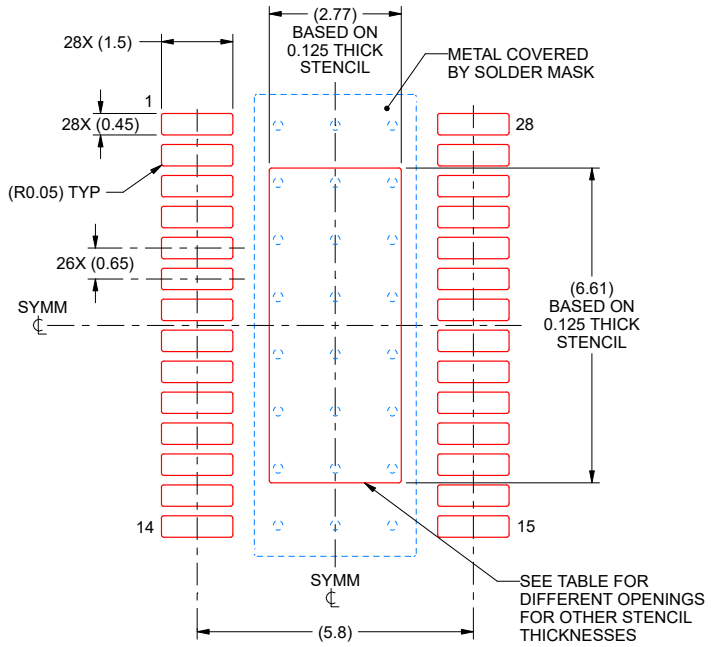
EXAMPLE STENCIL DESIGN

PWP0028T — **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.10 X 7.39
0.125	2.77 X 6.61 (SHOWN)
0.15	2.53 X 6.03
0.175	2.34 X 5.59

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV3946QPWPRQ1	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	3946
DRV3946QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	3946

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

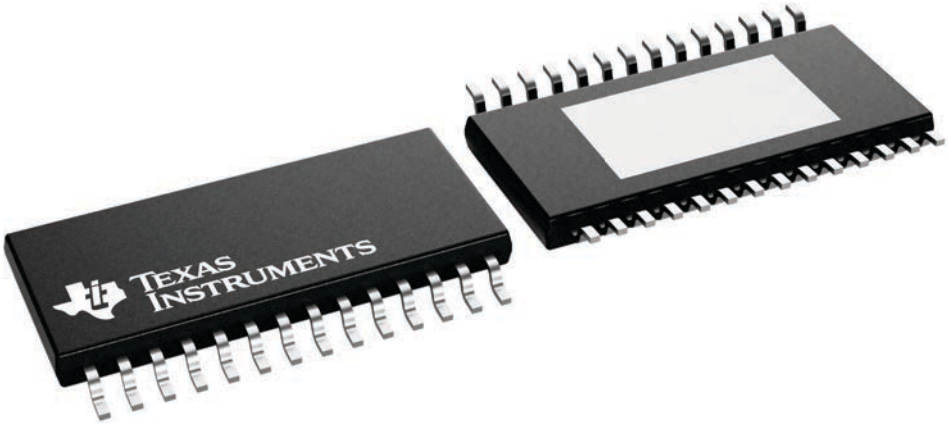
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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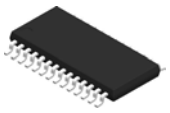
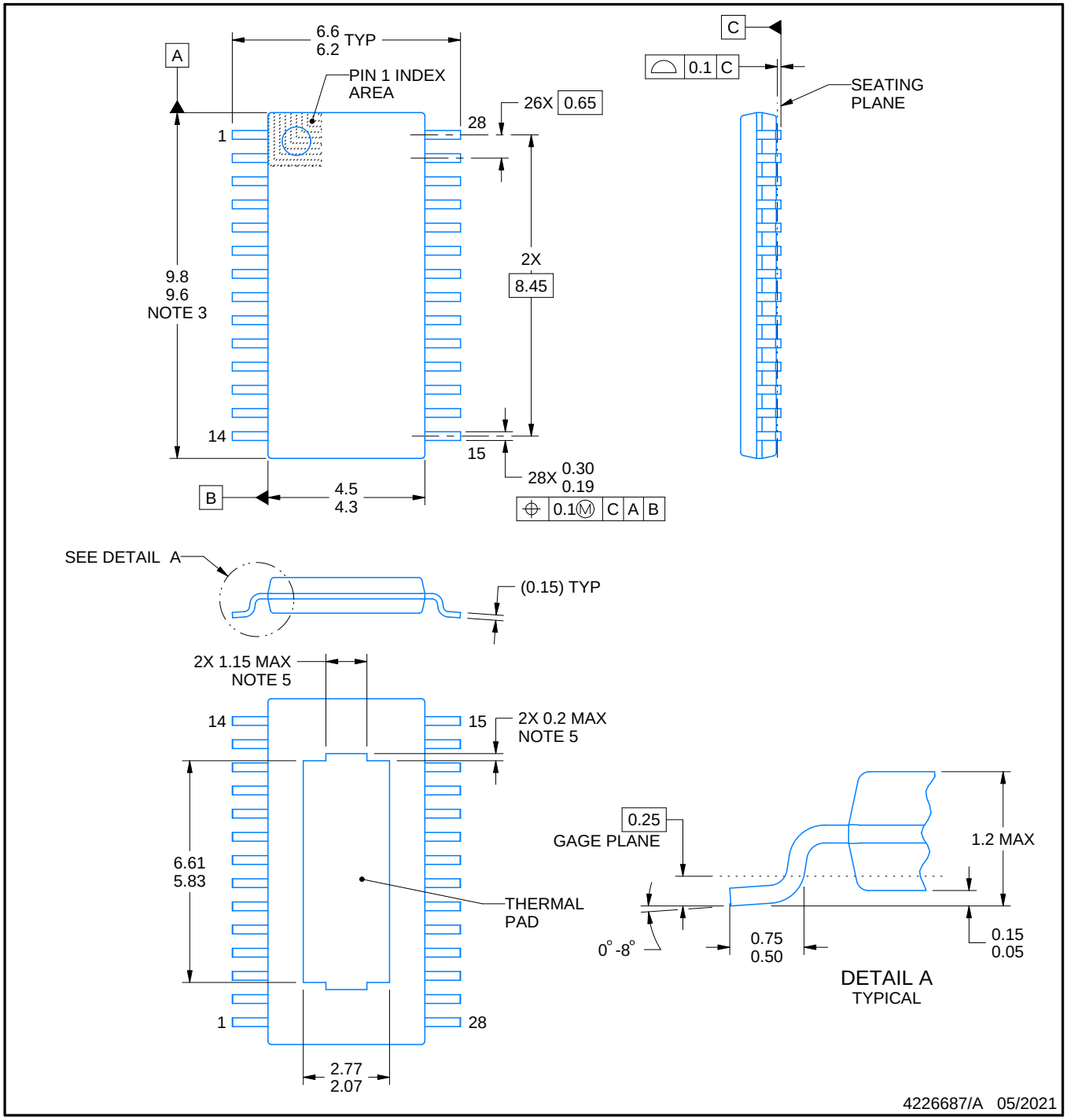
PACKAGE OUTLINE

PWP0028T



PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

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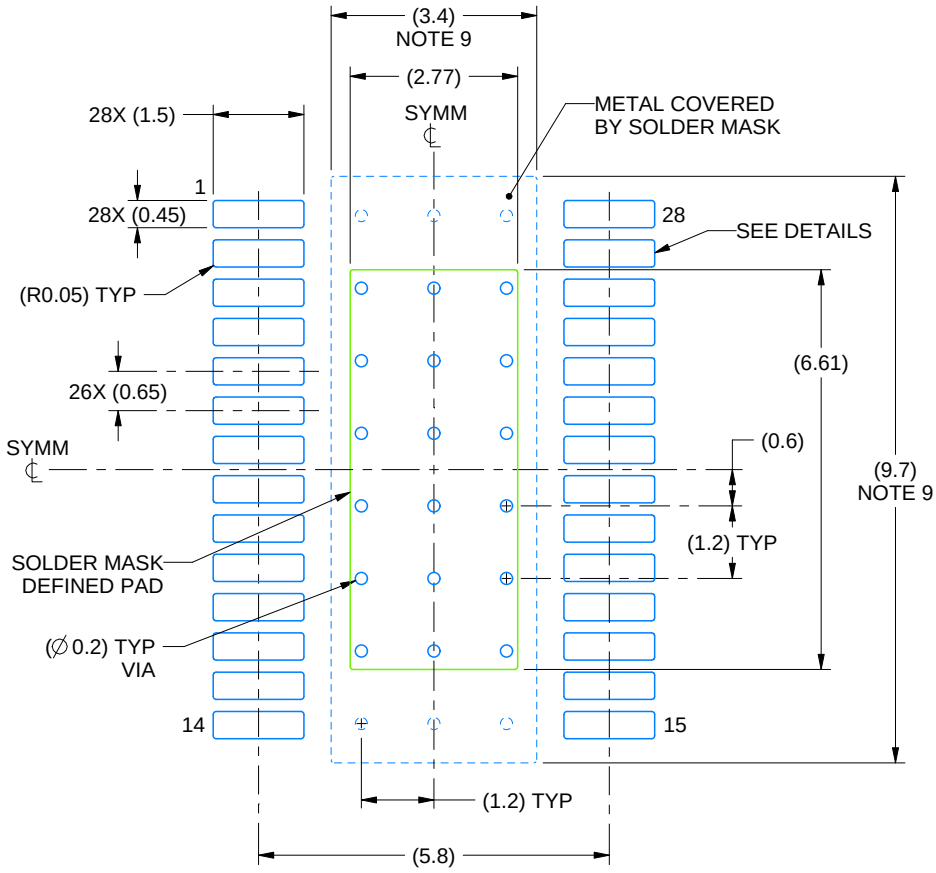
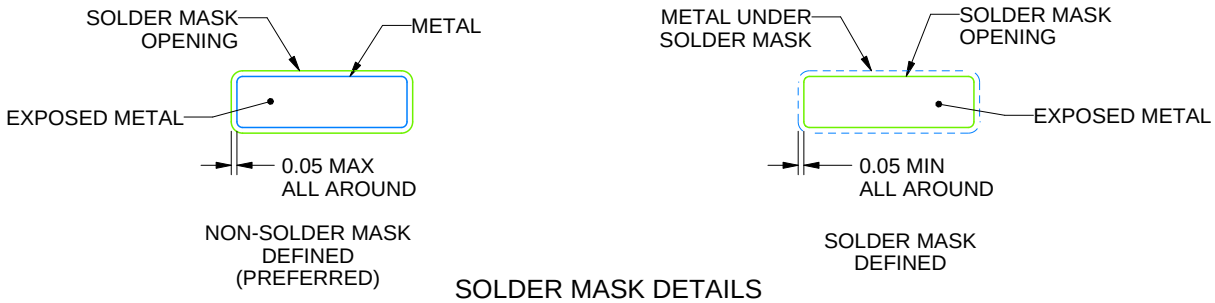
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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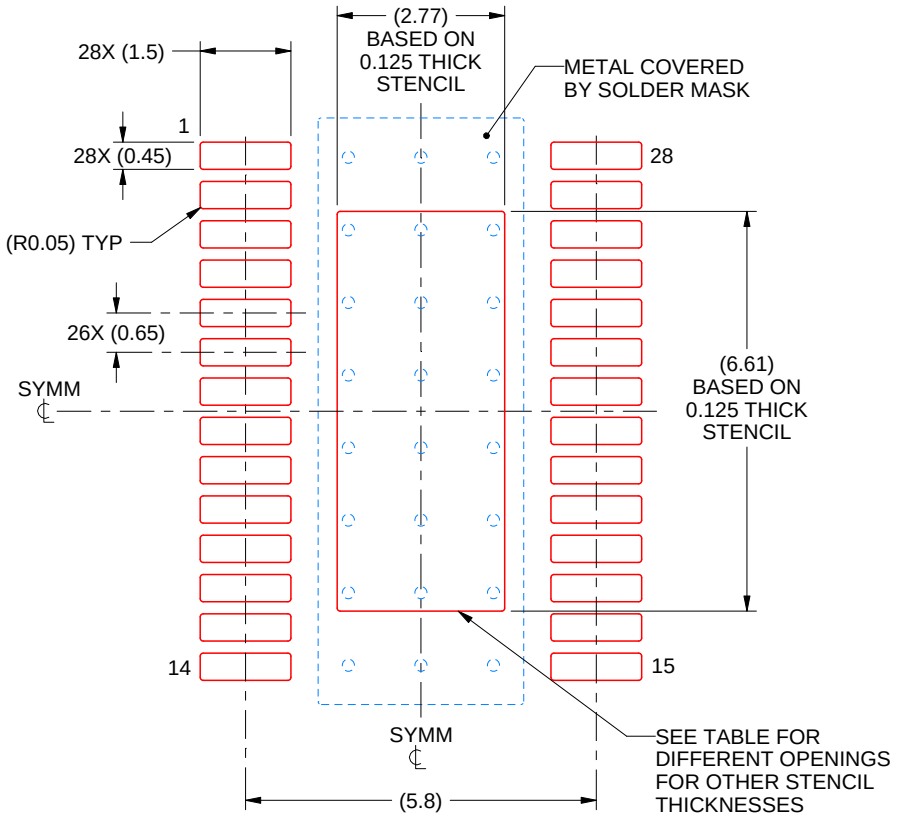
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.10 X 7.39
0.125	2.77 X 6.61 (SHOWN)
0.15	2.53 X 6.03
0.175	2.34 X 5.59

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NOTES: (continued)

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12. Board assembly site may have different recommendations for stencil design.

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