SPTECH Silicon NPN Power Transistors

DESCRIPTION

- With TO-3 package
- Low collector saturation voltage
- Excellent safe operating area

APPLICATIONS

- For use in high power audio amplifier applications and high voltage switching regulator circuits



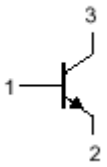


Fig.1 simplified outline (TO-3) and symbol

PINNING

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

Absolute maximum ratings(Ta=℃)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	70	V
V_{CEO}	Collector-emitter voltage	Open base	70	V
V_{EBO}	Emitter-base voltage	Open collector	6	V
I_C	Collector current		6	A
P_D	Total Power Dissipation	T_C=25℃	50	W
T_j	Junction temperature		175	℃
T_{stg}	Storage temperature		-55~175	℃

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CHARACTERISTICS

Tj=25℃ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CEO(SUS)}$	Collector-emitter sustaining voltage	I_C=50mA ;I_B=0	70			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E=1mA ;I_C=0	6			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=3A; I_B=0.3A			1.0	V
$V_{BE\ sat}$	Base-emitter saturation voltage	I_C=3A; I_B=0.3A			1.5	V
I_{CBO}	Collector cut-off current	V_{CB}=70V; I_E=0			0.1	mA
I_{EBO}	Emitter cut-off current	V_{EB}=6V; I_C=0			0.1	mA
h_{FE}	DC current gain	I_C=5A ; V_{CE}=4V	30		150	
f_T	Transition frequency	I_C=0.5A ; V_{CE}=12V		10		MHz

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PACKAGE OUTLINE

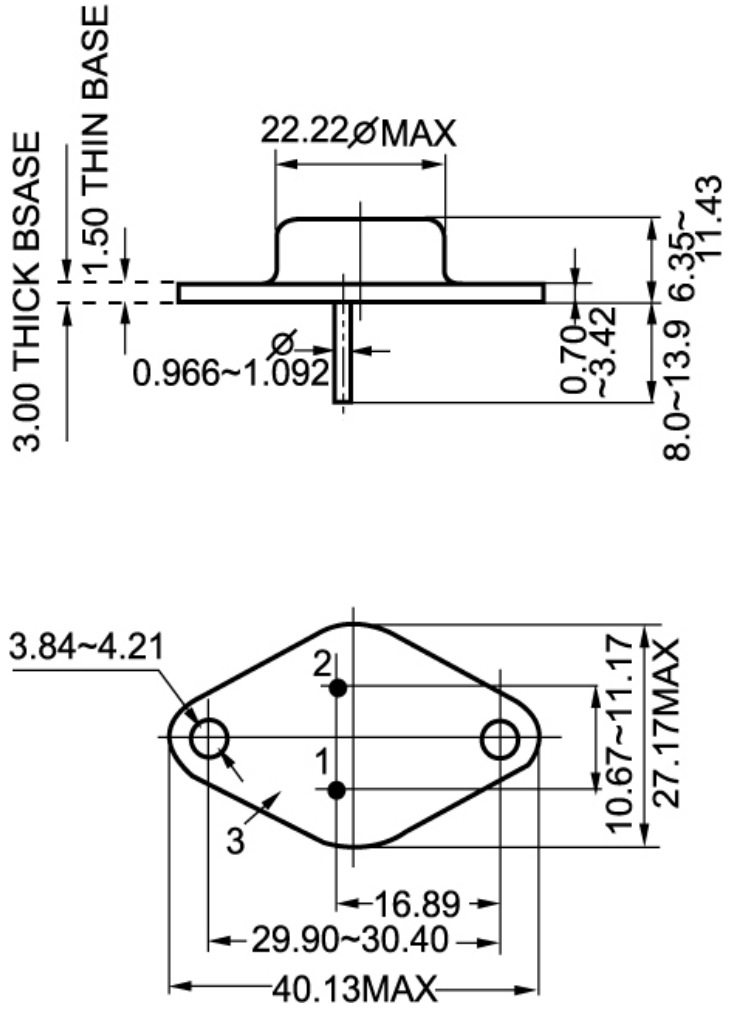


Fig.2 outline dimensions (unindicated tolerance:±0.10mm)